On-chip Power Supply for Subthreshold-Operated CMOS LSIs

Hideto Shimada Ken Ueno Tesuya Asai Yoshihito Amemiya
Department of Electrical Engineering, Hokkaido University
Kita 14, Nishi 7, Sapporo, 060-0814, Japan
shimada@lalsie.ist.hokudai.ac.jp

Abstract: An on-chip voltage supply regulator for subthreshold-operated CMOS logic LSIs is proposed. The regulator transforms lithium battery voltage 3 V to low supply voltage 0.4-0.5 V for subthreshold-operated CMOS logic LSIs. It monitors the gate delay in the LSI and produces an appropriate supply voltage such that the delay is equal to a value determined by a built-in capacitor-resistor reference. We designed the regulator circuit, using 0.18-μm CMOS parameters, and confirmed its operation with SPICE simulation.

Key-Words: - CMOS, LSI, subthreshold, on-chip, power supply, switching regulator, switched capacitor

1. Introduction

One promising area of research in microelectronics is the development of ultra-low power digital LSIs consisting of subthreshold-operated CMOS circuits, which are useful for energy-constrained applications such as micro-sensor network nodes [1-2], environmental monitoring tags, and implantable electronic medical devices. For such applications, lithium batteries are suitable energy sources because of their large energy density and small self-discharge. Therefore an on-chip voltage regulator is needed to transform lithium battery voltage 3 V to low supply voltage 0.4-0.5 V for subthreshold CMOS logic circuits. For such high-ratio voltage transformation, we designed a switched-capacitor voltage regulator described in the following.

2. Structure of the circuit

Block diagram

Figure 1 shows the block diagram of our voltage regulator consisting of a switched-capacitor converter, a delay-monitoring ring oscillator, a frequency comparator, and a clock generator to drive the converter. The converter accepts a battery voltage V_{EX} and produces a lower voltage V_{DD}, a supply voltage for subthreshold CMOS LSIs. The ring oscillator is also operated with V_{DD} to imitate gate operation in the LSI and thereby monitoring gate delay. A frequency comparator receives oscillation pulses from the ring oscillator and compares pulse frequency f to the time constant CR of a capacitor-resistor reference in the comparator. It detects the difference between $1/f$ and

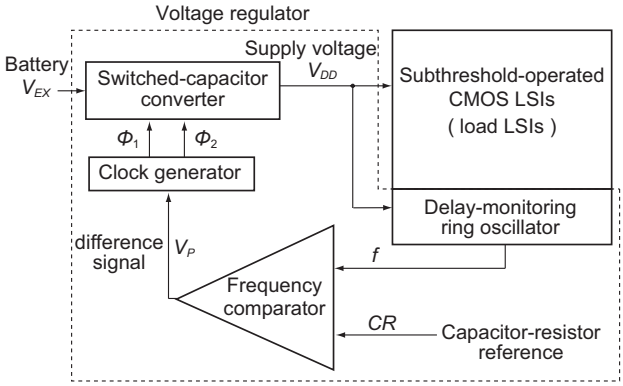

Fig. 1 Block diagram of voltage regulator.

CR, and sends the difference signal V_P to the clock generator. The clock generator produces non-overlapping clocks Φ_1 and Φ_2 to drive the switched-capacitor converter. As explained later, supply voltage V_{DD} is adjusted to an appropriate value such that the ring oscillator, therefore logic gates in the LSI, operates with a fixed speed determined by CR.

Switched-capacitor regulator

The switched-capacitor converter we used is shown in Fig. 2. Clocks Φ_1 and Φ_2 from the clock generator drive MOSFET switches M1-M14. The converter accepts battery voltage V_{EX} and produces output voltage V_{DD} by repeating charging and discharging of five capacitors C_R. During charging, the capacitors are series-connected with one another and connected to the battery. During discharging, they are parallel-connected and connected to load LSIs.

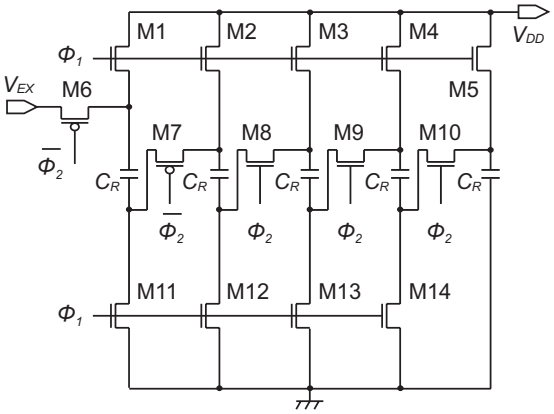

Fig. 2 Switched-capacitor converter.

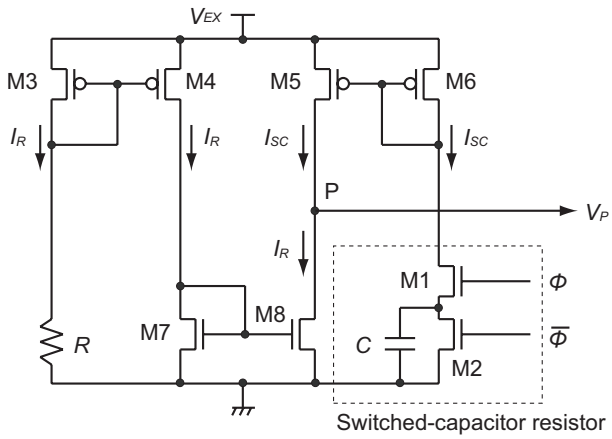

Fig. 3 Frequency comparator.

Output voltage V_{DD} depends on the frequency of the clocks.

Frequency comparator

Figure 3 shows the frequency comparator consisting of a switched-capacitor resistor (M1-M2-*C*) and a reference resistor *R* combined with each other through three current mirrors M3-M8. The switched-capacitor resistor is driven with pulses ϕ and $\overline{\phi}$ from the ring oscillator, with frequency *f*, and its resistance is 1/(*fC*). Current I_R in resistor *R* is given by

$$I_R = (V_{EX} - V_g)/R,$$

where V_g is the gate-source voltage of M3 (and M6). Current I_{SC} in the switched-capacitor resistor is given by

$$I_{SC} = fC\,(V_{EX} - V_g).$$

The voltage V_P of node P increases to V_{EX} for $I_R < I_{SC}$ and decreases to 0 for $I_R > I_{SC}$. Voltage signal V_P is sent to the clock generator.

Clock generator

The clock generator is a modified ring oscillator consisting of inverters with current-controlling pMOSFETs driven by voltage signal V_P from the frequency comparator. It produces non-overlapping clocks Φ_1 and Φ_2 to drive the switched-capacitor converter. The frequency of the clocks depends on V_P and decreases with increase in V_P.

Entire configuration

Figure 4 shows the entire circuit of our voltage regulator. The ring oscillator consists of NAND-gate inverters operated with voltage V_{DD} supplied by the converter, and it monitors gate delay in load LSIs. The output of ring oscillation drives the switched-capacitor resistor in the comparator through a non-overlapping pulse circuit. Node voltage V_P of the comparator drives the clock generator to produce clocks Φ_1 and Φ_2 for the converter. The entire circuit forms a feedback loop, and consequently, adjusts supply voltage V_{DD} so that frequency *f* of the ring oscillator will be 1/(*CR*); that is, the gate delay t_d of load LSIs will be

$$t_d = CR/(2n),$$

where *n* is the number of inverters in the ring oscillator.

3. Operation of the circuit

We confirmed the operation of our circuit, using SPICE simulation with a set of 0.18-μm CMOS parameters. Battery voltage V_{EX} was set to 3 V, converter capacitance C_R to 50 pF, and load LSI capacitance C_L to 500 pF. These capacitances are rather small and insufficient for the efficient operation of switched-capacitor converters, but we still used these so as to design an on-chip regulator. Resistance *R* and capacitance *C* in the comparator were set to 0.1 pF and 500 kΩ, and the number of NAND inverters in the ring oscillator was 3; that is, the regulator produced supply voltage V_{DD} such that the gate delay of load LSIs was 8.3 ns.

Figure 5 shows a waveform of supply voltage V_{DD} for a load current of 500 μA. Figure 6 depicts V_{DD} and ripple voltage as a function of load current. For load currents not more than 1 mA, V_{DD} was kept 0.49 V, a voltage needed to operate load LSIs with a 8.3-ns gate delay. A current of 1 mA suffices to operate a large subthreshold CMOS LSI. For larger load currents, V_{DD} dropped greatly because of an

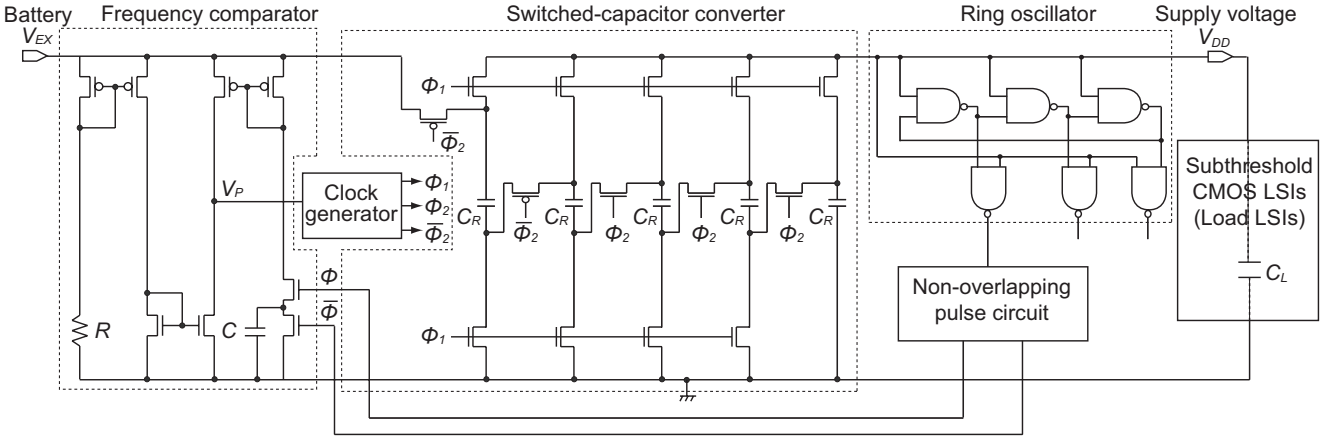

Fig. 4 Entire circuit of regulator.

insufficient charge of converter capacitance C_R. Large load current required frequent charging of C_R, or high-frequency switching of the converter, and this caused insufficient charge in C_R because of on-resistance of the switching MOSFETs in the converter.

Figure 7 shows the power efficiency of the regulator as a function of load current. The efficiency of the switched-capacitor converter was about 70 %. However, the total efficiency was only 35 % for 1-mA load current and decreases rapidly as load current decreased. This is so because the other components, especially the clock generator, consumed much energy regardless of load current. This is a problem because many subthreshold CMOS LSIs operate at 10-100 μA current and, therefore, the regulator has to provide such small currents with a high efficiency. We are now developing an improved, low-power clock generator.

This way, we designed an on-chip voltage regulator, or power supply, for subthreshold CMOS LSIs. Our regulator can be implemented with digital LSIs on a chip and would be useful to construct power-aware digital LSI systems.

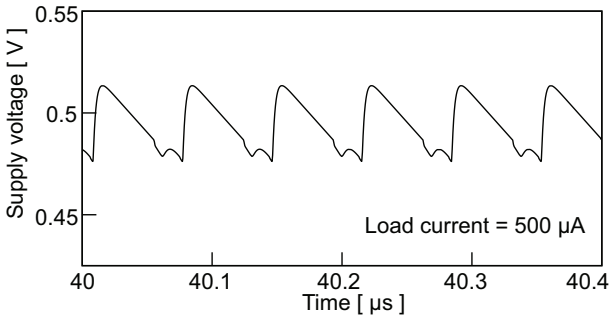

Fig. 5 Waveform of supply voltage V_{DD} (simulation).

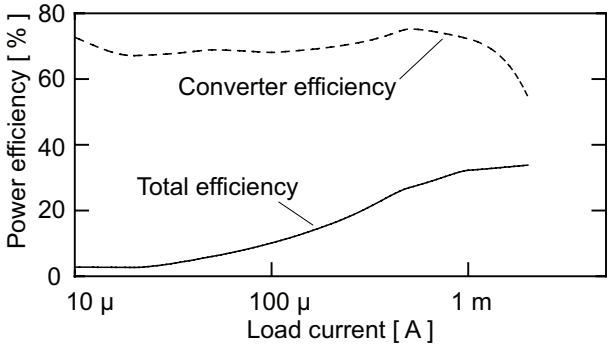

Fig. 6 Power efficiency as a function of load current (simulation).

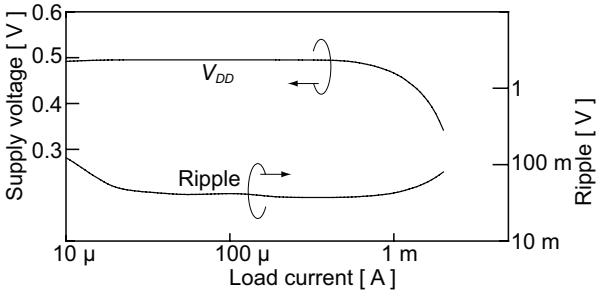

Fig. 7 Supply voltage V_{DD} and its ripple (simulation).

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