# On-Chip Solar Energy Harvester and PMU with Cold Start-Up and Regulated Output Voltage for Biomedical Applications

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***Abstract*—This paper presents experimental results from a system that comprises a fully autonomous energy harvester with a solar cell of 1 mm$^2$ as energy transducer and a Power Management Unit (PMU) on the same silicon substrate, and an output voltage regulator. Both chips are implemented in standard 0.18 $\mu$m CMOS technology with total layout areas of 1.575 mm$^2$ and 0.0126 mm$^2$, respectively. The system also contains an off-the-shelf 3.2 mm $\times$ 2.5 mm $\times$ 0.9 mm supercapacitor working as an off-chip battery or energy reservoir between the PMU and the voltage regulator. Experimental results show that the fast energy recovery of the on-chip solar cell and PMU permits the system to replenish the supercapacitor with enough charge as to sustain Bluetooth Low Energy (BLE) communications even with input light powers of 510 nW. The whole system is able to self-start-up without external mechanisms at 340 nW. This work is the first step towards a self-supplied sensor node with processing and communication capabilities. The small form factor and ultra-low power consumption of the system components is in compliance with biomedical applications requirements.**

***Index Terms*—Implantable devices, LDO, MPPT, on-chip energy harvesting, PMU, voltage reference generator**

## I. Introduction

Micro-energy harvesting has become an extended solution for low maintenance, small size and battery-less systems, such as implantable devices [1]–[3], wearable computing [4] or smart dust wireless sensors [5]. Recent research has demonstrated the solar micro-energy harvesting to be a viable solution in the field [1], [2]. The classical approach of light energy harvesting consists of an off-chip solar cell stuck over a CMOS chip with a Power Management Unit (PMU) [1]. Nevertheless, by integrating the solar cell and the CMOS circuitry on the same silicon substrate, a very small form factor and reduced cost can be met [6]. This approach, however, leads to several design challenges of the PMU. First, the scavenged power can be as low as a few nW. This makes it difficult to work without external control signals or start-up mechanisms [6]. Second, it is hard to handle a wide input power range with a significant energy efficiency [7]. As an example, the input power for an on-chip solar cell of 1 mm$^2$ varies from a few nW to several µW for an illumination range from 100 lx to 100 klx [8]. This calls for an efficient PMU with Maximum Power Point Tracking (MPPT) consuming nW and an ultra-low power voltage regulation module in order to keep the overall power budget of the system as low as possible.

A solution of a stand-alone sensing node comprises the sensor, the harvester with an energy reservoir, a processing unit and a wireless communication module. An intermediate approach would contain the harvester with the energy reservoir and the wireless unit to broadcast raw sensed data. A state-of-the-art full-custom solution is the System-in-Package (SiP) reported in [9], featuring standard Bluetooth Low Energy (BLE) communication with an average transmit power of 724 $\mu$W and an ultra-low power system-on-chip (SoC) for processing and harvesting consuming around 500 nW. The harvester BLE chip reported in [10] works from 0.2 V in transmitting mode. There are also off-the-shelf components as the chip DA14580 from Dialog Semiconductor [11] with current consumption of just 13.4 mA and 12.4 mA in receiver and transmitter modes, respectively, from supply voltages of 0.9 V. All these data might make feasible that the energy harvested by an on-chip energy transducer stored in an energy reservoir suffice for an energy autonomous sensing node. This is of utter importance in the context of biomedical applications, where low footprint and maintenance are a must. In addition, an energy transducer in standard CMOS technologies would reduce the cost of an implantable device.

Our work aims at a harvester with an on-chip solar cell and PMU on the same substrate in standard 0.18 $\mu$m CMOS technology. This paper presents a PMU powered by a 1 mm$^2$ on-chip solar cell fabricated on the same silicon substrate capable of rising up the harvested voltage above 1.3 V while driving an off-chip supercapacitor acting as an energy reservoir as well as a voltage regulation module. The small form factor and the absence of an external control of the proposed micro-energy harvesting system are very suitable for implantable devices. In particular, as a proof-of-concept application we target implantable intraocular devices for which the eye cavity dimensions limit the total size to roughly 5 mm $\times$ 5 mm $\times$ 1.5 mm.

This paper is the follow-up of a previous work, namely, the on-chip solar cell and PMU with unregulated output voltage addressed in [12], [13]. The present work includes

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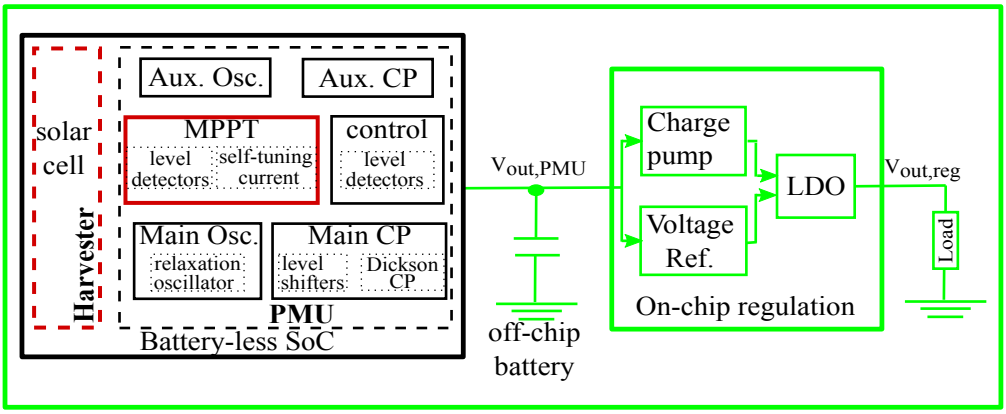


Fig. 1. Overview of the system containing a battery-less energy harvesting system consisting of an on-chip solar cell and a Power Management Unit (PMU) connected to an off-chip battery acting as energy reservoir and a voltage regulator. The integration of the harverster and the MPPT blocks (in red) on the same silicon substrate is the main novelty of the system. The boxes and components in green mark out the contribution with respect to previous work.

a voltage regulation module on a second chip featuring the ultra-low power voltage reference introduced in [14]. As an intermediate step towards a single chip with a PMU and an output voltage regulator or a SiP solution, this paper conveys an extensive set of experiments of both chips combined with the add-on of an off-chip supercapacitor on the way to energy autonomous ultra-low power sensing nodes with processing and communication functionalities.

The paper is organized as follows. Section II gives an overall description of the system with the two chips. Section III addresses the PMU with the energy transducer. Section IV explains the output voltage regulation. An extensive set of experimental results are collected in Section V. Finally, outlook and conclusions are conveyed in Section VI.

## II. Overall System Description

Fig. 1 shows the proposed architecture, consisting of a battery-less SoC composed of an on-chip solar cell and PMU fabricated on the same silicon substrate presented in [12], [13], connected to a voltage regulation module implemented on a second chip. The main novelty of this work, highlighted in red in Fig. 1, is on the integrated energy harvesting transducer and MPPT approach. This is based on a look-up table that takes into account the joint effect of the harvester's photodiode model at device level and the MPPT charge pump topology, where the gain, the flying capacitors and the frequency of oscillation are modified according to the incoming light. Also, the outer green box means the combination of the harvester chip and the voltage regulator, marking out the contribution provided by previously unpublished experimental results, as it is the case of the on-chip voltage regulator. The load and the off-chip battery are external components needed to assess the capacity of our system to self-supply energy for sensing and communication. The voltage regulator is supplied by the first chip and features an internal charge pump, a voltage reference generator, [14], and a capacitor-less low drop-out regulator (LDO). An off-chip supercapacitor that acts as an energy reservoir or off-chip battery has also been included in order to be able to handle load currents in the order of mAs.

The energy harvesting module consists of an on-chip solar cell as the only power source of the whole system directly

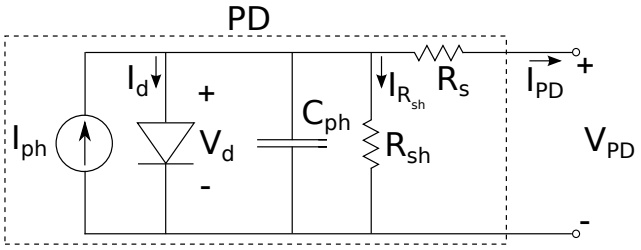


Fig. 2. Equivalent model of a photodiode as a solar cell.

connected to the PMU, with a total layout area of 1.575 mm$^2$, of which 1 mm$^2$ corresponds to the photodiode used as solar cell.

Differently from other energy harvesters based on power transfer through RF or ultrasound sources [15]–[17], usually a light energy harvester works in uncontrolled environments, where the energy amount provided from the outside varies widely. In implantable devices located in body areas exposed to light, such as inside the eye or under the skin, despite the high energy density provided by light in comparison with other energy sources [18], this wide variation in the input power is an issue which necessarily leads to design and technology challenges in order to provide a low footprint system with a long battery life. Some of the design challenges as ultra-low power techniques and an energy efficient MPPT are tackled in this paper. Nevertheless, we have not addressed technology challenges like the inclusion of high density storage elements such as buried capacitors in silicon. Also, from the system and application perspectives, extensive experiments in indoor and outdoor scenarios should be done to assess the lifespan of the battery when charged by environmental light. Still, harvested environmental light gives our system the possibility of collecting energy without an external element, which will be added only for RF communication purposes to transmit data collected along a given time interval. Controlled light environments also exist, as it is the case of clinics for intraocular pressure monitoring through tonometers in glaucoma patients, which employ slit lamps with light intensities that can reach 200 klx.

The PMU features two operation modes, start-up and normal

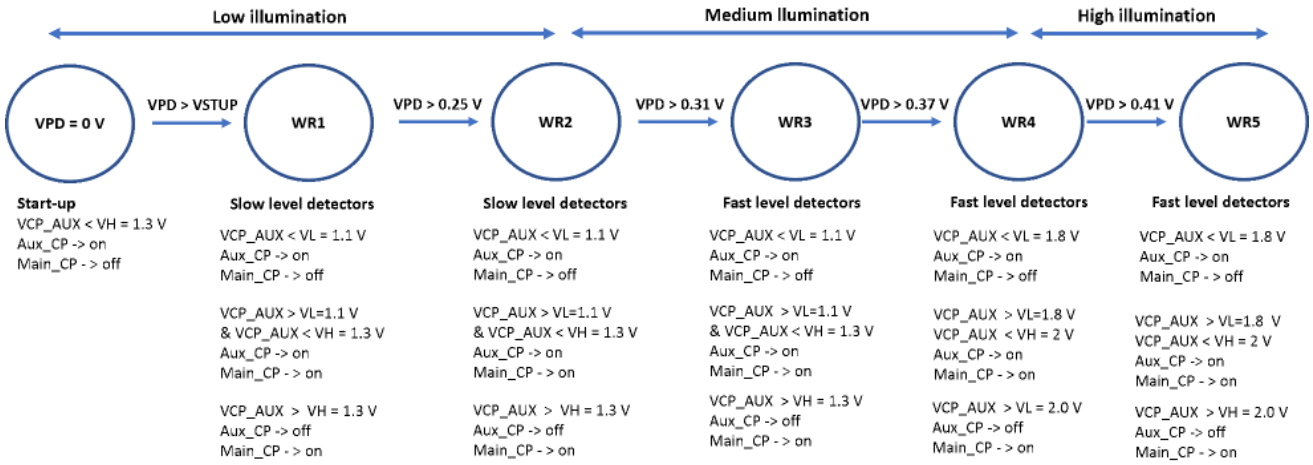


Fig. 3. State diagram of the power gating of the auxiliary and main oscillators and charge pumps across the different working regions (WRs) defined by our MPPT approach.

operation. The PMU includes an auxiliary oscillator (Aux. Osc.) driving an auxiliary charge pump (Aux. CP) that generates the voltage levels of both the control circuit and the main charge pump switches. The main oscillator and charge pump are OFF during the start-up process by means of power gating to cut energy consumption. The auxiliary DC-DC converter starts working when the voltage generated by the photodiode, $V_{PD}$, is high enough to switch on the auxiliary oscillator and to trigger the self-start-up process, $V_{PD} = V_{STUP} = 0.17$ V. The output voltage of the PMU, $V_{out,PMU}$, is an unregulated voltage provided by the main DC-DC converter.

The working principle of the PMU is based on a Maximum Power Point Tracking (MPPT) block which is always connected to the solar cell and works in an open-loop and continuous mode.

The voltage regulator has been designed to achieve very low power consumption with a reduced size. It features an on-chip low power voltage reference generator, [14], a charge pump and a capacitor-less LDO, being the total layout area of just 0.0126 mm$^2$. The voltage reference circuit is directly powered by $V_{out,PMU}$, while the LDO supply voltage is taken as the output of the on-chip Dickson charge pump increasing the unregulated PMU output voltage to a value of 3.3 V.

With the goal of achieving a fully autonomous and self-powered system, an off-the-shelf off-chip supercapacitor was connected to the output of the PMU in order to act as an energy reservoir. We used the CPX3225A752D module from Seiko Instruments with dimensions of 3.2 mm $\times$ 2.5 mm $\times$ 0.9 mm. The module implements an electric double layer capacitor (EDLC) providing a low internal impedance of only 25 $\Omega$ and low leakage current. This permits our solution to manage peak load currents of the order of mAs without draining the system.

## III. Energy Harvester and Power Management Unit

The system features a DC energy source, in particular, a 1 mm$^2$ on-chip solar cell for energy harvesting purposes directly connected to the PMU in order to save area. A photodiode as solar cell is typically modeled by the circuit shown in Fig. 2, [19]. This model features a current source $I_{ph}$, and a diode modeled as $I_d = I_s(e^{V_d/nV_T} - 1)$, where $I_s$ is the reverse saturation current, $n$ is the diode ideality factor and $V_T$ is the thermal voltage. $C_{ph}$ is the junction capacitance of the photodiode. $R_{sh}$ is a shunt resistance that accounts for the manufacturing defects, and $R_s$ is the series resistance that models device contacts and connections. As reported in [8], mixed circuit-device simulations for a $P^+$ over P-well in N-well over P-substrate during the design phase have allowed us to estimate current levels in the order of tens of $\mu$A for illumination levels in the order of tens of klx. Also, as shown with experimental results, different photodiode configurations with fingers of different pitch, and thus with different lateral photocollection capacities, have been measured to choose the best photodiode layout.

Concerning the PMU, its wide energy range from nW to $\mu$W without external control signals or start-up mechanisms is met with the combination of ultra-low power techniques and a novel MPPT approach. Our MPPT is inspired by the Fractional Open Circuit Voltage (FOCV) method, since the maximum power point is tracked through the photodiode voltage, $V_{PD}$, [20]. However, in our approach we do not measure the photodiode open circuit voltage but, instead, we use a lookup table defined during the design phase to adjust the gain and stage capacitance of the main charge pump, as well as the frequency of the clock signals of both the auxiliary and main charge pumps across five working regions (WR). This lookup table was defined using a joint analytical model of both the photodiode and the charge pump presented in a previous work [8]. As a result, four level detectors have been used to distinguish among five different working regions (WR1-WR5) for the MPPT to cover the whole voltage range of the photodiode. Their nominal trigger voltages were set to $V_{0V25}$ = 0.25 V, $V_{0V31}$ = 0.31 V, $V_{0V37}$ = 0.37 V and $V_{0V42}$ = 0.42 V during the design phase.

One of the low power design solutions for the PMU is to run power gating on both the auxiliary and the main oscillators and charge pumps, as well as to keep the output of the auxiliary charge pump $V_{CP\_AUX}$ limited across the WRs defined by

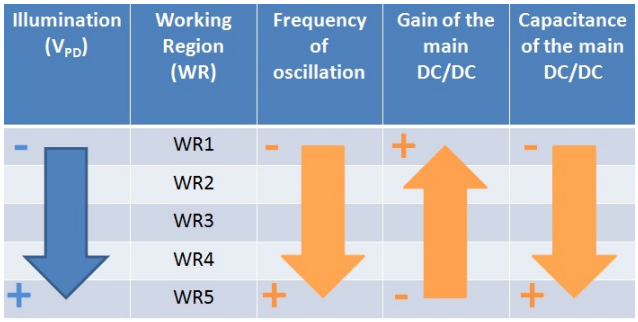


Fig. 4. Open-loop and continuous MPPT working principle: 5 WR are defined according to the illumination level ($V_{PD}$). For each WR the gain and stage capacitance of the main charge pump as well as the frequency of oscillation of both the main and auxiliary charge pumps is modified accordingly.

the MPPT approach. This is done with the control block implemented as a finite state machine event driven by the photodiode voltage $V_{PD}$, as illustrated in Fig. 3. As seen, $V_{PD}$ triggers transitions between states, including the start-up of the system when $V_{CP\_AUX}$ crosses the start-up threshold voltage $V_{STUP}$, and where Aux_CP and Main_CP mean auxiliary and main charge pumps, respectively. Different voltage level detectors in the control block (see Fig. 1) have been designed to match the incoming power light. As a consequence, slow and low power detectors are used in low illumination, while the opposite in high illumination. Also, voltage levels $V_L$ and $V_H$ are set to separate start-up from normal operation and to run power gating in the control circuit and the auxiliary and main oscillators and charge pumps across WRs. Finally, it should also be noted that level shifters are needed to provide voltage levels compatible with the high voltages, e.g., $V_H$ = 2 V, used in the control block.

The MPPT also modifies parameters in the auxiliary and main oscillators and charge pumps. Nevertheless, as the auxiliary oscillator and charge pump are critical to start up from a very low input power, their overhead power for programmability is kept to a minimum. Thus, the power efficiency of the PMU is mainly optimized in the main oscillator and charge pump throughout the input light power span. Fig. 4 shows the trend in different parameters of the main charge pump across WRs. Fig. 5 shows the connection between the MPPT block and the auxiliary and the main oscillators and charge pumps. It includes a self-tuning current circuit implemented with transistors in diode connection as reported in [13] and biased by $V_{PD}$, which is the power supply of the auxiliary and main oscillator, and as such changes the frequency of the auxiliary oscillator and performs a fine tuning of the frequency of the main oscillator across WRs independently of the charge pump topology by modifying their bias voltage.

The main DC-DC converter is based on a Dickson charge pump with transmission gates as switches and with variable gain and capacitance per stage, [12], [13]. As illustrated by Fig. 4, capacitances and gain of the main DC-DC converter are programmed for every WR according to the $V_{PD}$ voltage, searching for the maximum load current $I_{LMAX}$ at a given PMU output voltage, which in the case of the PMU as a stand-alone chip had been designed as 1.1 V. This search is

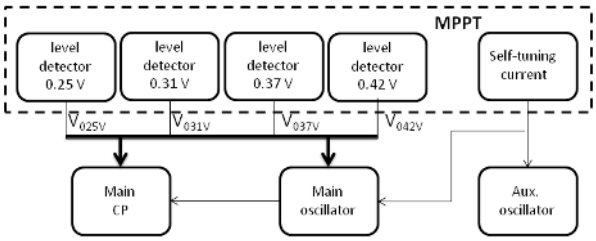


Fig. 5. MPPT architecture.

carried out during the design phase with a joint analytical model of photodiode and charge pump reported in [8]. Still, the equivalent circuit model and the dynamic equation of the charge consumed by the main charge pump implemented as a Dickson topology [21] allows to understand the trend in its gain, frequency and capacitance values displayed on Fig. 4 to achieve the maximum charge or power efficiency according to the incident light power.

On the one hand, a Dickson charge pump can be modeled by an equivalent RC circuit model with parameters $R_{eq}.C_{eq}$ regardless of the driven load. The equivalent resistance $R_{eq}$ is given by [21]:

$$R_{eq} = \frac{N}{C.f} \tag{1}$$

where $C$ is the pumping or flying capacitance of every stage, assuming all of them with the same value, $N$ is the number of stages, and $f$ is the frequency of the two non-overlapping clock signals of the charge pump. The equivalent $C_{eq}$ is $C_T/3$, with $C_T$ being the sum of all flying capacitances. In our case, the input to the main charge pump is the photodiode voltage, i.e. $V_{PD}$. Higher input power levels, and thus higher $V_{PD}$ voltages mean a larger input current available. Equation (1) shows that in order to provide the highest possible current to the load, a charge pump with few stages $N$, as well as larger pumping capacitances $C$ and a higher clock frequency $f$ is needed. This matches impedances, leading to more power transfer from the photodiode to the load.

On the other hand, the charge consumed by a Dickson charge pump during the rise time of its output voltage $V_{out}$ from $t = 0$ until $t_{target}$ is formulated as [21]:

$$Q = (N+1)\left(\frac{C_T}{3} + C_L\right)\left[V_{out}(t_{target}) - V_{out}(0)\right] + \alpha C_T V_{PD}\frac{t_{target}}{T} \tag{2}$$

where $C_L$ is the load capacitance, and $V_{out}(t_{target})$ and $V_{out}(0)$ are the settled and initial output voltages, $\alpha$ is a technology dependent constant which accounts for the charge drawn by the parasitic capacitances of the flying capacitors of the charge pump, and $T$ is the period of the two non-overlapping clock signals.

The terms proportional to $C_L$ and $C_T$ of (2) mean the charge transferred to the load capacitance $C_L$ and the charge drawn by the charge pump, respectively, while the term proportional to $V_{PD}$ is the charge consumed in the parasitic

capacitances, which is wasted power, and as such it decreases power efficiency. Low light power makes the charge wasted in the parasitic capacitances larger in comparison with the useful charge transferred to $C_L$, thus, larger gains through more stages $N$ combined with a smaller $C_T$ and longer clock periods $T$, and thus lower frequencies, lead to higher power efficiencies. High light power allows for smaller gains, a larger $C_T$ and higher frequencies. Also, larger gains for a higher input light power, and thus, a higher $V_{PD}$, would lead to prohibitively high output voltages in the main charge pump, decreasing power efficiency too. CAD simulations and an upper limit for reconfigurability of the main charge pump to keep PMU area low have led us to the next gains and capacitances across WRs, namely, $\times 7$ with 100 pF per stage of the charge pump for WR1, $\times 6$ with 200 pF for WR2, $\times 5$ with 400 pF for WR3, $\times 4$ with 600 pF for WR4 and $\times 4$ with 750 pF for WR5. Finally, in terms of technology, capacitors used for high illumination are made with PMOS transistors (PCAPs) to shrink area, while the stages that are active for low illumination are PCAPs and MIM devices connected in parallel to reduce leakage currents.

Although (1) and (2) are fundamental design equations of the main charge pump, the design procedure also accounts for other circuits in the PMU. As an example, the search for the optimum frequency of the two non-overlapping clock signals of the main charge pump should include the power of the oscillator that provides such signals. A first qualitative argument to explain the frequency trend of Fig. 4 with the charge pump and the oscillator is that higher frequencies lead to higher dynamic power drawn by the oscillator and at the gate of the charge pump switches. Low illumination calls for low frequencies to support the power demanded by the different PMU circuits. The design methodology followed in this work was to make use of the joint analytical model introduced in [8] combined with CAD simulations of all circuits in the PMU.

An additional low power mechanism in the main charge pump is the inclusion of high gate voltages in its switches to decrease resistive losses. In so doing, we implement level shifters driven by the level detectors of the MPPT block. Details of such level circuits are found in [13].

The auxiliary charge pump is a Pelliconi circuit [22] of 8 stages with NMOS transistors in P-well as diodes to avoid the substrate effect and increase the efficiency of the converter, and thus, that of the start-up phase. The capacitors are implemented with MIM structures to maintain low leakage currents. As stated above, the converter has a fixed gain and capacitance per stage in order to keep power consumption low and start up from as low an illumination as possible, so as shown in Fig. 5, the frequency of the clock signal is the only way to adjust the output power of the converter according to the illumination.

In terms of circuit implementation, the main and auxiliary oscillators are relaxation oscillators based on [23]. Both of them are free running oscillators without any specific start-up mechanism. Also, both of them share two solutions to change their frequencies; through the change of their power supply, i.e., $V_{PD}$, and through a fine adjustment with a biasing voltage that sets an internal current in both circuits. This biasing

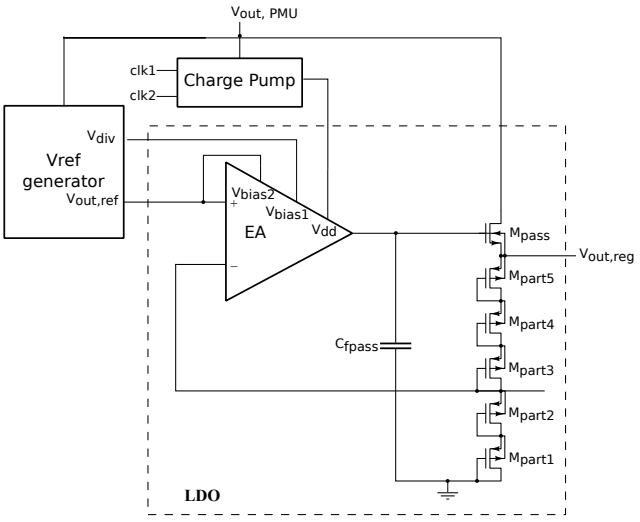


Fig. 6. Architecture of the voltage regulator module composed of a reference voltage generator, a charge pump and an LDO.

voltage is the voltage generated by a cascode topology of transistors in diode mode supplied by $V_{PD}$ too, providing a current range from 50 pA for $V_{PD} = 0.2$ V up to 4 nA for $V_{PD} = 0.5$ V. These two solutions make the frequency of both oscillators change in an increasing monotone sequence across WRs. Additionally, the frequency of the main oscillator changes in discrete steps by selecting five different capacitance values in a capacitor bank according to the WR. As a consequence, the resultant frequency of the main oscillator varies continuously from 100 Hz to 150 kHz. The frequency of the auxiliary oscillator changes in the range of 1.5 kHz to 500 kHz. Finally, the trigger voltage of every level detector of the MPPT block is set by a PMOS cascode structure [24]. These voltages ($V_{0V25}$, $V_{0V31}$, $V_{0V37}$, or $V_{0V42}$) are defined by adjusting the dimensions of transistors with different threshold voltages. Further details of all these circuits can be found in [13].

## IV. Voltage regulation module

The energy harvesting with PMU described in the previous section provides an unregulated output voltage, $V_{out,PMU}$. In this section we describe a voltage regulation module aiming at providing a target regulated output voltage of $V_{out,reg}$ = 1.3 V. The voltage regulation module considered in this case, depicted in Fig. 6, includes a classical capacitor-less LDO architecture consisting of a pass transistor, $M_{pass}$, an error amplifier (EA) and a feedback network, transistors $M_{parti}$ ($i = 1, 2, ..., 5$). It also features a charge pump and a reference voltage generator. For the LDO, an NMOS pass transistor has been chosen as stability requirements are less stringent and it shows better Power Supply Rejection (PSR) than their PMOS counterpart, [25]. In order to accommodate large load currents using an NMOS pass transistor, sufficiently large voltages are needed at the gate of $M_{pass}$. For this reason, we have incorporated a 3-stage Dickson charge pump, shown in Fig. 7, to increase the supply voltage of the error amplifier to a value of $V_{out,CP} = 3.3$ V, with the input voltage of the charge pump,

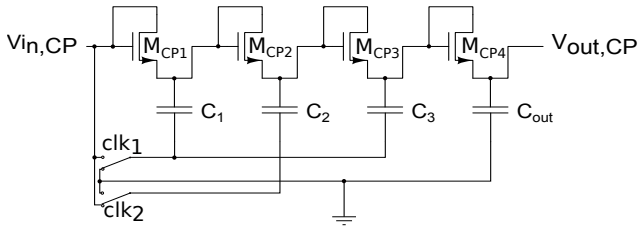


Fig. 7. Architecture of the 3-stage Dickson charge pump of the voltage regulation module.

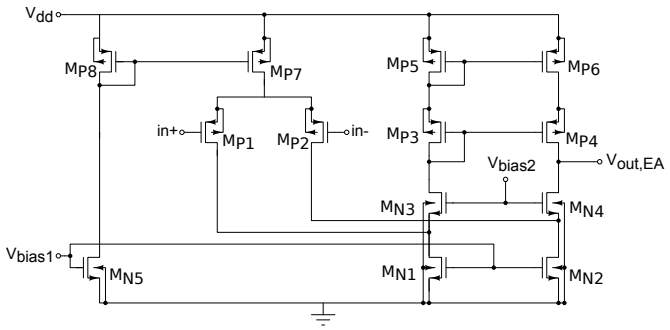


Fig. 8. Circuit schematic of the LDO error amplifier.

being the output of the PMU, $\mathrm{V_{in,CP}} = \mathrm{V_{out,PMU}}$. The switches have been implemented using transmission gates. The output voltage neglecting the losses due to the switches capacitances can be calculated as (3),

$$V_{\mathrm{out,CP}} = 4\,V_{\mathrm{out,PMU}} - (V_{th1} + V_{th2} + V_{th3} + V_{th4}) \qquad (3)$$

where $V_{th1}$, $V_{th2}$, $V_{th3}$ and $V_{th4}$ are the threshold voltages of transistors $\mathrm{M_{CP1}}$, $\mathrm{M_{CP2}}$, $\mathrm{M_{CP3}}$ and $\mathrm{M_{CP4}}$ in Fig. 7, respectively.

The error amplifier has been implemented using a folded-cascode structure with a PMOS differential input pair, Fig. 8. The amplifier dominant pole, $w_{\mathrm{EA}}$, is located at the output node due to both its high impedance and the relatively large output capacitance, which corresponds to the parasitic capacitance of the pass transistor $M_{\mathrm{pass}}$ and to capacitor $C_{\mathrm{fpass}}$, and coincides with the LDO dominant pole, $w_{\mathrm{LDO}}$. The frequency of the dominant pole can be calculated as,

$$w_{\mathrm{EA}} = w_{\mathrm{LDO}} = \frac{1}{R_{\mathrm{out,EA}}\,C_{\mathrm{pass}}} \qquad (4)$$

with $C_{\mathrm{pass}}$ being the capacitance between the gate of the pass transistor and ground and $R_{\mathrm{out,EA}}$ the output impedance of the error amplifier,

$$R_{\mathrm{out,EA}} = \frac{\left(\frac{r_{o\mathrm{MN2}}\,r_{o\mathrm{MP2}}}{r_{o\mathrm{MN2}}+r_{o\mathrm{MP2}}}\,g_{m\mathrm{MN4}}\,r_{o\mathrm{MN4}}\right)\left(r_{o\mathrm{MP6}}\,g_{m\mathrm{MP4}}\,r_{o\mathrm{MP4}}\right)}{\left(\frac{r_{o\mathrm{MN2}}\,r_{o\mathrm{MP2}}}{r_{o\mathrm{MN2}}+r_{o\mathrm{MP2}}}\,g_{m\mathrm{MN4}}\,r_{o\mathrm{MN4}}\right) + \left(r_{o\mathrm{MP6}}\,g_{m\mathrm{MP4}}\,r_{o\mathrm{MP4}}\right)} \qquad (5)$$

The non-dominant pole at the output of the LDO can be calculated as

$$w_{\mathrm{out,LDO}} = -\frac{g_{\mathrm{mpass}} + g_{\mathrm{opass}} + g_{\mathrm{L}} + g_{\mathrm{part}}}{C_{\mathrm{L}} + C_{\mathrm{gspass}} + C_{\mathrm{sdpass}}} \qquad (6)$$

where $g_{\mathrm{mpass}}$ and $g_{\mathrm{opass}}$ are the transconductance and the inverse of the drain source resistance of the pass transistor, respectively, $g_{\mathrm{L}}$ is the load conductance, $g_{\mathrm{part}}$ the conductance

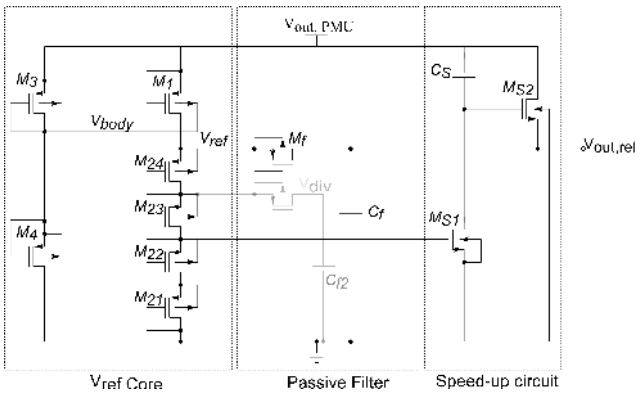


Fig. 9. Circuit schematic of the voltage reference generator.

of the voltage divider formed by transistors $M_{\mathrm{part}i}$, $C_{\mathrm{L}}$ the load capacitance and $C_{\mathrm{gspass}}$, $C_{\mathrm{sdpass}}$ the gate source and source drain capacitances of the pass transistor. As the value of both $g_{\mathrm{mpass}}$ and $g_{\mathrm{L}}$ decreases for small load currents, which would move the frequency of the output pole close to that of the dominant pole and cause stability problems, the voltage divider formed by transistors $M_{\mathrm{part}i}$ has been dimensioned as to ensure a minimum current consumption of approximately 100 pA at the target value of $\mathrm{V_{out,reg}}$ = 1.3 V to guarantee the stability of the LDO. The biasing voltages of the error amplifier, $V_{\mathrm{bias1}}$ and $V_{\mathrm{bias2}}$, are taken from the voltage reference generator shown in Fig. 9.

The voltage reference circuit uses only regular transistors in standard 0.18 $\mu$m CMOS technology and has been developed for its application in body implantable devices [14]. The main objectives are to achieve a very low power consumption, low process sensitivity and good PSR, disregarding temperature dependency because in this context the temperature will remain approximately constant and equal to 36° C. It is composed of a $V_{ref}$ core, a passive RC low-pass filter and a speed-up circuit. The core of the reference voltage generator does not have a feedback loop. Transistors $M_3$ and $M_4$ at the left branch are series connected and generate a control voltage $\mathrm{V_{body}}$. At the right branch, transistors $M_1$ and $M_{2i}$ are also series connected and generate an output voltage $\mathrm{V_{ref}}$. The stacked diode connected transistors $M_{21}$, $M_{22}$, $M_{23}$, $M_{24}$ are used to obtain a higher reference voltage without increasing the current level through the right branch. Thus, the left branch controls the right branch through voltage $\mathrm{V_{body}}$, but there is no implicit feedback loop. The $M_f$ transistor and $C_f$ capacitor form an RC low-pass filter to improve high frequency PSR of the voltage reference as seen in [26]. In addition, a speed-up mechanism has been added given that due to the low current flowing through $M_1$ to maintain low power consumption and the high resistance of the filter transistor $M_f$, the time necessary to charge $C_f$ capacitor can be excessively large, resulting in a high settling time. To minimize this effect, a simple speed-up circuit is proposed, which injects charge on the output node when the supply voltage is connected and switches off once the voltage $\mathrm{V_{out,ref}}$ settles. The speed-up circuit consists of transistors $\mathrm{M}_{S1}$ and $\mathrm{M}_{S2}$ and capacitor $C_S$. When the supply voltage goes from 0 to $\mathrm{V}_{dd}$, with $\mathrm{V}_{dd}$ =

$V_{out,PMU}$, the gate voltage of $M_{S2}$ reaches a value close to $V_{dd}$ causing a voltage increase in $V_{ref}$ due to the current through $M_{S2}$. Then, $C_S$ capacitor is charged across $M_{S1}$ decreasing $M_{S2}$ gate voltage while $M_{S1}$ gate voltage increases cutting off $M_{S2}$ and isolating the output node from $V_{dd}$. The aim of the speed-up circuit is simply to enhance the switching-on time of the output voltage and plays no role in setting the circuit operating point.

## V. Experimental Results

The proof-of-concept system is composed of two chips, shown in Fig. 10 and an off-chip supercapacitor for energy storage. The first chip was fabricated in standard 0.18 µm CMOS technology and includes the solar cell and the PMU with a form factor of 1.575 $mm^2$ plus additional structures for testing purposes. Fig. 10(a) shows a microphotograph of the $5 \times 5$ $mm^2$ chip marking the position of the device under test considered in this work. The solar cell considered is a $1 \times 1$ $mm^2$ photodiode with fingers of 1 µm pitch. The generated voltage of such on-chip photodiode is in the range [0.27, 0.46] V for an illumination span of 100 lx to 100 Klx, and a harvested power between 3.7 nW and 8.3 µW for the same illumination range. The second chip, fabricated in the same 0.18 µm CMOS technology is shown in Fig. 10(b). It includes the voltage regulation module and is powered by the unregulated output voltage of the first chip, $V_{out,PMU}$. The experimental setup is shown in Fig. 11. A regulated lamp is used to illuminate the system. The illumination level is controlled by modifying the supply voltage of the lamp and the distance to the chip. The TES 1332 digital lux meter was used to measure the illumination level. For the visualization of the signals, a Tektronix MDO4034C oscilloscope was used. In addition, two Keithley SMUs from the 2400 series were used for obtaining the experimental data. The measurement process was automatized using a data acquisition board (DAQ) controlled by NI LabVIEW software.

As shown in [27], the lateral collection of photons by a photodiode might increase the photocurrent. Several photodiode configurations with fingers of different pitch to split our whole $P^+$ over P-well in N-well over P-substrate photodiode of $1 \times 1$ $mm^2$ in several sections have been included on the chip with the PMU to this end. Fig. 12 shows that a separation between fingers of 1 µm leads to the best power efficiency. Thus, this is the configuration used for all measurements below. Fig. 13 conveys the power generated by the photodiode vs its voltage for different light illuminations.

To measure the power efficiency of the whole system, the two chips were connected directly without the off-chip capacitor. The experimental end-to-end efficiency is defined as $\frac{P_{out}}{P_{mpp}}$ where $P_{out}$ is the output power at the target value of $V_{out,reg}$=1.3 V and $P_{mpp}$ is the maximum power generated by the photodiode at a given illumination. To measure $P_{mpp}$ one of the SMUs was connected at the output of an isolated on-chip solar cell identical to the one connected to the PMU and fabricated as a test structure on the same chip due to the impossibility of simultaneously measuring and using the collected energy. The other SMU was connected at the output

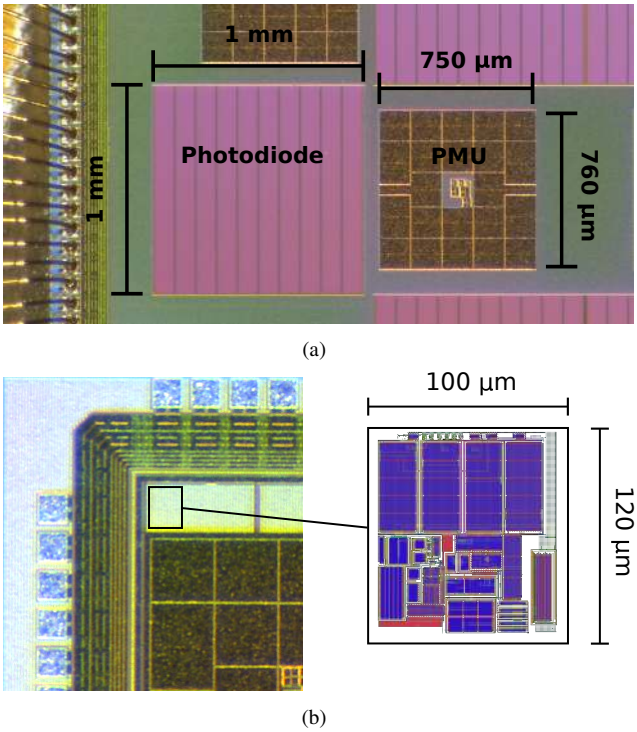


Fig. 10. Microphotograph of the (a) energy harvesting with PMU SoC, and (b) volage regulation module.

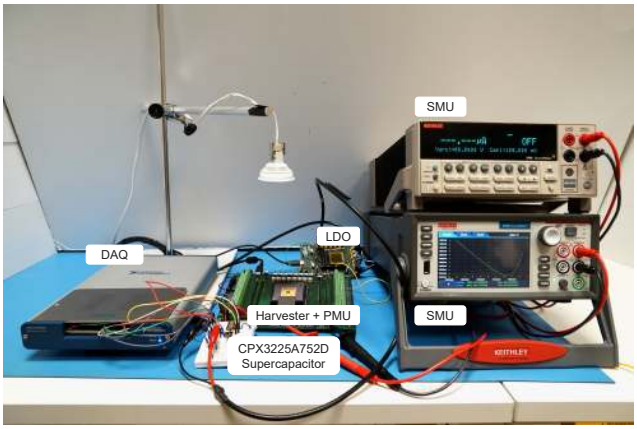


Fig. 11. Experimental setup of the system under test.

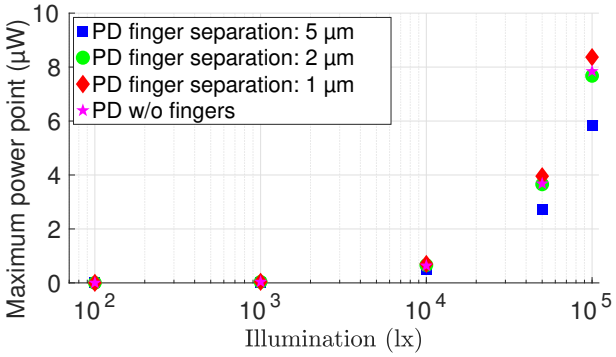


Fig. 12. Measurements of the power generated with different distances between fingers in a photodiode of $1 \times 1$ $mm^2$.

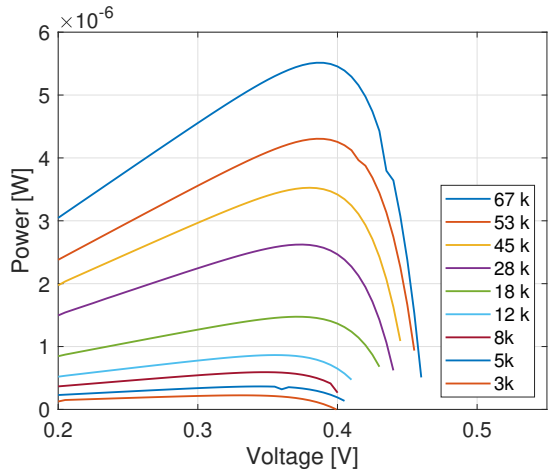


Fig. 13. Power in the photodiode of $1 \times 1$ mm$^2$ vs photodiode voltage for different illumination levels (klx).

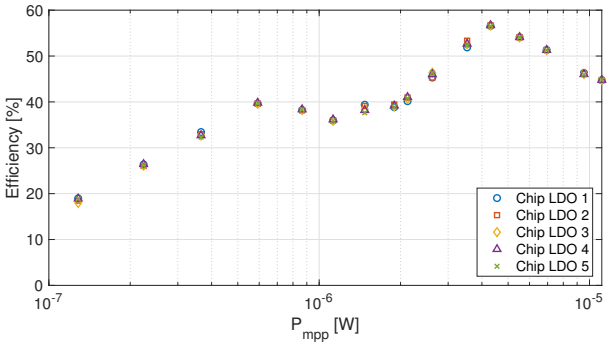


Fig. 14. Experimental end-to-end efficiency as a function of the input power for 5 different samples of the voltage regulation chip for a fixed harvester/PMU SoC.

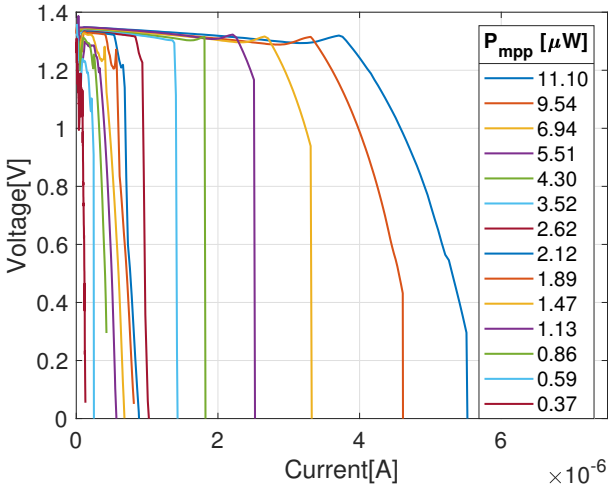


Fig. 15. Measured regulated output voltage as a function of the load current for different illuminations corresponding to different generated input powers at the on-chip solar cell, $P_{mpp}$, without the off-chip storage capacitor.

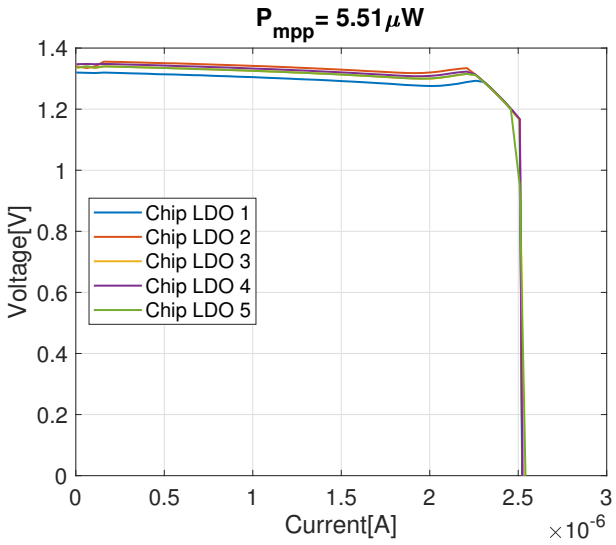


Fig. 16. Measured regulated output voltage as a function of the load current for 5 different samples of the voltage regulation module for a fixed harvester/PMU SoC for an input power of 5.51 $\mu$W and without the off-chip storage capacitor.

of the second chip to measure $P_{out}$. Fig. 14 shows the experimental efficiency of the whole system for 5 different samples of the voltage regulation module for a fixed harvester/PMU SoC. The dispersion among different chips is kept low. The peak efficiency of the system reaches 56.03% at 2.41 $\mu$W of output power. This value remains very close to that of the PMU alone, which was measured as 57% at 2.07 $\mu$W of output power. For low and medium illumination levels the efficiency drops to around 20%-40%. The peaks seen on the efficiency curve were also found on the experimental response of the unregulated system and are attributed to the transition between different working regions of the MPPT approach, [13].

A second set of measurements with the PMU directly connected to the regulation module without an external capacitor was performed in order to assess the range of load currents that can be endured while maintaining the regulated output voltage at $V_{out,reg}$ = 1.3 V. In this case, a variable current drain was connected at the output of the system in order to account for the different load currents. The experimental results are shown in Fig. 15 for different illumination levels corresponding to different generated input powers at the on-chip solar cell, $P_{mpp}$. As expected, the larger the illumination input power, the wider the range of current loads that can be served by the system. With respect to process variations, Fig. 16 shows the experimental results for 5 different samples of the voltage regulation module for a fixed harvester/PMU SoC. The input power considered in this case was 5.51 $\mu$W and, as can be seen, measured process variations are minor.

In order to assess the capacity of the system to act as the power supply of a complete biomedical implantable device we connected as an energy reservoir the CPX3225A752D supercapacitor at the output of the unregulated energy harvesting chip as shown in Fig. 17. This capacitor provides the system with an energy reservoir of $C_{storage}$ = 7.5 mF featuring a low internal impedance of 25 $\Omega$ and a leakage current about 10 nA. A variable resistor is connected at the output of the system to represent changing load currents of different magnitude and

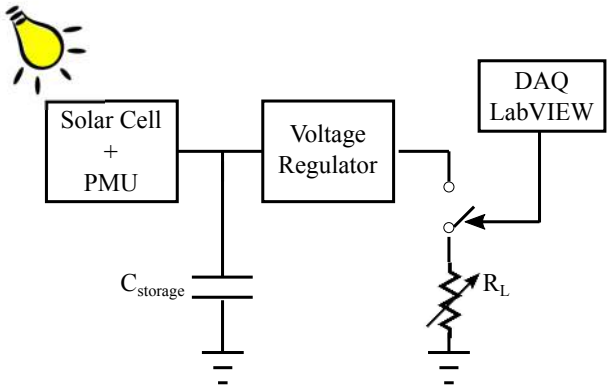


Fig. 17. Configuration of the experimental setup for the measurement of the transient behavior of the complete system under changing load current pulses of different magnitude and duration.

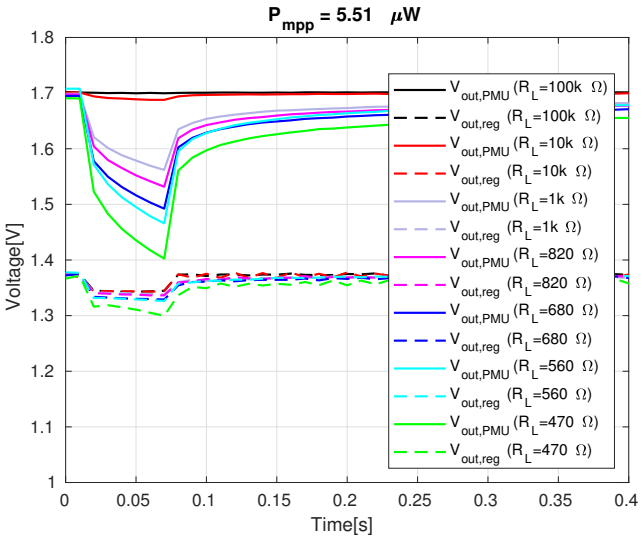


Fig. 18. Experimental dynamic behavior of the whole system when different load currents are applied at time $t$= 20 ms for a duration of 60 ms considering an input power of $P_{mpp}$=5.51 $\mu$W.

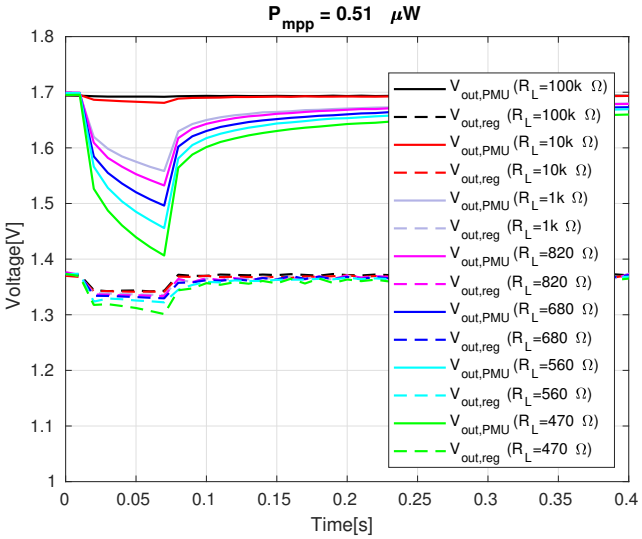


Fig. 19. Experimental dynamic behavior of the whole system when different load currents are applied at time $t$= 20 ms for a duration of 60 ms considering an input power of $P_{mpp}$=0.51 $\mu$W.

duration. This resistor is connected and disconnected from the output to analyze the transient behaviour of the system under different conditions using the commercial switch TS5A23166 ($R_{ON}$ = 0.9 Ω). The control of this switch is implemented with a data acquisition board and LabVIEW. The initial conditions were set to $V_{out,PMU}$ = 1.7 V, that is, the initial voltage at the supercapacitor, $C_{storage}$. A voltage pulse of a duration of 60 ms was applied at time $t$ = 20 ms to connect the voltage regulator to different current loads ranging from 17 $\mu$A to 2.76 mA. To generate these load currents, the value of the load resistor, $R_L$ was varied from $R_L$= 100 kΩ to $R_L$ = 470 Ω, considering an initial value of $V_{out,reg}$ = 1.3 V. Fig.18 shows the measured time response of the whole system for an input power of 5.51 μW. As seen, the system is capable of maintaining the target regulated voltage of 1.3 V at the output of the system up to load current demands of 2.76 mA ($R_L$ = 470 Ω), as in this case the output voltage drops to 1.29 V. Also, the storage capacitor recovers to the initial voltage after a short transit time. The same behavior can be observed for input powers as low as 510 nW, as shown in Fig. 19. To contextualize these numbers, the voltage drop at the storage capacitor, $V_{out,PMU}$ during the pulse duration of 60 ms in Fig. 18 represents a drained charge of approximately 1.5 mC, roughly four orders of magnitude higher than the charge consumed for an average transmit power of 724 $\mu$W assuming a constant voltage of approximately 1 V in [9], which makes it compatible with the BLE standard.

In [13], the minimum input power needed for the PMU alone to be able to start up was experimentally determined to be 2.38 nW. To do so, an SMU was connected to an isolated solar cell identical to the one connected to the PMU and fabricated on the same chip in order to obtain the PV curve. A second SMU was connected to the output of the PMU. It was experimentally determined that the PMU working in WR1 was able to start up from an input power of 2.38 nW charging an external capacitor at a voltage higher than 1.1 V. Following the same procedure, we determined the minimum self-startup input power of the whole system composed of the harvester and the regulator modules. In order to make a fair estimation of this startup power, a minimum load current of 50 nA was considered as representation of the quiescent current corresponding to an implantable device potentially connected to the output of the system. In addition, the off-chip battery of 7.5 mF was replaced by a smaller capacitor of 100 nF in order to speed up the charging process as for these very low illumination levels charging the 7.5 mF would take hours. The results are summarized in Table I, showing the maximum voltage reached by the storage capacitor for different input powers, and their associated rising times. As it can be seen, the minimum input power required is 340 nW.

Table II conveys the performance metrics of our system and a comparison with the state-of-the-art of integrated energy-harvesting systems. As in our case, the work in [6] is the only one that integrates both energy transducer and PMU on the

TABLE I
EXPERIMENTAL DETERMINATION OF THE MINIMUM INPUT POWER FOR SELF-STARTUP OF THE WHOLE SYSTEM WITH LOAD CAPACITOR OF 100 nF

| $P_{mpp}$ (nW) | $V_{out,PMU}$ (V) | Rising Time (s) |
|---|---|---|
| 100 | 0.534 | 5.617 |
| 200 | 0.98 | 6.729 |
| 300 | 1.137 | 2.605 |
| 340 | 1.349 | 6.72 |
| 400 | 1.392 | 3.006 |
| 500 | 1.467 | 2.811 |
| 600 | 1.507 | 1.805 |
| 700 | 1.541 | 1.733 |

same silicon substrate. Nevertheless, this work lacks MPPT and output regulation. The work addressed in [3] aims at implantable devices. It is focussed on the range of nW of input power, and it does not feature MPPT and output voltage regulation. The work in [28] integrates a charge pump and MPPT featuring a very high end-to-end peak energy efficiency at 72%. Their cold start-up, however, needs an input voltage and power consumption around 1 V and 5.9 µW, respectively. Both, the PMU alone and our system with the PMU and the regulator feature cold start-up from 2.38 and 340 nW, respectively. The work in [7] manages an input power range of 20 pW to 1.5 µW without output voltage regulation and cold start-up, and with a peak efficiency of 50% at 8 nW. Finally, the work in [29] is our main contender. This harvester includes the width modulation of the switches in the charge pumps as an extra dimension to change through MPTT. The input power range of [29] is estimated from the data on output power and the end-to-end efficiency provided in the paper. This results in a wide input power range from 160 nW up to above 300,000 nW, with a peak efficiency of 88% for a load of 200,000 nA. The idea of channel width modulation could be incorporated into our design by laying out several switches in parallel in the auxiliary and main charge pumps with their accompanying programming signals, improving our end-to-end efficiency. Also, the minimum cold start-up energy would decrease with PMU and voltage regulator on the same silicon substrate. Finally, more recent approaches for DC energy inputs like the one reported in [30] designed for thermoelectrics include self-start-up from several µA of input current, reaching a high peak efficiency of 84% through external inductors.

## VI. CONCLUSIONS

This work presents experimental results of a low-power energy harvesting system composed of a micro solar cell of 1 $mm^2$ and PMU on the same chip connected to a voltage regulation module to provide a regulated output voltage of 1.3 V. Both chips are implemented in standard 0.18 $\mu$m CMOS technology. The system also contains a supercapacitor of 7.5 mF between the PMU and the regulator. Experimental results show that the fast energy recovery of the PMU allows to replenish the supercapacitor with enough charge as to sustain Bluetooth Low Energy (BLE) communications even with input light powers as low as 510 nW. The whole system is able to self-start-up without external mechanisms at 340 nW. Future work will be focused on laying out PMU and output voltage regulator on the same substrate, as well as on incorporating channel width modulation towards ex-vivo experiments.

## ACKNOWLEDGMENT

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TABLE II
EXPERIMENTAL DATA SUMMARY OF OUR PROOF-OF-CONCEPT CHIP AND STATE-OF-THE-ART

| | [6] | [3] | [28] | [29] | [7] | This Work |
|---|---|---|---|---|---|---|
| **Technology** | standard 0.18 μm CMOS | 0.18 μm CMOS | 0.18 μm CMOS | 65 nm CMOS | 0.18 μm CMOS | standard 0.18 μm CMOS two chips: PMU + regulator |
| **Voltage boosting** | charge pump | boost with voltage doubler | charge pump | charge pump | discontinuous charge pump | charge pump |
| **Transducer + PMU on-chip** | yes | no | no | no | no | yes |
| **Transducer + PMU area ($mm^2$)** | 1.3 + 0.24 | ? + 1.53 | ? + 0.552 | ? + 0.54 | ? + 2.72 + off-chip cap. | PMU: 1 + 0.575 regulator: 0.012 |
| **Input power range (nW)** | - | 1.1 - 6.25 | 5900 - 47000 | 160 - > 330000 | 0.02 - 1500 | PMU alone: 2.38 - >10000 PMU + regulator: 340 - >10000 |
| **Output power range (nW)** | - | 0.544 - 4 | 3840 - 30550 | 100 - 300000 | 0.005 - 600 | PMU alone: 0 - 4500 PMU + regulator: 113-> 10000 |
| **Cold start-up** | yes | no | yes | yes | no | yes |
| **Minimum input power to start-up (nW)** | - | - | - | 100 | - | PMU alone: 2.38 PMU + regulator: 340 |
| **MPPT** | no | no | yes | yes | yes | yes |
| **Output regulation** | no | no | yes | yes | no | yes; on two chips |
| **End-to-end peak efficiency (%) @ $P_{out}$ (μW)** | 67@1.27 | 53@0.0012 | 72@- | 88@- 200 | 50@0.008 | PMU alone: 57@2.07 PMU + regulator: 56.03@2.41 |


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