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Authors
Shakouri, A
Zhang, Y

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On-Chip Solid-State Cooling for Integrated Circuits Using Thin-Film Microrefrigerators

Ali Shakouri and Yan Zhang

***Abstract*—An overview of recent advances in solid-state cooling utilizing thin-film silicon germanium-based microrefrigerators is given. Key parameters affecting micro cooler performance are described. A 3-μm thick 200 $\times$ (3 nm Si/12 nm $Si_{0.75}Ge_{0.25}$) superlattice device can achieve maximum cooling of 4 °C at room temperature, maximum cooling power density of 600 W/cm^2 for 40-μm diameter device and fast transient response on the order of tens of micro-seconds independent of the device size. Three-dimensional electrothermal simulations show that individual microrefrigerators could be used to remove hot spots in silicon chips with minimal increase in the overall power dissipation.**

***Index Terms*—Microrefrigerators, silicon chips, thin-film silicon germanium-based microrefrigerators.**

I. Thermal Issue in Electronics and Optoelectronic Integrated Circuits

CURRENT trends in optoelectronic and microelectronic devices is minimizing the die size while both increasing level of integration and driving clock speeds to higher frequencies. This results in higher power dissipation and an increase in the die temperature. The failure rate due to electromigration and oxide breakdown is exponentially dependent on temperature. Thus, thermal management plays a vital role in integrated circuit (IC) design. According to chip manufacturer predictions, within the next five to ten years, the power requirements of the IC chips are going to exceed current cooling techniques [1]. This will necessitate computer case temperature to be 20 °C–30 °C lower than current values. Another distinguishing characteristic of IC chips is their uneven temperature distribution, which leads to “hot spots.” The temperature inside a chip can vary by 5 °C $\sim$ 30 °C from one location to another. Peak heat flux at hot spots could be five or six times chip’s average value, 10–50 W/cm^2. [1] Thermal designs are driven by these hot spots instead of the whole chip temperature. In the case of optoelectronic devices, temperature differences between the active region and the heat sink can be hundreds of degrees.

Thermal management solutions can be divided into two groups: passive heat spreading and active cooling. In the former technique, one tries to lower the thermal resistance between active region and the heat sink by increasing the spreading area and using better thermal conductivity interface materials. Techniques such as flipping the laser over and mounting the junction closer to the heat sink have been demonstrated [2]. Better copper or diamond-based heat sinks and thermal interface materials are also being investigated [3]. These techniques lower the junction temperature but they do not keep it at constant value as the ambient temperature is changing. For a typical distributed feedback (DFB) laser, the wavelength shifts with temperature by about 0.2 $\sim$ 0.3 nm/°C. In high performance optoelectronic applications, such as wavelength division multiplexed (WDM) systems, 1 °C or 2 °C temperature change can cause cross-talk between different channels. Thus temperature stabilization is important in many high speed or dense-wavelength-division multiplexed optoelectronic systems. This can only be achieved by using active refrigeration. In addition, an improved heat sink cannot eliminate small hot spots in electronic IC chips on the order of hundreds of microns in size. For such applications microscale refrigerators could be very useful.

Compressor-based refrigerators do not scale well at low dimensions. In addition, there is a fundamental complexity and difficulty in manufacturing such micro-scale components. The cooling capacity scales with the volume of the gas while many loss mechanisms, such as friction and heat loss, scale with the surface area. Since the surface to volume ratio increases as the size shrinks, it is difficult to make efficient micro-scale mechanical-based refrigerators [4].

Another approach to reduce hot spots in IC chips is through optimized cell placement [5]. The temperature gradient inside the chip could be improved by a factor of two, though at the cost of increasing wire length and cell area which limits minimization and may bring more Joule heating inside the chip. Through the statistical methods of power and timing analysis, provided by programs like McPower [6] and mean estimator of density (MED) [7] etc., it is possible to find the nominal on-chip temperature profile. However, this method involves the complex thermal design process at very early layout stage and the optimal thermal design might cause increase of die area, which is very expensive. Thus, developing high cooling power density thin-film refrigerators, which are compatible with the micro-fabrication process, could have a strong impact on IC optimization [8].

II. Conventional Thermoelectric Coolers and Recent Advances in BiTe-Based Thin Films

Bismuth Telluride thermoelectric coolers are commonly used in commercial optoelectronic applications [9], [10]. They provide silent solid-state cooling. They range in size form $1.8 \times 3.4 \times 2.4$ up to $62 \times 62 \times 5.8$ mm^3. Thermoelectric coolers’ main problems are low efficiency, low cooling power density, and bulk fabrication techniques, which are not

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The authors are with the Baskin School of Engineering, University of California, Santa Cruz, CA 95064 USA (e-mail: ali@soe.ucsc.edu).

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compatible with integrated circuit manufacturing. The existing thermoelectric modules cannot easily remove the on-chip hot spots because of their large size. Thus, an alternative localized cooling solution is highly desirable.

Conventional thermoelectric (TE) coolers are based on the Peltier effect at the metal/semiconductor junction [5]. The Peltier effect is a reverse of the Seebeck effect. When the current flows from material (a) into material (b) and then back to material (a), it heats the first junction and cools the second one (or vice versa). Thus, heat is transferred from one junction to the other. The microscopic picture is as follows: when electrons flow from a material in which they have an average transport energy that is lower than the Fermi energy, to another material in which their average transport energy is higher, they absorb thermal energy from the lattice, and this will cool the junction between the two materials.

A typical thermoelectric cooler is shown in Fig. 1. It is composed of a series of n- and p-type semiconductor elements. Multiple elements are used to lower the operating current of TE modules. In a practical cooling application, for example, removing 10 W heat from a surface area of 1 cm^2, a single p-type or n-type element would require several amps of current and dozens of millivolts of voltage. This causes problems with the required power supplies, but more importantly, at such high currents Joule heating in the wires and electrical contacts could reduce the maximum cooling and efficiency significantly. In order to decrease the current for the same cooling capacity, one can put many thermoelectric elements electrically in series and thermally in parallel. Instead of a single element with a cross section s, one uses N elements with cross sections s/N, this reduces the current to I/N and increases the voltage to $N \times V$. In order to put multiple elements electrically in series and thermally in parallel, both n- and p-type semiconductors are required. When the current is flowing from n to p (i.e., electrons moving from the p-branch to the metallic contact and from that to the n-branch), the heat is absorbed at the junctions p-semiconductor/metal and metal/n-semiconductor. All these junctions are attached to a top plate, which forms the cool surface of the module.

For current commercial TE modules, the maximum cooling around room temperature is about 70 °C, however the cooling power density is low, on the order of 5–10 $\mathrm{W/cm^2}$. The worse situation is when the heat is transferred to the bottom surface. The amount of heat generation at the hot side could be double or triple the amount of heat removed from the cold side due to the low coefficient-of-performance in commercially available modules ($\sim 6\% - 8\%$ of Carnot efficiency), [4], [5]. The micro-scale optoelectronic devices can generate 100–1000 $\mathrm{W/cm^2}$ heating, which is far beyond the capability of current TE module. The maximum cooling power density of a TE module is inversely proportional to the length of its elements (distance between hot and cold junctions). However it is a challenge to manufacture thermoelectric elements with lengths smaller than 200–300 μm. Non-ideal effects such as metal-semiconductor contact resistance inside the TE module and the finite thermal resistance of the heat sink start to dominate as the TE module is miniaturized. Some ultra-thin TE modules are available commercially [11]. They can reach a cooling power density on the order of 50–100 $\mathrm{W/cm^2}$.

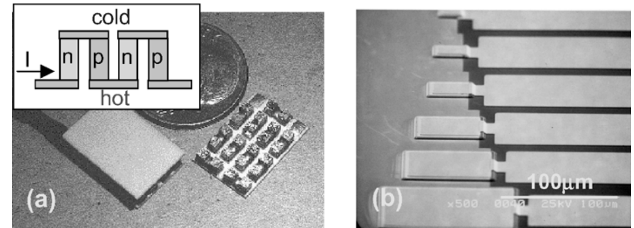

Fig. 1. (a) Conventional bulk BiTe thermoelectric module and (b) thin-film superlattice SiGe/Si heterostructure integrated thermionic cooler fabricated using batch integrated circuit fabrication techniques.

During the last couple of years, there have been significant advances in thin-film BiTe-based thermoelectric coolers which have demonstrated at research laboratories. R. Venkatasubramanian *et al.* at Research Triangle Institute in North Carolina have demonstrated 3–5 μm thick, 100 μm diameter BiTe/PbTe superlattice coolers with maximum cooling of $\sim 30\,^{\circ}\mathrm{C}$ and maximum cooling power density $> 500\ \mathrm{W/cm^2}$ (this is an estimated value and not directly measured) [12]. These values have been achieved with the use of electron transmitting, phonon blocking superlattices and ultra low metal/semiconductor contact resistance. Böttner *et al.* at the Fraunhaufer Institute in Germany have been working on monolithic integration of conventional BiTe and BiSbTe bulk material on silicon substrate [13]. They have been able to deposit 20-μm thick legs using sputtering and integrated circuit fabrication techniques to produce coolers on large scale (on 4-in silicon wafers). They have demonstrated maximum cooling of $\sim 12\,^{\circ}\mathrm{C}$ with a 3 p- and n-leg at a current of ~ 1 A. The estimated maximum cooling power density is $\sim 100\ \mathrm{W/cm^2}$. Strategies have been recently developed for improving the coefficient-of-performance (COP) of thermoelectric coolers such as the use of quantum confinement [14]–[16] or skutterudite materials [17], [18].

III. Heterostructure Integrated Thin Film Coolers

One attractive solution for microscale temperature control is to monolithically integrate thin-film thermoelectric coolers with active optoelectronic devices. In a collaboration between UCSC, UCSB, and HRL Laboratories, we have been working on the use of thermionic emission in hetereostructures in order to improve the cooling performance of conventional semiconductors used in microelectronics and optoelectronics [19]–[22]. In the thermionic emission process, hot electrons from a cathode layer that is selectively emitted over a barrier to the anode junction. This causes evaporative cooling of the cathode layer and can improve the effective Seebeck coefficient of the barrier material. Short period superlattices can also reduce lattice thermal conductivity and thus improve the efficiency of thermoelectric energy conversion. We have fabricated and characterized InGaAsP/InP, InGaAs/InAlAs, SiGe/Si, SiGeC/Si heterostructure-integrated thermionic (HIT) micro-refrigerators. Different superlattice periods, doping and thicknesses (1–5 μm), and various device sizes (ranging from 100 μm^2 to 40 000 μm^2) have been characterized.

As a specific example we show the results for a superlattice samples which was grown with a molecular beam epitaxy

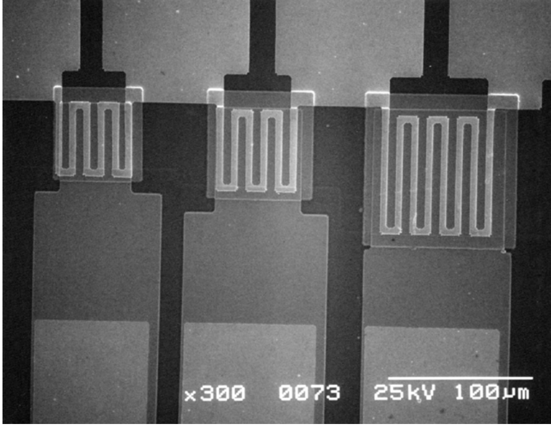

Fig. 2. Scanning electron microscopy (SEM) picture of SiGe/Si microrefrigerators integrated with thin-film heaters/sensors.

(MBE) machine on five inch diameter (001)-oriented Si substrates, doped to $0.001 \sim 0.006$ Ω-cm with Boron. The structure of the microrefrigerator consisted of a 3-μm thick $200 \times$ (3 nm Si/12 nm $Si_{0.75}Ge_{0.25}$) superlattice grown symmetrically strained on a $Si_{0.8}Ge_{0.2}$ buffer layer on top of Si substrate. The doping level is 5×10^{19} cm^{-3} for the superlattice.

Fig. 2 shows a SEM picture of the mirorefrigerators integrated with a layer of thin-film metallic wires. For convenient measurements of cooling, power density, and transient response, we integrated a thin layer of metal wire on top of the micro-refrigerators. The integrated wire could work both as a sensor for temperature measurements and a heat supply on top of the device. Fig. 3 shows the measured cooling on micro-refrigerator with different device sizes. From this graph we see that the 60×60 μm^2 device has highest cooling. The optimized device size depends on inherent nonideal effects in the device: Joule heating generated by the substrate and the heat flow back from the heat sink. As demonstrated by the simplified 1D thermoelectric model, $Q = STI - (1/2)I^2R - (\Delta T/R_{\rm th})$, ($Q$, cooling power, which equals to cooling power density (CPD) times device area (A), S, Seebeck coefficient, T, ambient temperature, I, current supplied to the device, R, electrical resistance of the thermoelectric element, $R_{\rm th}$, its thermal resistance, and ΔT, temperature difference.) Thus, $\Delta T = (CPD * A + (1/2)I^2R - STI) * R_{\rm th}$, $R_{\rm th}$ and $R_{\rm e}$ are proportional to $A^{1/2}$ due to three-dimensional heat and current spreading in the substrate. In addition, contact resistance scales with area and side contact resistance scales with root mean square of area. Similarly, superlattice and substrate electrical/thermal resistance also have different area dependence. Combine all these non-ideal factors. There always has to be an optimized device size for each material and structure composition to achieve the maximum cooling. Theoretical simulations in [26] have shown that there is an optimum device size of $50 \times 50 \sim 60 \times 60$ μm^2 which gives maximum cooling. This matches the observed experimental results in Fig. 3. Fig. 4 shows the maximum cooling versus applied heat load density on top of microrefrigerator. Using this data, the maximum cooling power density can be deduced. During experiments, a constant current was supplied to the heater, and the cooling of microrefrigerators was measured by a thermocouple. By increasing the current to the heater, more

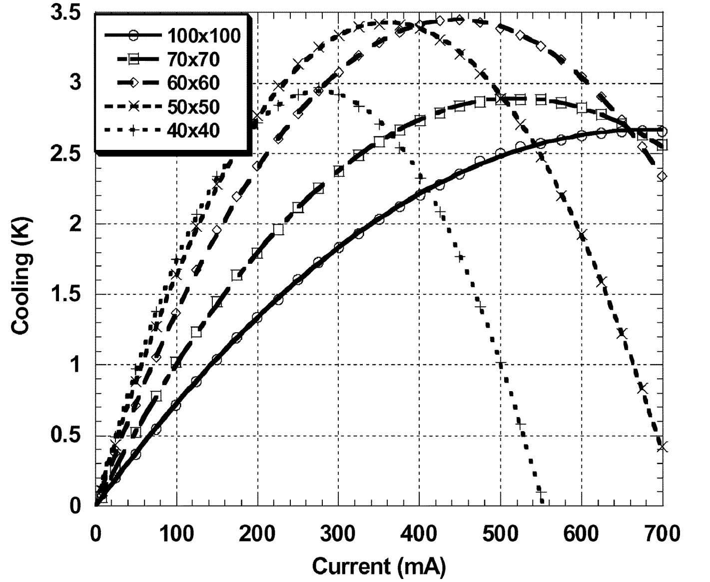

Fig. 3. Cooling temperature versus supplied current is measured by a micro-thermocouple on top of 40×40 μm^2, 50×50 μm^2, 60×60 μm^2, 70×70 μm^2, 100×100 μm^2 area micro coolers.

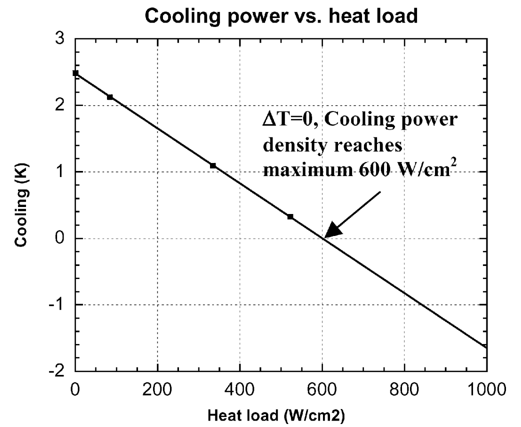

Fig. 4. Maximum cooling temperature versus heat load for a typical SiGe microrefrigerator (size: 40×40 μm^2). By definition, at maximum cooling power density, cooling temperature is zero. Since there is a linear relationship, if heat load power density is, e.g., a factor of two smaller than the maximum value (300 W/cm^2), cooling by a factor of two smaller than the maximum value (1.2 C) can be achieved at the same time.

heat load was added on top of the refrigerators. The maximum cooling power is defined as the heat load power that makes the device's maximum cooling temperature equal to zero.

When comparing these thin-film integrated SiGe/Si micro-refrigerators with bulk thermoelectronic modules, there are mainly three advantages. First of all, very small size and standard thin-film fabrication method makes these micro-refrigerators suitable for monolithic integration inside IC chips. It is possible to put the refrigerator near active devices and cool the hot spots directly. Second, the high cooling power density is one of the main advantages compared to commercial bulk TE refrigerators. Third, the transient response of the current SiGe/Si superlattice refrigerators is several orders of magnitude better than the bulk TE refrigerators. The standard commercial TE refrigerator has a response on the order of tens of seconds. Fig. 5 shows the fitted transient response of the thermoelectric

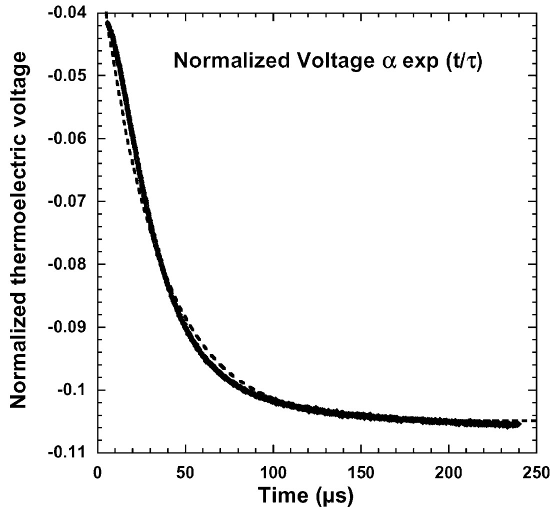

Fig. 5. Fitted transient response of SiGe/Si superlattice microrefrigerator.

voltage for a typical SiGe/Si microrefrigerator. This thermoelectric voltage is generated according to the Seebeck effect due to the temperature difference across microrefrigerator. The temperature difference was established by supplying ac current (1-kHZ square wave) to the thin-film heaters. The generated Joule heating on the top surface of the device establishes a temperature difference across superlattice and substrate which results in a thermoelectric voltage. When the heating is turned on and off, the rise/fall time of this thermoelectric voltage is on the same order as the transient response of the active microrefrigerator. Since the heating and cooling is across the same thin-film device. Fig. 5 illustrates the transient response of a typical SiGe/Si superlattice sample $\sim 34\ \mu S$, which is an order of 10^5 times faster than bulk TE refrigerators. In fact, the actual transient response of the device is faster than this measured value. Direct measurement of temperature using optical thermoreflectance technique gives a transient response of $\sim 20\ \mu S$ [23]. The transient response measured by the heater sensor method is limited by the thermal mass of metal lines.

According to the theoretical simulation, the current limitation of the superlattice coolers still lies in the contact resistance between the metal and cap/buffer layer, which is on the order of $10^{-6}\ \Omega\text{cm}^2$. Detailed modeling predicts that 20–30 °C of cooling with a cooling power density exceeding several thousands of W/cm^2 is possible with the optimized SiGe superlattice structures. [24]–[26] Future research interests will also focus on integrating microrefrigerators with electronic and optoelectronic devices.

IV. Application of Microrefrigerator

To demonstrate microrefrigerators' effectiveness to remove hotspots in an integrated circuit, we use the three-dimensional (3-D) electrothermal model to calculate the temperature profile on top of a silicon die with and without microrefrigerator. In the model, we integrate two 3 μm-thick superlattice microrefrigerator ($70 \times 70\ \mu\text{m}^2$) with the silicon chip (1 cm$\times$1 cm$\times$750 μm), one on the corner (50 μm away from edge), and the other on the center. On top of microrefrigerators, we place the same size hot spots, which simulate the high-power operating transistors.

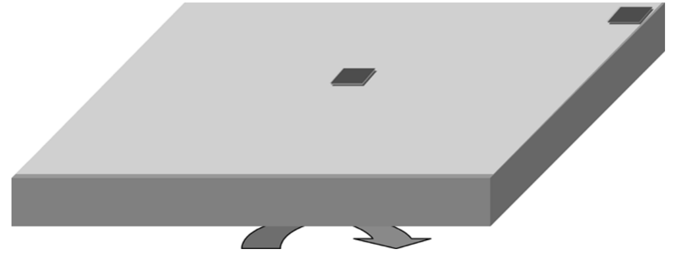

Fig. 6. Illustration of the model configuration. Uniform heat flux of 10 W/cm^2 is applied to the top surface of the silicon chip. Two hot spots of 70×70-μm square exist at the center and at the corner of the chip (heat flux $=$ 300 W/cm^2). SiGe-based microrefrigerators are used to selectively remove hot spots.

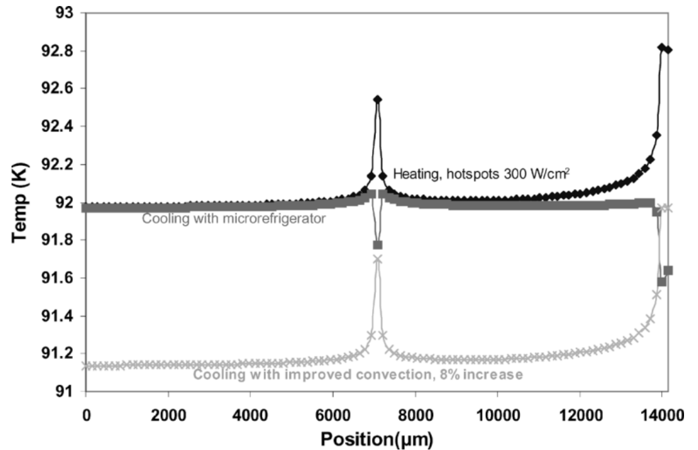

Fig. 7. Diagonal temperature profiles on the top surface of the silicon chip.

In this simulation, we assume the background die heating of 10 W/cm^2 and two hotspots (one center and one corner) with heating power of 300 W/cm^2, as illustrated in Fig. 6. The die operates at 80 °C with a convection coefficient of 0.88 $\text{W/cm}^2\text{K}$ at the back of the silicon substrate. When there is no microrefrigerator, the whole die heats up to $\sim 92\,^\circ\text{C}$ and the hotspots heat up to 92.6 °C at the center and 92.8 °C at edge. When we integrated the microrefrigerator at the hotspots and supplied with the optimized current 0.4 A, the hotspots cools down to 91.6 °C, which is 0.4 °C below the die temperature. The microrefrigerators remove hotspots with negligible temperature increase in the whole chip. This is illustrated in the diagonal temperature plot on the top surface of the die in Fig. 7. One should note that Joule heating in the substrate due to the current flow to the refrigerators is taken into account in these simulations. Alternatively, if we improve the convection condition to achieve similar results as microrefrigerator on hotspots, the convection coefficient has to be increased by 8%. Of course, using better convection condition or better heat sink makes the whole chip temperature drops down 0.9 °C, however, this has the penalty that requires significant additional power dissipation in the heat sink. Thus microrefrigerator will be an efficient way to remove hotspots. In the above simulation, the power consumed by each microrefrigerators is 23 mW, which is very minimal compared to the 10 W total heating on the chip. Considering the 15 mW heating power that each refrigerator removes from the hotspots, we estimate the coefficient-of-performance (COP) of this mircrorefrigerator to be ~ 0.7.

V. Conclusion

We discussed different approaches to solve the heating problems for microelectronics and optoelectronics. An overview of on-chip solid-state cooling utilizing thin-film silicon germanium microrefrigerators has been given. Recent advances in thin-film Si/SiGe superlattice micro-refrigerators allow localized temperature control with large cooling power density $\sim$ 600 W/cm^2. Meanwhile, these devices also demonstrated fast response on the order of 20–40 μs. As demonstrated in the application example, this will be suitable for on-chip temperature control to remove hot spots.

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Ali Shakouri received the M.S. degree from Ecole Nationale Superieure des Telecommunications de Paris, Paris, France, in 1990 and the Ph.D. degree from the California Institute of Technology, Pasadena, in 1995.

He is an Associate Professor of electrical engineering at the University of California, Santa Cruz. His current research is on nanoscale heat and current transport in semiconductor devices, submicron thermal imaging, micro refrigerators on a chip, and novel optoelectronic integrated circuits. He is the Director of the Thermionic Energy Conversion Center (a multi-university research initiative aiming to improve direct thermal to electric energy conversion technologies).

Dr. Shakouri received the Packard Fellowship in 1999 and the NSF Career Award in 2000.

Yan Zhang received the B.S. degree from Shanghai University, Shanghai, China, in 1997, the M.Sc degree from the National University of Singapore, Singapore, in 2000, and is currently pursuing the Ph.D. degree in the Electrical Engineering Department, University of California, Santa Cruz.

Her current research is on nano-scale heat and current transport in semiconductor devices, utilizing microrefrigerator for on-chip cooling solution and electrothermal energy conversion.