On-Chip Time Measurement Architecture with Femtosecond Timing Resolution

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Abstract

This paper presents a new on-chip time measurement architecture which is based on the Time-to-Digital Conversion (TDC) method that is capable of achieving a timing resolution of tens of femtoseconds without the use of external automatic test equipment (ATE). This is the highest temporal resolution that has been reported to-date and is achieved by the use of the homodyne technique. The proposed architecture has been designed using a 0.12μm CMOS process and simulation results based on foundry transistor models indicates that it is possible to achieve a timing resolution of 40 fs. The time measurement architecture is standalone and occupies a small silicon area, 150μm by 180μm, making it attractive for high resolution on-chip time measurement.

1. Introduction

High speed communications has been one of the key driving forces of the electronics industry. The ITRS'05 [1] predicts that on-chip clock speeds will increase into the tens of Gigahertz range which will require time measurement architectures with timing resolutions of tens of femtoseconds. Currently, timing characteristics of VLSI devices are performed using automatic test equipment (ATE). Such testers are able of achieving accurate timing measurements, however they are expensive. Furthermore, the increased integration and performance of VLSI devices due to technology scaling has produced limitations in traditional timing performance test methods. For example, bandwidth and additional timing skew brought about by the increase of electrical distance between the tester and DUT [2]. A solution to address these problems involves placing a single high resolution time measurement architecture directly onto the same device being tested [3]. The use of on-chip time-to-digital converters (TDC) is the most effective method for achieving high resolution required for measuring high speed timing parameters. Current techniques for implementing on-chip time-to-digital converters (TDC) have already been proposed. For example, the counter based technique [4], the vernier oscillator [5], time-to-voltage converter techniques [6, 7], Pulse Shrinking [8] and flash based TDC techniques [2]. Table.1 gives a summary of the timing resolution achieved using the various TDC techniques reported to-date. As can be seen, higher timing resolution is achieved with the application of the vernier and flash based TDC techniques as apposed to counter based, pulse shrinking and time-to-voltage techniques. Although the resolutions of the above techniques will undoubtedly increase with technology, this may come at a cost.

Table 1. Recent work on Time-Measurement

Time Measurement Architecture	Resolution
Vernier delay line [9]	5ps
Flash [2]	5ps
Time-to-Voltage Conversion [6]	14ps
Vernier Oscillator [5]	18.5ps
Interpolator [10]	30ps
Pulse Shrinking [8]	57.3ps
Programmable Time-to-Voltage Conversion [7]	103ps

Two recent attempts at increasing the temporal resolution of time measurement architectures have been proposed by incorporating time amplifiers that precede the TDC in order to improve the overall timing resolution [11, 12]. This is achieved by amplifying the time interval into a timing range that the TDC is able to process. However, these techniques are not capable of achieving the required timing resolution since they only provide resolution of hundreds of femtoseconds.

This paper proposes a new architecture capable of producing tens of femtosecond timing resolution and is organised as follows. In section 2, we introduce the principles of the Homodyne technique for time measurement applications and also describe the proposed time measurement architecture. Section 3 describes the importance of analogue-to-digital conversion (ADC) in time measurement architectures and describes the implementation of the ΔΣ ADC. Section 4 shows simulation results using SPECTRE models for a 0.12μm CMOS process and finally in section 5 conclusions are given.

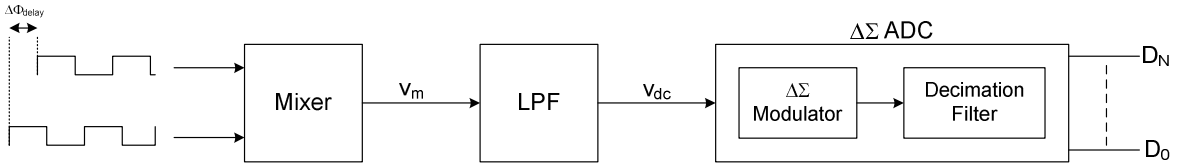

Figure 1: Proposed Time Measurement Architecture

2. Homodyne Technique for Time Measurement

The Homodyne technique was originally developed for RF oscillators [13]. This paper investigates this technique for producing high resolution on-chip time measurements and proposes a new fully integrated on-chip time measurement architecture (Fig 1) that is based on time-to-digital conversion method. The architecture is composed of three main components: an analogue mixer, a filter and an analogue-to-digital converter (ADC). The homodyne technique converts a phase difference into a dc voltage (V_{dc}) by modulating the input with a reference phase signal. A low pass filter is coupled to the output of the mixer to produce a dc voltage that is a function of the phase difference ($\Delta\Phi_{delay}$). The modulation is achieved by the use of an analogue mixer, followed by a low pass filter. For example, if two sinusoidal signals with the same amplitude, A and frequency, ω, have different phases, ϕ_1 and ϕ_2, respectively, then the output of the mixer can be expressed as

$$V_m(t) = A^2 \cos(\omega t + \phi_1)\cos(\omega t + \phi_2) \qquad (1)$$

and

$$V_m(t) = \frac{A^2}{2}\left(\cos(\phi_1 - \phi_2) + \cos(2\omega t + \phi_1 + \phi_2)\right) \qquad (2)$$

The low pass filter is used to remove the 2ω term, leaving only the dc term which is proportional to the cosine of the phase difference multiplied by a constant.

$$V_{dc}(t) = \frac{A^2}{2}\left(\cos(\phi_1 - \phi_2)\right) \qquad (3)$$

To achieve high timing resolution the mixer circuit design needs to meet some conflicting requirements including, speed and area. Such requirements can be met using the cascode mixer circuit [14] in Figure 2. Transistors M3 and M4 form a constant current source. Two input Vin1 and Vin2 are applied to the gates of transistors M1 and M2 respectively and the output of the mixer is taken from the drains of transistors M2 and M4. The transistor sizing was chosen to achieve the required bias currents of 10μA and appropriate driving capabilities to the filter. The cascode mixer has the additional advantage of operating with low supply voltages needed for the 1.2μm technology used for implementation. For the design of the Low Pass Filter (LPF) of the proposed architecture, a switched-capacitor bi-quad with a cut-off frequency of 100 KHz was used [15].

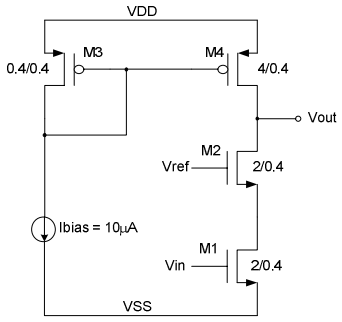

Figure 2: Cascode Mixer

3 Analogue-to-Digital Conversion

The purpose of the ADC is to convert the dc voltage from the output of the filter to a digital output code. The key to achieving femtosecond resolution using the proposed architecture is the implementation of a high resolution ADC. For this reason, the Delta-Sigma (ΔΣ) ADC was selected as opposed to Nyquist rate ADCs because of its high resolution capabilities, area requirements and also the accuracy of the converter does not depend on precise component matching, precise sample-and-hold circuitry or trimming, like Nyquist converters such as Successive Approximation and Dual Slope ADCs [16].

Delta Sigma (ΔΣ) ADC

The ΔΣ ADC depicted in Figure 1 consists of a ΔΣ modulator and a decimation filter. There exists

numerous ΔΣ ADC architecture [17] and the choice usually involves trade-offs between resolution, circuit complexity and stability. Through extensive simulations, we have found that a 1st-order ΔΣ ADC with an oversampling ratio (OSR) of 32 is sufficient to achieve femtosecond resolution avoiding stability and complexity issues often associated with higher order converters. A block diagram of the 1st-order ΔΣ modulator is shown in Figure 3. It consists of an integrator and a single bit quantizer.

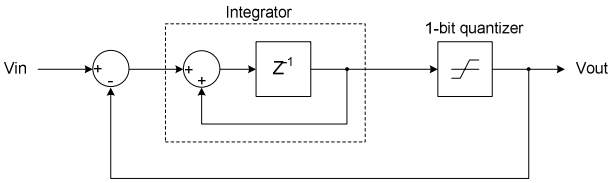

Figure 3: Block diagram of the 1st Order ΔΣ Modulator

The oversampling ratio (OSR) of the modulator is given by the following equation

$$OSR = \frac{f_s}{2f_B} \tag{4}$$

Where f_s is the sampling frequency and f_B is the input signal bandwidth. For this application the OSR is set to 32, in order to provide to appropriating noise shaping required to achieve the high resolution time measurement. The ΔΣ modulator is based on a switched-capacitor implementation and is shown in Figure 4.

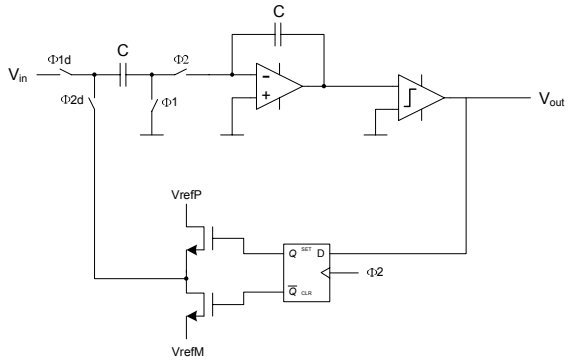

Figure 4: 1st order switched-capacitor ΔΣ modulator

The ΔΣ modulator operates on a two phase clocking scheme, where both normal and delayed versions of the clock are generated to avoid signal dependant charge injection. The two phase clock generator is shown in Figure 5 and the clocking scheme is shown in Figure 6.

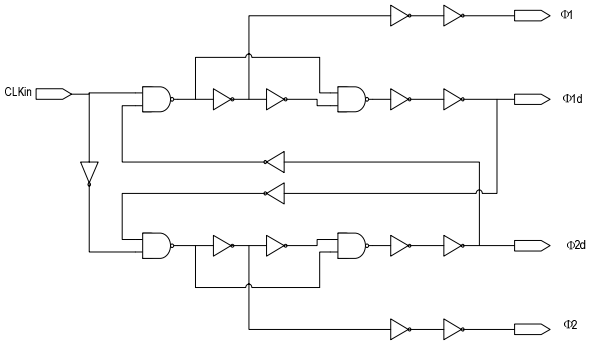

Figure 5: Non-overlapping clock generator

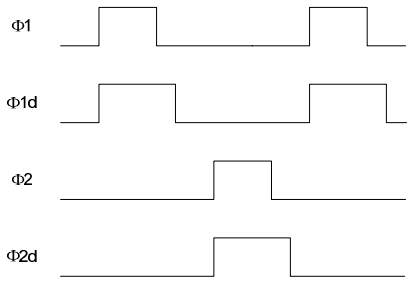

Figure 6: Non-overlapped clock timing

Amplifier Design

The amplifier employed in the integrator is a critical element within the ΔΣ modulator (Fig. 4). Any integrator leakage resulting from the finite dc gain of the amplifier will reduce the modulator attenuation of the quantization noise at low frequencies. Although the modulator can tolerate non-ideal components, the required dc gain of the amplifier is chosen slightly higher than the oversampling ratio. Figure 7 shows the amplifier employed in the modulator. It is based on the folded cascode operational amplifier and has a class AB output stage so that the output can swing close to the supply voltages. The bias circuitry is not shown for clarity. The transistor sizes in the amplifier have been designed to achieve a DC gain of 60dB.

Comparator

The comparator used for the single bit quantizer within the ΔΣ modulator (Fig 4) is shown in Figure 8. The input of the comparator consists of a rail-to-rail input stage that contains two complementary differential pairs in parallel. When one of the common mode (CM) inputs is close to VDD, differential pair M1 and M2 is active. When the CM input is close to VSS, differential

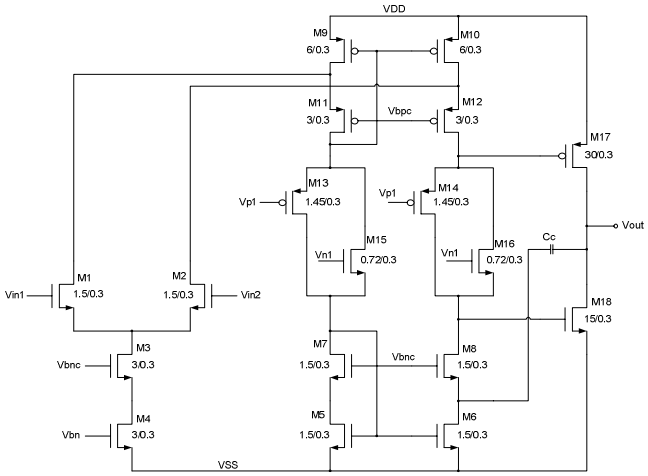

Figure 7: Folded cascode operational amplifier.

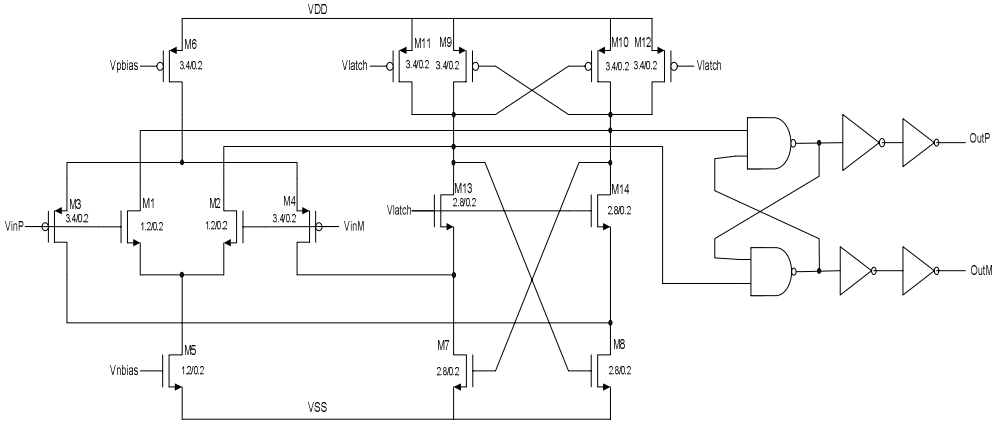

Figure 8: Comparator

pair M3 and M4 is active. *Vpbias* and *Vnbias* are the bias voltages for the tail currents of the two differential pairs which is supplied by a bias circuit; this is not shown for simplicity. The operation of the comparator is as follows. When *Vlatch* is low, the comparator is in a reset state and transistors M11 and M12 couple the drains of transistors M9 and M10 to VDD. Transistors M13 and M14 are off and there is no supply current flowing. When *Vlatch* is high, transistors M11 and M12 are open. The cross coupled regenerative inverters amplify the voltage difference and one of the output nodes is at VDD and the other is at VSS. Figure 9 shows the comparator simulation results. The comparator is clocked at 2.5GHz as shown by the first plot. A 500 MHz clock signal is applied to the positive input (VinP) and the negative input (VinM) of the comparator is varied from 1.08V (90% of VDD), 0.6V with ±1mV offset and 120mV (10% of VDD). The propagation delay of the comparator (measured from

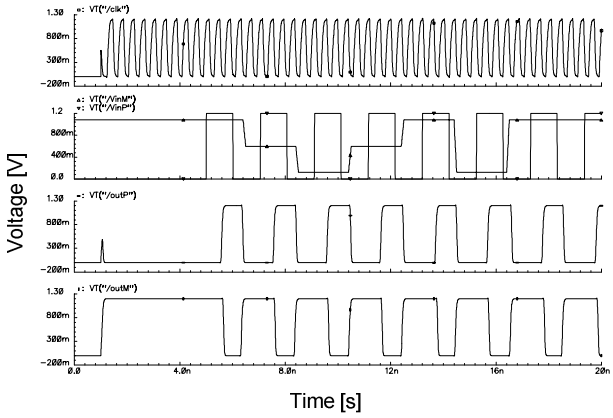

Figure 9: Comparator Simulations

the 50% of the clock signal to 50% of the low to high transition) of 200ps is achieved with loading of 50fF.

Decimation Filter

The Decimation filter of the ΔΣ ADC that follows the ΔΣ modulator is shown in Figure 10[17]. The filter performs both digital filtering and down-sampling of the single bit input data stream form the modulator. The architecture of the decimation filter consists of a counter, a clock divider and a register, making it suitable for time measurement architectures as it is small and easy to integrate. The divide-by ratio of the clock divider is set equal to the oversampling ratio (OSR) of the ΔΣ modulator, in this case the OSR is set to 32.

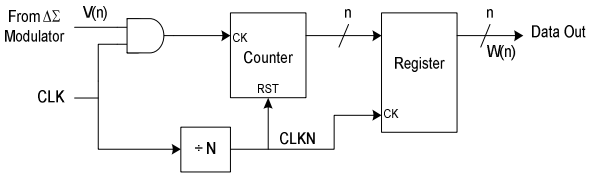

Figure 10: Decimation Filter

4. Simulation Results

In order to verify the performance of the proposed timing measurement architecture based on the time-to-digital conversion method using the homodyne technique, the circuit level designs, considered in section 3, were implemented using a 0.12µm CMOS process. Using the SPECTRE simulator together with foundry transistor models, Figure 11 shows the output of the low pass filter of the proposed architecture when the input phase delay of two clock signals running at a frequency of 1 GHz was varied from 0 to 500fs. As it can be seen, there a linear relationship between the voltage output and the phase difference of the input as expected.

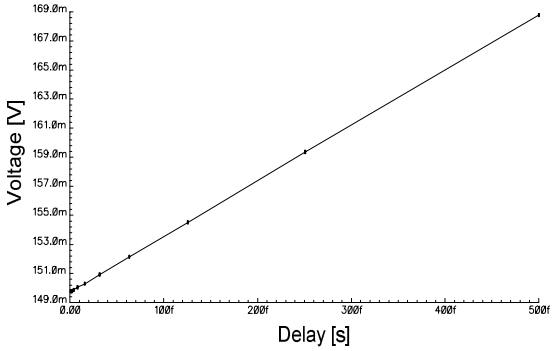

Figure 11: Simulated relationship between timing resolution and the output of the LPF.

To further demonstrate the correct operation of the proposed time measurement architecture, Figure 12 shows a simulation of two clock inputs (Clock_in and Clock_ref) with a phase difference (ΔΦ) of 40fs (top plots), the mixer and filter outputs are shown in the third and forth plot, respectively and the output from the ΔΣ modulator is shown in the fifth plot.

To give insight into silicon area, careful layout techniques, such as common centroid layout of critical transistors (e.g. input transistors of opamp and comparator circuits) and separated analogue and digital layouts were used to reduce offsets and switching noise that would affect the overall performance of the time measurement architecture. The measurement core occupies a silicon area of 150µm by 180µm, making it attractive for high resolution on-chip time measurement.

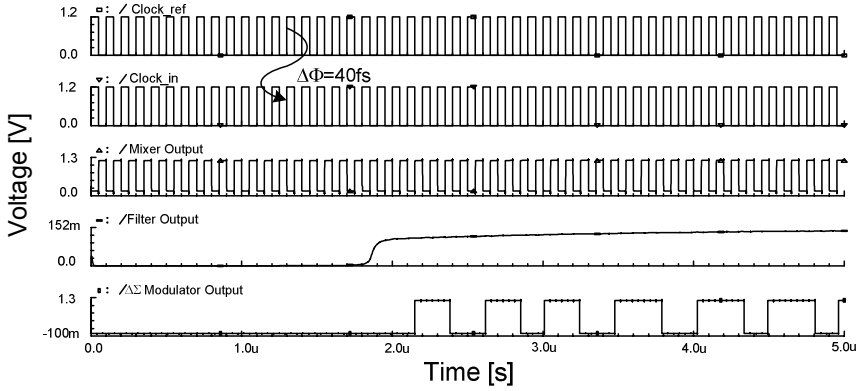

Figure 12: Input and output waveforms of the proposed architecture.

5. Conclusions

This paper has investigated the capability of the Homodyne technique, which was originally developed for RF oscillators, for producing high resolution time measurements. We have proposed a new on-chip time measurement architecture based on the TDC method using the homodyne technique. It has been shown that such a technique is effective in achieving high resolution of tens of femtoseconds which is need for high performance VLSI devices operating with clock frequencies of tens of Gigahertz. This has been made possible through appropriate sections of mixer, filter and data conversion techniques. Simulations using SPECTRE models based on the 0.12µm CMOS process show that measurements are capable with a resolution of 40fs which is the highest reported to-date.

Acknowledgement

This work is supported in part by the EPSRC, U.K., under grant GR/S95770.

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