On Continuous-Time Incremental ΣΔ ADCs With Extended Range

Julian Garcia, *Student Member, IEEE*, Saul Rodriguez, *Member, IEEE*, and Ana Rusu, *Member, IEEE*

***Abstract*—In this paper, the use of continuous-time implementation in extended-range (ER) incremental sigma-delta analog-to-digital converters is analyzed in order to explore a possible solution to low-power multichannel applications. The operation principle, possible loop filter topologies, and critical issues are considered using a general approach. It is demonstrated that, in order to fully benefit from ER, careful attention has to be paid to the analog–digital transfer function mismatches. A third-order single-bit topology validates the theoretical analysis. Its performance is evaluated while the impact of key circuit nonidealities is quantified through behavioral-level simulations. It is shown that, by applying analog-digital mismatch compensation in the digital domain, it is possible to relax the amplifiers' finite gain–bandwidth product and finite dc gain requirements, thus allowing a power-conscious alternative.**

***Index Terms*—A/D conversion, continuous time (CT), extended range (ER), incremental sigma-delta (ΣΔ) (IΣΔ) analog-to-digital converter (ADC).**

I. Introduction

THE DEMAND for the integration of analog-to-digital converters (ADCs) into low-power multichannel sensor applications, such as neuropotential recording devices [1] and portable laboratory equipment [2], has grown during the last years. The resolution requirements of these applications can vary from approximately 6–8 b up to 14 b, with bandwidths generally from kilohertz to megahertz range. While successive-approximation-register (SAR) ADCs successfully cover resolutions up to approximately 8–10 b, incremental sigma-delta (ΣΔ) (IΣΔ) ADCs are particularly well suited to address requirements of more than 10 b [3]–[6]. Similar to their traditional counterparts, they benefit from a relax matching in the analog components through the use of oversampling–noise-shaping techniques, at the cost of increased digital complexity. However, they differ from traditional ΣΔ ADCs in that they are able to process time multiplexed signals, acting as a high-resolution Nyquist ADC. In particular, high-order single-loop (SL) discrete-time (DT) topologies have been implemented [4]–[6], with the aim of reducing the required number of cycles per conversion N. This allows either to increase the ADC's bandwidth or to reduce the modulator's sampling frequency, which, in turn, reduces the power dissipation. The number of required cycles per conversion has been further reduced with the introduction of high-order extended-range (ER) IΣΔ ADCs, which combines an IΣΔ ADC together with a low-power Nyquist ADC [2]. Up to now, the design of high-order SL ER IΣΔ ADCs has only been focused on DT implementations. In this work, the use of continuous-time (CT) implementation in high-order SL ER IΣΔ ADCs is explored as an alternative approach for low-power multichannel applications. Although a sampling occurs at the output of the multiplexor (MUX) which precedes a multichannel ADC, the advantage in a CT implementation stems from the absence of switches in the loop filter which relaxes the settling and bandwidth requirements of the active blocks, thus leading to a reduction in the power consumption. Moreover, this work analyzes the impact of CT circuit nonidealities and the resulting analog-digital transfer function mismatches, highlighting key aspects so as to fully benefit from the advantages of the ER approach in a CT implementation.

The rest of this paper is organized as follows. Section II introduces the operation of SL CT ERIΣΔ ADCs along with the noise cancellation filter design. The influence of the loop filter topology is investigated in Section III. Section IV presents the qualitative analysis of circuit-level nonidealities and analog-digital transfer function mismatches. The theoretical results are validated, through behavioral-level simulations, by using a third-order single-bit CT ER IΣΔ ADC in Section V. Finally, Section VI concludes this paper.

II. CT ERIΣΔ ADC Operation

IΣΔ ADCs are a subclass of ΣΔ ADCs that run continuously in transient mode and feature, as a consequence, a one-to-one mapping between input and output [7]. This characteristic makes them suitable for multichannel applications. Unlike conventional ΣΔ ADCs, the quantization error of IΣΔ ADCs can be made available at the output of the last integrator by using a specific type of digital filter. A second ADC can then capture this output to further reduce the quantization error and "extend the range" of the IΣΔ ADC. This combination of an IΣΔ ADC plus a second ADC for quantization error refinement forms an ERIΣΔ ADC [7]. Fig. 1 shows a general ER IΣΔ ADC block diagram with the channel MUX and the necessary sample-and-hold (SH) circuits. The MUX, together with the input SH, samples each of the input channels and holds the signal $U(z)$ for a period equal to N/f_S. This signal is then processed by the CT ΣΔ modulator and the noise cancellation

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The authors are with the School of Information and Communication Technology, KTH Royal Institute of Technology, 164 40 Kista, Sweden (e-mail: julianmg@kth.se).

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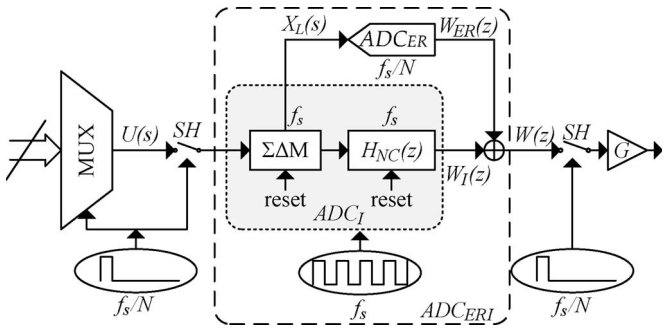

Fig. 1. Multichannel SL ERIΣΔ ADC block diagram.

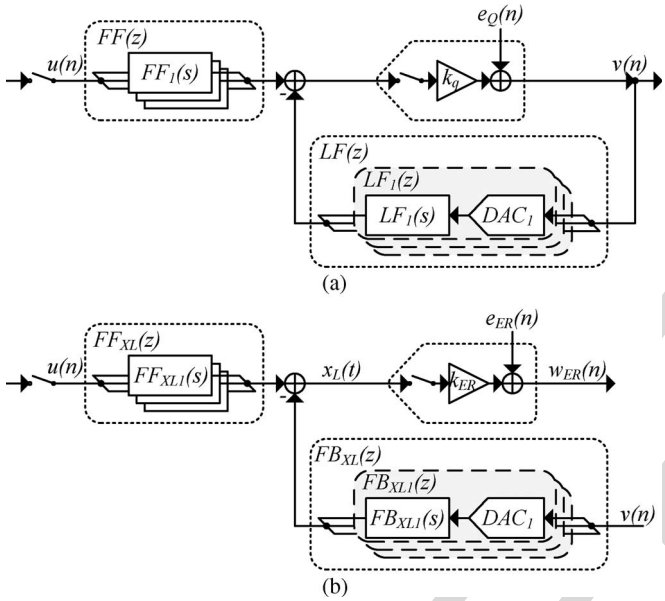

Fig. 2. (a) Linearized block diagram of a CT ΣΔ modulator used in the ERIΣΔ ADC and (b) linearized block diagram to derive the CT-DT equivalent output of the last integrator.

filter $H_{\mathrm{NC}}(z)$, which form the incremental portion of the ADC, i.e., $\mathrm{ADC_I}$, running at a frequency f_S. After N cycles have passed, a valid result from $\mathrm{ADC_I}$ is combined with the output of the ER ADC, i.e., $\mathrm{ADC_{ER}}$, and sampled by the output SH. The ΣΔ modulator, as well as the noise cancellation filter, is then reset and ready to accept the next sample. The block diagram includes also the gain G relating the held analog input U with the valid digital output of the $\mathrm{ADC_{ERI}}$ $w(N)$ at the instants $N \cdot T_S$.

A. DT Transformations

As the quantization error of the IΣΔ ADC should be made available at the output of the last integrator, the output of the modulator and the output of the last integrator are needed to compute $H_{\mathrm{NC}}(z)$ and evaluate the output of the ERIΣΔ ADC. To achieve this, impulse-invariant transformation (IIT) with a normalized sampling rate of one ($T_S = 1$) is used for performing CT to DT (CT–DT) transformations wherever needed.

Fig. 2(a) shows the block diagram for a general low-pass SL CT ΣΔ modulator, where any type of loop filter, quantizer's levels, and digital-to-analog converter (DAC) coding scheme can be considered. Its output $V(z)$ can be expressed as

$$\begin{aligned} V(z) &= U(z)STF(z) + E_Q(z)NTF(z) \\ &= V_U(z) + V_E(z) \end{aligned} \tag{1}$$

where $NTF(z)$ is the CT-DT noise transfer function (NTF) given by

$$NTF(z) = \left.\frac{V(z)}{E_Q(z)}\right|_{U=0} = \frac{1}{1 + k_q LF(z)} \tag{2}$$

where k_q is the quantizer gain and $LF(z)$ is the CT–DT equivalent loop filter given by the sum of the feedback branches. Unlike traditional CT implementations, IIT can be used in IΣΔ ADCs for multichannel applications to calculate the signal transfer function (STF). This is due to the input channel SH which has a similar transfer function as nonreturn-to-zero (NRZ) DACs. Taking this into account, the CT-DT equivalent STF can be expressed as

$$STF(z) = \left.\frac{V(z)}{U(z)}\right|_{E_Q=0} = \frac{k_q FF(z)}{1 + k_q LF(z)} \tag{3}$$

where $FF(z)$ is the CT-DT equivalent feedforward transfer function given by the sum of the feedforward branches. $V(z)$ can also be expressed as a sum of two terms $V_U(z)$ and $V_E(z)$, depending on $U(z)$ and $E_Q(z)$, respectively, and given by

$$V_U(z) = V(z)|_{E_Q=0} = U(z)STF(z) \tag{4}$$

$$V_E(z) = V(z)|_{U=0} = E_Q(z)NTF(z). \tag{5}$$

As shown in Fig. 2(b), the same methodology can be employed to obtain the CT-DT equivalent output of the last integrator $X_L(z)$, which, at sampling times equal to $1/f_S$, is given by

$$\begin{aligned} X_L(z) &= U(z)FF_{X_L}(z) - V(z)FB_{X_L}(z) \\ &= X_{LU}(z) + X_{LE}(z) \end{aligned} \tag{6}$$

where $FF_{X_L}(z)$ is the feedforward CT-DT transfer function, from the input SH to the last integrator output, given by

$$FF_{X_L}(z) = \sum_{i=1}^{k} FF_{X_{Li}}(z) \tag{7}$$

where k is the number of feedforward branches and $FF_{X_{Li}}(z)$ is the CT-DT equivalent transfer function of each individual feedforward branch. Similarly, $FB_{X_L}(z)$ is the feedback CT-DT transfer function, from the feedback DACs to the last integrator output, given by

$$FB_{X_L}(z) = \sum_{i=1}^{k} FB_{X_{Li}}(z) \tag{8}$$

where k is the number of feedback branches and $FB_{X_{Li}}(z)$ is the CT-DT equivalent transfer function of each individual feedback branch. $X_L(z)$ can also be expressed as the sum of the terms $X_{LU}(z)$ and $X_{LE}(z)$ which depend on $U(z)$ and $E_Q(z)$,

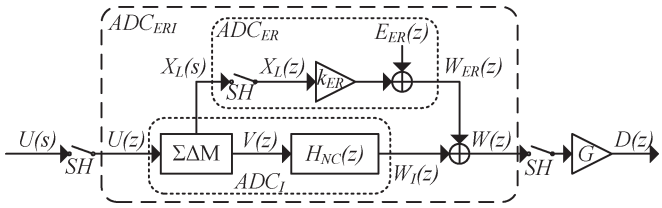

Fig. 3. Linearized block diagram of the ERIΣΔ ADC.

respectively. These terms can be obtained by replacing (1), (4), and (5) into (6) and are given by

$$\begin{aligned} X_{LU}(z) &= X_L(z)|_{E_Q=0} \\ &= U(z)\left(FF_{X_L}(z) - STF(z)FB_{X_L}(z)\right) \quad (9) \\ X_{LE}(z) &= X_L(z)|_{U=0} \\ &= -E_Q(z)NTF(z)FB_{X_L}(z). \quad (10) \end{aligned}$$

Based on the DT equivalents of the modulator's and last integrator's outputs, given in (1) and (6), respectively, it is possible to obtain the noise cancellation filter transfer function $H_{\mathrm{NC}}(z)$, as shown in the following section.

B. Noise Cancellation Filter

The purpose of the noise cancellation filter $H_{\mathrm{NC}}(z)$ is to cancel the noise contribution of the modulator's quantizer $E_Q(z)$. $H_{\mathrm{NC}}(z)$ can be designed, as in [8], by assuming a sampling rate of $X_L(z)$ equal to the output rate of $H_{\mathrm{NC}}(z)$. Fig. 3 shows a linearized model of the ERIΣΔ ADC, together with a scaling coefficient G that relates the ADC's output value $W(z)$ to the input $U(z)$. The output of the $\mathrm{ADC_{ERI}}$ $W(z)$ at sampling times equal to $1/f_S$ is given by

$$\begin{aligned} W(z) &= W_I(z) + W_{\mathrm{ER}}(z) \\ &= V(z)H_{\mathrm{NC}}(z) + X_L(z)k_{\mathrm{ER}} + E_{\mathrm{ER}}(z) \quad (11) \end{aligned}$$

where $W_I(z)$ and $W_{\mathrm{ER}}(z)$ are the outputs of $\mathrm{ADC_I}$ and $\mathrm{ADC_{ER}}$, respectively, $E_{\mathrm{ER}}(z)$ is the quantization noise of $\mathrm{ADC_{ER}}$, and k_{ER} is the $\mathrm{ADC_{ER}}$ gain.

By replacing (1) and (6) into (11), it can be observed that the cancellation of $E_Q(z)$ can be obtained by solving

$$0 = V_E(z)H_{\mathrm{NC}}(z) + X_{LE}(z)k_{\mathrm{ER}} \quad (12)$$

from where the value of $H_{\mathrm{NC}}(z)$ is found equal to

$$H_{\mathrm{NC}}(z) = -\frac{X_{LE}(z)k_{\mathrm{ER}}}{V_E(z)} = FB_{X_L}(z)k_{\mathrm{ER}}. \quad (13)$$

The output of the $\mathrm{ADC_{ERI}}$ $W(z)$ when using the noise cancellation filter $H_{\mathrm{NC}}(z)$, given by (13), will then be

$$W(z) = U(z)FF_{X_L}(z)k_{\mathrm{ER}} + E_{\mathrm{ER}}(z). \quad (14)$$

The main advantage of (13) and (14) is that they are valid for any type of loop filter, allowing a rapid identification of the noise cancellation filter $H_{\mathrm{NC}}(z)$. Moreover, these equations provide the groundwork from where the ADC output can be calculated, and as it will be addressed in the subsequent sections, the influence of the loop filter topology and the sensitivity to key CT nonidealities can be analyzed.

C. ADC Output Estimation

As explained in Section II-B, the calculation of $H_{\mathrm{NC}}(z)$ was performed assuming that every block in the ADC operates at the modulator's sampling rate, while from Fig. 1, it can be seen that the ADC produces a valid output only every N cycles. Accordingly, the valid ADC's output, as well as the scaling coefficient G, can be obtained by evaluating (14) at sampling times $n = N$, as follows.

Considering that $FF_{X_L}(z)$ is a causal linear-time-invariant system and that $U(z)$ is a causal sequence ($u(n) = 0$ for $n < 0$), the $\mathrm{ADC_{ERI}}$ output given in (14), at sampling times equal to $1/f_S$, can be expressed in the time domain as

$$w(n) = \sum_{k=0}^{n} u(n)h(n-k) + e_{\mathrm{ER}}(n) \quad (15)$$

where $h(n)$ is the impulse response of $FF_{X_L}(z)$ multiplied by the $\mathrm{ADC_{ER}}$ gain given by

$$h(n) = \mathcal{Z}^{-1}\left\{FF_{X_L}(z)\right\}k_{\mathrm{ER}}. \quad (16)$$

Furthermore, by recalling that the $\mathrm{ADC_{ERI}}$ output is only valid after N cycles and that the input $U(z)$ is held, thus constant, over N cycles, the output of the $\mathrm{ADC_{ERI}}$, at sampling times equal to N/f_S, can be expressed as

$$w(N) = U\left(\sum_{k=0}^{n} h(n-k)\right)\Bigg|_{n=N} + e_{\mathrm{ER}}(N) \quad (17)$$

where U is the value of the held input. The scaled output of the $\mathrm{ADC_{ERI}}$ can then be directly obtained from (17) as

$$d(N) = w(N)G = U + e_{\mathrm{ER}}(N)G \quad (18)$$

where G is the scaling coefficient given by

$$G = \frac{1}{\left(\sum_{k=0}^{n} h(n-k)\right)|_{n=N}}. \quad (19)$$

The second term of (18) represents the $\mathrm{ADC_{ERI}}$ quantization error and can be used to estimate the achievable signal-to-quantization-noise ratio (SQNR). Assuming a sinusoidal input signal with a full-scale input value equal to U_{FS}, the general SQNR expression for the $\mathrm{ADC_{ERI}}$ is

$$SQNR_{\mathrm{ERI}} = 20\log\left(\frac{\frac{U_{\mathrm{FS}}}{2\sqrt{2}}}{e_{\mathrm{ER,RMS}}G}\right) \quad (20)$$

where $e_{\mathrm{ER,RMS}}$ is the root-mean-square (RMS) value of $e_{\mathrm{ER}}(N)$. Note that a general expression is given here, with respect to the $\mathrm{ADC_{ERI}}$ SQNR, in order to preserve a general approach that could be applied for any type of loop filter. Further considerations will be made in Section III when the influence of the loop filter will be taken into account.

D. Incremental Versus ER Performance

As stated in Section II-B, the objective of $H_{\mathrm{NC}}(z)$ is to cancel the noise contribution of the modulator's quantizer. Looking from the perspective of two separate systems $\mathrm{ADC_{ER}}$

and ADC_I, $H_\text{NC}(z)$ is forcing the quantization error of the unscaled ADC_I output $W_I(z)$ to be equal in magnitude to $X_L(z)$, so it can be refined by ADC_ER. This type of filter $[H_\text{NC}(z) = FB_{X_L}(z)]$ has been used not only for ER [2] but also for several incremental implementations [5], [7]–[10], where $H_\text{NC}(z)$ has been obtained by setting an upper limit of the ADC_I quantization error based on the bounded output of the last integrator [11].

The performance improvement of ER implementations with respect to such IΣΔ ADCs can be verified by calculating the SQNR of the ADC_I and relating it to (20). The unscaled output of ADC_I $W_I(z)$ can be obtained from Fig. 3 and is given by

$$W_I(z) = V(z)H_\text{NC}(z) = V(z)FB_{X_L}(z)k_\text{ER}. \tag{21}$$

Moreover, by substituting (21) into (6) and evaluating it at sampling times equal to N/f_S, it is possible to derive the unscaled value of the incremental quantization error as

$$x_L(N) = \frac{U}{Gk_\text{ER}} - \frac{w_I(N)}{k_\text{ER}} \tag{22}$$

from where the scaled quantization error can be expressed as

$$e_I(N) = d_I(N) - U = -x_L(N)Gk_\text{ER} \tag{23}$$

where $d_I(N)$ is the scaled ADC_I output given by

$$d_I(N) = w_I(N)G. \tag{24}$$

Assuming a sinusoidal input signal with a full-scale input value equal to U_FS, the SQNR of the ADC_I is thus

$$SQNR_I = 20\log\left(\frac{\frac{U_\text{FS}}{2\sqrt{2}}}{x_{L,\text{RMS}}Gk_\text{ER}}\right) \tag{25}$$

where $x_{L,\text{RMS}}$ is the RMS value of $x_L(N)$. Considering (25), the $SQNR_\text{ERI}$ in (20) can be expressed as

$$\begin{aligned} SQNR_\text{ERI} &= 20\log\left(\frac{\frac{U_\text{FS}}{2\sqrt{2}}}{x_{L,\text{RMS}}Gk_\text{ER}} \cdot \frac{x_{L,\text{RMS}}Gk_\text{ER}}{e_{\text{ER,RMS}}G}\right) \\ &= SQNR_I + SQNR_\text{ER} \end{aligned} \tag{26}$$

where $SQNR_\text{ER}$ is the SQNR of the ADC_ER given by

$$SQNR_\text{ER} = \frac{x_{L,\text{RMS}}k_\text{ER}}{e_{\text{ER,RMS}}}. \tag{27}$$

Similar with (20), no further assumptions are made on the statistical properties of the ADC_I and ADC_ER quantization errors. According to (26), the SQNR performance of the incremental section ADC is directly, and linearly, improved by the SQNR of the ADC_ER. The selection of an appropriate loop filter topology, as demonstrated hereinafter, will be critical in order to fully benefit from such improvement.

III. Loop Filter Influence

From (26), it was observed that the SQNR performance of the ADC_ERI can be divided into the respective performances of its subsystems ADC_ER and ADC_I. As a first-level approximation and assuming a dynamic range (DR) of the ADC_ER equal to its input $x_L(N)$, the magnitude of $e_{\text{ER,RMS}}$ can be assumed inversely proportional with respect to the number of ADC_ER levels. Although no further observations can be made about $x_{L,\text{RMS}}$ and G until a loop filter is selected, it is already apparent that, in order to maximize the $SQNR_\text{ERI}$ performance, $x_{L,\text{RMS}}$ has to be minimized. The magnitude of $x_{L,\text{RMS}}$, and its dependence with respect to the loop filter topology, can be qualitatively analyzed from $X_L(z)$ in (6). Furthermore, this analysis can also be used to establish key differences between DT and CT incremental implementations and ER implementations.

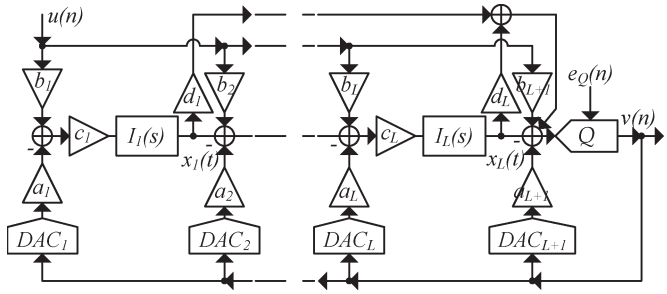

Fig. 4. General block diagram of a low-pass SL CT ΣΔ modulator, with all zeros at dc, used in the ERIΣΔ ADC.

As it would be impractical to cover all possible loop filter topologies, this work will concentrate on previous structures used in incremental and ER implementations. Several topologies have been used in such implementations, with $FB_{X_L}(z)$ as digital filters, including cascade-of-integrators-in-feedback (CIFB) configuration [9], cascade-of-integrators-in-feedforward (CIFF) configuration [10], and cascade-of-integrators-in-feedforward-with-input-feedforward (CIFF+IFF) configuration [2], [5], [7], [8]. These topologies can be studied with the aid of a block diagram for a general low-pass SL ΣΔ modulator, as shown in Fig. 4. With respect to DT incremental ADCs [12], the use of CIFF+IFF ($b_2, \ldots, b_L = 0$, $b_{L+1} = 1$, and $d_1, \ldots, d_L \neq 0$) topology presents two key advantages compared to its counterparts: 1) superior immunity to coefficients' spread and 2) input signal independence of $X_L(z)$. Moreover, the input signal independence reduces the magnitude of $X_L(z)$, which represents an advantage not only for incremental but also for ER implementations.

With respect to CT incremental ADCs, the sensitivity to coefficient deviations can be appreciated by analyzing $H_\text{NC}(z)$ from (13) and its dependence on $FB_{X_L}(z)$. Taking (8) into account, $FB_{X_L}(z)$ can also be expressed as

$$FB_{X_L}(z) = \sum_{i=1}^{L}\left(IIT\left(R_i(s)\prod_{j=i}^{L}I_j(s)\right)\prod_{j=i}^{L}c_j a_i\right) \tag{28}$$

where c_j and a_i are the scaling coefficients of the modulator, $R_i(s)$ is the DAC impulse response of the ith feedback branch, and $I_j(s)$ is the transfer function of the jth integrator. From (28), it can be seen that, as there are different sets of scaling coefficients per branch, the number of feedback branches will have a strong impact on how the integrator's mismatches will affect $W_I(z)$. It can be also seen that, when there is only one

feedback branch, as in CIFF and CIFF+IFF configurations, the integrators' coefficients will only act as scaling factors and their spread will not degrade the resolution of the ADC_I output $W_I(z)$. This behavior is similar to that of DT incremental ADCs and is consistent with the simulations shown in [8] for a third-order CT IΣΔ ADC with CIFF+IFF topology.

While only feedback paths were considered when designing $H_{\text{NC}}(z)$, both paths have to be taken into account to obtain $X_L(z)$, thus, the noise characteristics of $W_I(z)$. The input signal dependence of $X_L(z)$ can be analyzed with (9) from where relevant observations can be made. Naturally, as in traditional ΣΔ modulators, the use of CIFB topologies prevents the input signal independence. Furthermore, assuming a single feedback path, the dependence of $X_L(z)$ on the input signal will be determined by both the number of feedforward branches and the DAC coding scheme. In CT implementations with NRZ DAC, the independence is obtained by using CIFF+IFF which leads to a unity STF and $FF_{X_L}(z) = FB_{X_L}(z)$. However, this is not sufficient when using other DAC coding schemes in high-order modulators. The dependence of $X_L(z)$ on $U(z)$ is caused by the difference in the transfer functions $FB_{X_L}(z)$ and $FF_{X_L}(z)$ and the deviation of the STF from unity due to the use of a non-NRZ coding scheme in the feedback DAC. In order to counteract this issue, the signal independence of $X_L(z)$ can be guaranteed if a CIFF-with-full-input-feedforward topology ($b_1, \ldots, b_{L+1} \neq 0$ and $d_1, \ldots, d_L \neq 0$) is used, in combination with a multibit implementation ($k_q = 1$). It is also worth to mention that the input signal independence of $X_L(z)$ ($X_{LU}(z) = 0$) is not sufficient to assure the uncorrelation of the ADC quantization error with respect to the input signal, as the quantization noise $E_Q(z)$ could also be signal dependent, particularly for dc input signals [13].

When revisiting these features for the ERIΣΔ case, it can be observed that minimizing the magnitude of $X_L(z)$ is still critical, favoring the use of feedforward topologies. On the other hand, the effect of the $X_L(z)$ input signal correlation will, most likely, not appear in the ADC_ERI quantization error, due to the requantization that occurs in the ADC_ER. It will, however, impact the SQNR of the ADC_ER as it will determine the statistical properties of its input. Although the effect of nonidealities will be analyzed in Section IV, it is already visible that, as the quantization error cancellation depends on the matching of two branches $W_I(z)$ and $W_{\text{ER}}(z)$, any mismatch between these two branches will degrade the improvement gained by the use of ER.

IV. ERIΣΔ ADC Nonideal Behavior

The purpose of ER is to reduce the power dissipation of an IΣΔ ADC by using a low-power Nyquist-rate ADC [2] which refines its quantization error, thus reducing the required number of cycles N. Accordingly, a low-power ADC, such as a SAR converter, with a high number of bits could be used as ADC_ER. Such strategy is based on the assumption that the quantization error of the incremental portion is always available at the output of the last integrator and, thus, can be refined. The assumption of the ADC_ERI quantization error availability at the output of the last integrator is, however, no longer valid when nonidealities are present and limits, as a consequence, the use of error refinement. This effect will be first analyzed qualitatively while a case study will, later on, quantify its impact.

The source of this limitation can be appreciated by expressing (11) in terms of (1) and (6) while considering that the CT-DT transformation of the analog blocks will now depend on certain nonideal variable m. For simplicity, the ADC_ER gain, shown in Fig. 3, is assumed one, as in a multibit case ($k_{\text{ER}} = 1$). The output of ADC_ER $W_{\text{ER}}(z, m)$ is given by

$$W_{\text{ER}}(z,m) = U(z)FF_{X_L}(z,m) - V(z,m)FB_{X_L}(z,m) + E_{\text{ER}}(z). \quad (29)$$

Similarly, the output of ADC_I $W_I(z, m)$ is given by

$$W_I(z,m) = V(z,m)FB_{X_L}(z). \quad (30)$$

Taking these equations into account, the output $W(z, m)$ of the ADC_ERI, at sampling times equal to $1/f_S$, when subjected to mismatches between the analog and digital transfer functions, is given by

$$W(z,m) = U(z)FF_{X_L}(z,m) + E_{\text{ER}}(z) + V(z,m)\left(FB_{X_L}(z) - FB_{X_L}(z,m)\right). \quad (31)$$

Under ideal conditions, $FB_{X_L}(z)$ is equal to $FB_{X_L}(z,m)$, and (31) reduces to (11). Under mismatches, however, there will be a "leak" of $V(z,m)$ into the ADC_ERI quantization error which will be given by

$$E_{\text{ERI}}(z) = E_{\text{ER}}(z) + E_M(z,m) \quad (32)$$

where $E_{\text{ERI}}(z)$ is the ADC_ERI quantization error and $E_M(z, m)$ represents the portion of such quantization error that is due to mismatches between the analog and digital transfer functions, given by

$$\begin{aligned} E_M(z,m) &= V(z,m)\left(FB_{X_L}(z) - FB_{X_L}(z,m)\right) \\ &= V(z,m)\Delta_M(z,m) \end{aligned} \quad (33)$$

where $\Delta_M(z, m)$ represents the mismatch between analog and digital transfer functions. The importance of obtaining a close matching between the digital and the nonideal analog transfer functions can be appreciated from (33). As with cascaded modulators, the noise leakage can be minimized by modifying the noise cancellation filter $H_{\text{NC}}(z)$, so it resembles the nonideal analog transfer function $FB_{X_L}(z, m)$. From (31), it can be also seen that, under mismatches, there will be a gain error when calculating the scaled output of the ADC $d(N)$. This error will stem from the mismatches between $FF_{X_L}(z, m)$ and $FF_{X_L}(z)$.

The previous equations can be used to estimate the "leak" of $V(z, m)$ into the ADC_ERI and are useful to understand the origin of the mismatches. However, time-domain simulations are necessary to fully quantify their effect. Under mismatches, it is not sufficient to compute $\Delta_M(z, m)$ for quantifying the mismatch effect, as $E_M(z, m)$ also depends on $V(z, m)$, which will be also affected by the deviation of $FB_{X_L}(z, m)$. Time-domain simulations can therefore help in selecting a suitable set of parameters to obtain a required resolution under mismatches.

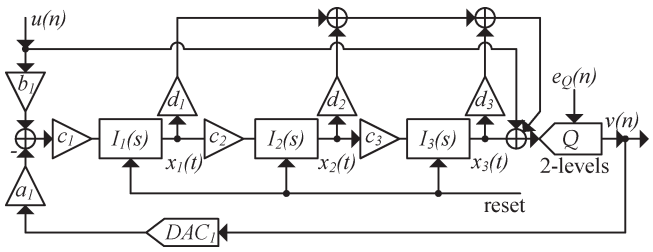

Fig. 5. Block diagram of the third-order single-bit CT IΣΔ modulator employed in the case study.

TABLE I
COEFFICIENT VALUES OF THE MODULATOR SHOWN IN Fig. 5

c_1	7.0042	d_1	2
c_2	0.7137	d_2	1
c_3	0.354	d_3	-0.5
a_1	0.5	b_1	0.05

V. CASE STUDY: A THIRD-ORDER ERIΣΔ ADC

To illustrate the theoretical analysis made in the previous sections, a test case based on the designed IΣΔ ADC proposed in [8] is presented here. The ER IΣΔ ADC's performance, as well as its sensitivity to nonidealities and the possibility of applying digital compensation of the analog-digital mismatches, has been evaluated through MATLAB/Simulink transient simulations. The modulator is shown in Fig. 5 and features a CIFF+IFF loop filter topology to minimize, as explained in Section III, the signal dependence of the quantization error. Furthermore, a third-order single-bit architecture has been chosen as it provides a good tradeoff between the number of cycles and digital filter complexity. A switched-capacitor-resistor (SCR) coding scheme, with a mean lifetime value $\tau = 1/10T_S$, is used as feedback DAC to reduce the sensitivity to clock jitter.

Stability considerations are similar as those for DT IΣΔ ADCs [7]. Accordingly, the NTF has been chosen using [14] with an out-of-band gain of 1.5 and assuring that the output of the last integrator $x_3(n)$ is bounded between the input full-scale values $\pm U_{\rm FS}/2$. The maximum input signal $U_{\max}$ has been set to -3 dBFS, close to the maximum stable amplitude of the converter, and the modulator's coefficients, assuming a normalized sampling rate of one ($T_S = 1$), are listed in Table I. The noise cancellation filter $H_{\rm NC}(z)$ has been obtained from (13) and is given by

$$H_{\rm NC}(z) = \left(\frac{\alpha}{(z-1)} + \frac{\beta}{(z-1)^2} + \frac{\gamma}{(z-1)^3}\right) k \tag{34}$$

where

$$\alpha = \frac{1}{8}\left(8\tau^2\left(1 - e^{-\frac{1}{2\tau}}\right) - 4\tau + 1\right) \tag{35}$$

$$\beta = -\frac{1}{2}\left(2\tau\left(1 - e^{-\frac{1}{2\tau}}\right) - 2 + e^{-\frac{1}{2\tau}}\right) \tag{36}$$

$$\gamma = 1 - e^{-\frac{1}{2\tau}} \tag{37}$$

$$k = k_{\rm ER}\tau a_1 \prod_{j=1}^{3} c_j. \tag{38}$$

Similarly, the value of the gain G, scaling the ADC_{ERI} output to the input U, is obtained from (19) and is given by

$$G = \frac{6}{k_{\rm ER} N^3 b_1 \prod_{j=1}^{3} c_j}. \tag{39}$$

Equations (34)–(39) provide the starting point for estimating the ADC's performance, evaluating its sensitivity to nonidealities and counteracting analog-digital mismatches.

A. Theoretical Performance

The ADC theoretical performance can be roughly approximated from (26). Assuming that the output of the last integrator $x_L(N)$, where $L = 3$, has a uniform distribution with a full-scale value equal to the full-scale value of the input signal $U_{\rm FS}$, the DR of the ADC_{I} DR_I, resulted from (25), can be expressed as

$$\begin{aligned} DR_I &= 20\log\left(\frac{\frac{U_{\rm FS}}{2\sqrt{2}}}{\frac{U_{\rm FS}}{\sqrt{12}} G k_{\rm ER}}\right) \\ &= 20\log\left(\sqrt{\frac{3}{2}}\frac{1}{G k_{\rm ER}}\right). \end{aligned} \tag{40}$$

Therefore, by replacing (39) into (40), it is possible to obtain the DR of the test case as

$$DR_I = 20\log\left(\sqrt{\frac{3}{2}}\frac{N^3 b_1 \prod_{j=1}^{3} c_j}{6}\right). \tag{41}$$

Similarly, the ADC_{ER} DR $DR_{\rm ER}$ can be approximated by assuming that its full-scale input is identical with the output of the last integrator $x_3(N)$ and that its quantization error has a uniform distribution with a full-scale value also equal to the full-scale value of $x_3(N)$. As $x_3(N)$ is also assumed to have a uniform distribution, the DR of the ADC_{ER} $DR_{\rm ER}$, resulted from (27), will be given by

$$DR_{\rm ER} = 20\log\left(\frac{\frac{x_{3,\rm FS}}{\sqrt{12}}}{\frac{x_{3,\rm FS}}{2^{B_{\rm ER}}\sqrt{12}}}\right) = 6.02 B_{\rm ER} \tag{42}$$

where $x_{3,\rm FS}$ is the full-scale value of $x_3(N)$ and $B_{\rm ER}$ is the number of bits in the ER ADC, i.e., ADC_{ER}. It is worth to notice that (42) has been derived assuming a multibit case ($k_{\rm ER} = 1$), which is according with the statistical properties assumed for the ADC_{ER} quantization error.

From (41) and (42), the impact of system-level parameters on the ADC's performance can be appreciated as follows. With respect to the ADC_{I} DR, it can be seen that DR_I is proportional to N^3. Generalizing, the DR for a modulator of order L will be proportional to N^L, when CIFF+IFF topology is used. Furthermore, the use of multibit quantization will decrease the full-scale value of $x_3(N)$, due to a reduction in the modulator's quantization error, and will allow a more aggressive NTF, which, in turn, will increase the value of the loop filter coefficients. With respect to the ADC_{ER}, the effect of the ADC_{ER} bits $B_{\rm ER}$ can be easily seen in (42), obtaining a 6.02-dB increment in DR for each bit added.

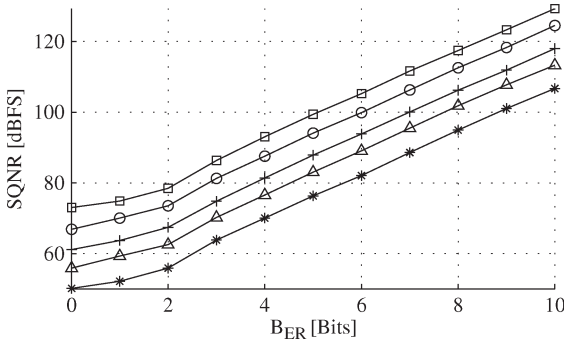

Fig. 6. SQNR versus number of cycles N and bits of ER converter B_{ER} for a third-order single-bit CIFF+IFF IΣΔ ADC. (References: (□) $N = 61$, (◯) $N = 48$, (+) $N = 39$, (△) $N = 31$, and (⋆) $N = 25$).

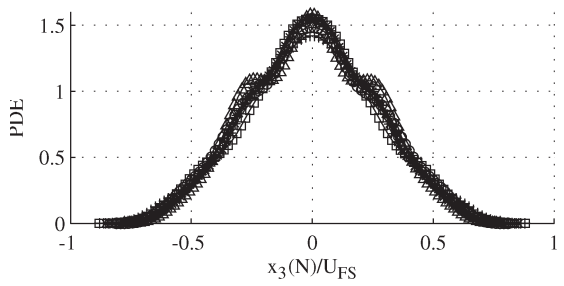

Fig. 7. PDE of $x_3(N)$. (References: (□) $N = 61$, (◯) $N = 48$, (+) $N = 3$, (△) $N = 31$, and (⋆) $N = 25$).

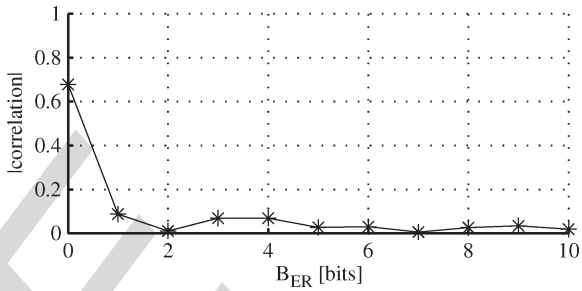

Fig. 8. Linear correlation between input signal and quantization error versus $\mathrm{ADC_{ER}}$ bits.

In order to validate (41) and (42), system-level transient simulations have been performed on the test case ERIΣΔ ADC, composed by the IΣΔ modulator in Fig. 5 with a noise cancellation filter $H_{\mathrm{NC}}(z)$, as described in (34). Shown in Fig. 6, the SQNR for an input signal with a −6-dBFS amplitude has been computed for a number of cycles N, while sweeping the number of $\mathrm{ADC_{ER}}$ bits B_{ER} from zero (for the incremental case) to ten. The number of required cycles has been calculated using (41) in order to achieve, in the incremental case, an SQNR from 42 to 66 dB in steps of 6 dB, so as to better appreciate its influence on the ADC's performance. As in traditional ΣΔ modulators [15] and pipelined ADCs, the effective gain of the $\mathrm{ADC_{ER}}$ k_{ER} in Fig. 3 has been assumed equal to two for the single-bit case and equal to one for the multibit case. Moreover, the full-scale input of the $\mathrm{ADC_{ER}}$ is assumed identical to $x_3(N)$. When compared to the performance of an IΣΔ ADC ($B_{\mathrm{ER}} = 0$), Fig. 6 shows that a similar SQNR could be achieved by using a 5-b $\mathrm{ADC_{ER}}$ while decreasing the number of cycle runs by 41%. Assuming a low-power $\mathrm{ADC_{ER}}$, this option could provide a lower power alternative.

Although the system-level simulations shown in Fig. 6 agree qualitatively with the approximations made in (41) and (42), there are some discrepancies worth mentioning. With respect to the $\mathrm{ADC_I}$ case ($B_{\mathrm{ER}} = 0$), (41) correctly predicts the influence of N on the $\mathrm{ADC_I}$ performance, increasing, as calculated, by approximately 6 dB per case. However, the predicted values have an offset of approximately 8 dB with respect to the simulation results. For example, (41) predicts an SQNR of 42 dB, for a −6-dBFS input signal and $N = 25$, instead of the 50 dB observed in the simulations, thus underestimating the $\mathrm{ADC_I}$ performance by 8 dB. Similar discrepancies are also found for other values of N. With respect to the $\mathrm{ADC_{ER}}$ performance, two different trends can be observed. When using an $\mathrm{ADC_{ER}}$ with 3–10-b resolution, its SQNR performance has a slope corresponding to approximately 6 dB per bit. On the other hand, the slope is degraded to around 3 dB per bit when using one or two bits. When compared to (42), this will translate into an overestimation of the $\mathrm{ADC_{ER}}$ performance. These discrepancies can be understood by observing the probability density estimate (PDE) of the unscaled $\mathrm{ADC_I}$ quantization error $x_3(N)$, which will influence the performance of both the $\mathrm{ADC_I}$ and $\mathrm{ADC_{ER}}$. Fig. 7 shows the PDE of $x_3(N)$ for the number of cycles selected previously, where two fundamental differences can be appreciated with respect to the assumptions made for such output: 1) Its full-scale value is not equal to the full-scale input value, and 2) the distribution is not uniform but rather concentrated between $\pm 0.5\ U_{\mathrm{FS}}$. The reduction in the full-scale value of $x_3(N)$ and its distribution will decrease its RMS power, thus increasing the $\mathrm{ADC_I}$ performance with respect to the value predicted in (41). On the other hand, the distribution shown in Fig. 7 will negatively affect the SQNR performance of the $\mathrm{ADC_{ER}}$ for low number of bits. For the single-bit case, this could be partially counteracted by empirically modifying the effective $\mathrm{ADC_{ER}}$ gain; however, this is not possible for the multibit case.

Although the first-order approximation made in (41) and (42) can help to establish the system-level parameters, this section highlights the importance of system-level simulations in order to capture the behavior of ERIΣΔ ADCs, where the assumptions that are regularly made in traditional ΣΔ modulators are no longer valid.

B. Quantization Error Signal Dependence

According to Section III, even though the $\mathrm{ADC_I}$ quantization error could be signal dependent, this characteristic would be minimized when ER is applied. This behavior has been evaluated by analyzing the correlation coefficient [16] between the input and the $\mathrm{ADC_{ERI}}$ quantization noise as a function of the number of $\mathrm{ADC_{ER}}$ bits B_{ER}, as shown in Fig. 8. As it is possible to appreciate, the $\mathrm{ADC_I}$ quantization error ($B_{\mathrm{ER}} = 0$) has a strong correlation with the input signal; however, this effect is substantially counteracted when applying ER with at least 1 b.

C. Sensitivity to Circuit Nonidealities

As mentioned in Sections III and IV, the ADC_I quantization error refinement depends on the matching between the analog and digital transfer functions. Therefore, any mismatch between these functions, created by nonidealities, would cause a degradation of the improvement gained by using the ER approach. The sensitivity to key circuit-level nonidealities has been evaluated in MATLAB/Simulink environment with respect to the ADC's performance degradation. This has been performed by applying a -6-dBFS sinusoidal input signal and computing the signal-to-noise-plus-distortion ratio (SNDR). Fig. 9 shows the sensitivity to the considered nonidealities, when sweeping the ADC_ER bits B_ER from three to ten. To avoid cluttering, only the case of $N = 25$ is presented here.

With respect to the sensitivity to process variations, it is assumed that the RC products, affecting the gain $1/RC$ of each integrator, will suffer the same spread [17] Δ_{RC}. As shown in Fig. 5, the integrators' gain is given by the products of $(b_1\ c_1)$ and $(a_1\ c_1)$ for the first integrator and by c_2 and c_3 for the second and third integrators, respectively. As the spread will be the same for all RC products, it can be mapped as a coefficient error $(1 + \Delta_{RC})$ which can be added before each $I_i(s)$. Furthermore, as the coefficients d_1–d_3 can be implemented by ratios of R or C, their effect has been considered negligible. From Fig. 9(a), the high sensitivity of the test-case ADC to process variations which highlights the need of tuning circuitry to fully benefit from the ER approach can be seen. As shown in Section III, this behavior is in contrast with respect to incremental counterparts with similar loop filter topology, where coefficient variations will mainly affect the ADC's gain.

Nonidealities in the integrators' op-amps have been modeled assuming an op-amp–RC implementation [18]. Accordingly, the integrator's transfer function, from the ith input path, is given by

$$I(s)_i|_{RC} = \frac{k_i f_S}{s\left(1 + \frac{1}{A(s)}\right) + \frac{1}{A(s)}\sum_{j=1}^{L} k_j f_S} \tag{43}$$

where $A(s)$ is the nonideal op-amp transfer function, k_i is the integrator's scaling coefficient, and L is the number of input paths in the integrator. When considering the effect of a frequency-independent finite op-amp gain $A(s) = A_\text{dc}$, the integrator transfer function of (43) can be expressed as

$$I(s)_i|_{RC-A_\text{dc}} \approx \frac{k_i f_S}{s + \frac{1}{A_\text{dc}}\sum_{j=1}^{L} k_j f_S}. \tag{44}$$

Moreover, the effect of finite amplifier gain-bandwidth product (GBW) can be studied assuming a single-pole model for the op-amp transfer function $A(s)$ given by

$$A(s) = \frac{A_\text{dc}}{\frac{s}{\omega_p} + 1} \qquad GBW = A_\text{dc}\omega_p. \tag{45}$$

The integrator transfer function of (43), when considering the effect of finite amplifier GBW and assuming an amplifier dc gain A_dc sufficiently high, is obtained by replacing (45) in (43)

$$I(s)_i|_{RC-GBW} \overset{A_\text{dc}\gg}{\approx} \frac{k_i f_S}{s} \frac{\frac{GBW}{GBW + \sum_{j=1}^{L}|k_j f_S|}}{\frac{s}{GBW + \sum_{j=1}^{L}|k_j f_S|} + 1}. \tag{46}$$

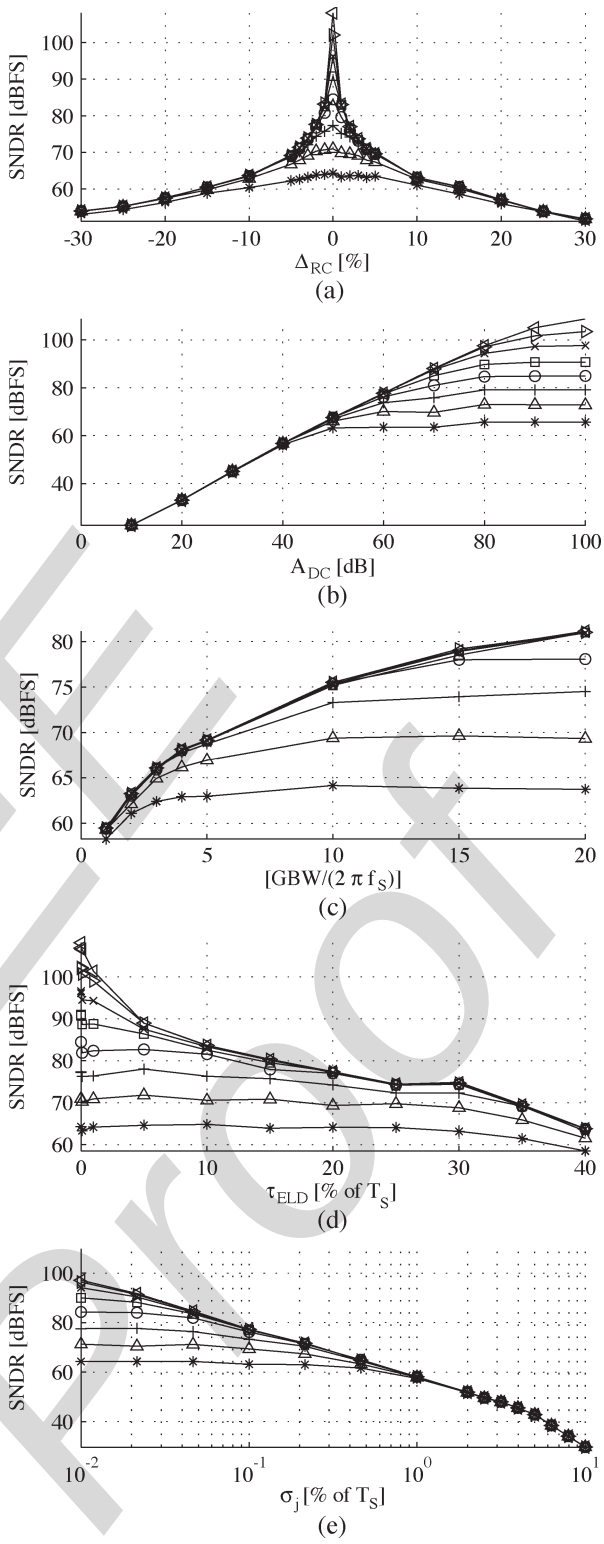

Fig. 9. ADC_ERI SNDR performance versus (a) integrators' coefficient deviation, (b) integrators' finite dc gain, (c) integrators' finite GBW, (d) DAC ELD, and (e) jitter standard deviation. (References: ADC_ER bits of (⋆) three, (△) four, (+) five, (◯) six, (□) seven, (×) eight, (▷) nine, and (◁) ten).

Fig. 9(b) and (c) shows the effects of finite amplifier dc gain and finite amplifier GBW, respectively, when considering (44) and (46) in the Simulink model. Contrary to what occurs in traditional SL ΣΔ ADCs and in line with cascaded modulators, the use of either low dc gain or low GBW will limit the use of the ER approach. This represents a severe drawback as it would affect the power consumption of CT ERIΣΔ ADCs.

The effect of nonidealities in the DAC waveform has been included with respect to the sensitivity to excess loop delay (ELD) and clock jitter, as shown in Fig. 9(d) and (e), respectively. Such effects have been modeled either by simply delaying the DAC feedback waveform by a constant time τ_{ELD}, in the case of ELD, or by randomly varying the DAC's clock edges, with a statistical standard deviation σ_j, in the case of jitter. Although the use of SCR coding scheme has attenuated the sensitivity to jitter, it can be seen, as in the previous cases, that the sensitivity increases when increasing the number of bits in the $\mathrm{ADC_{ER}}$, imposing tight requirements at a high number of $\mathrm{ADC_{ER}}$ bits. On the other hand, while sensitivity to ELD also exhibits a similar trend, it can be seen that such requirements would not be as restrictive as for the jitter case. This is due to the use of an SCR DAC, which will not only decrease the sensitivity to jitter but also increase the tolerance to ELD.

From Fig. 9, it is also possible to appreciate certain similarities between each case from where some general observations can be drawn. When looking at the influence of B_{ER}, all previous simulations contain a region, or "envelope," where there is no performance gain by the addition of extra $\mathrm{ADC_{ER}}$ bits. This is consistent with the qualitative analysis made in Section IV from where it is possible to realize that, for a given nonideality value, a mismatch between the digital and analog transfer functions will occur and certain noise will be injected; therefore, increasing the number of $\mathrm{ADC_{ER}}$ bits will no longer be effective. This effect highlights the need of careful noise cancellation filter design so as to counteract such negative effect.

D. Design Centering of Noise Cancellation Filter

As shown in Section IV, one of the main differences between traditional SL ΣΔ ADCs and ERIΣΔ counterparts is the existence, as in cascaded ΣΔ ADCs, of a noise cancellation filter that should match certain analog transfer function in order to prevent noise leakage. The filter developed in (34) provides a good system-level approximation and can be used to establish the theoretical performance of the ADC. However, it does not take into consideration nonidealities that appear in circuit implementation which results, as exemplified in Section V-C, in a suboptimal solution. In principle, it would be possible to mathematically derive a noise cancellation filter to account for all introduced nonidealities. This approach, however, becomes too cumbersome when going from system level to more refined abstraction levels such as block- or circuit-level implementation. In this work, optimization tools are employed so as to account for analog nonidealities in the noise cancellation filter design and, thus, reduce noise leakage. This approach has the advantage that can be directly applied, in all design steps, by simply rerunning the optimization algorithm.

TABLE II
COMPARISON OF TESTED ALGORITHMS

Function	$\mathrm{ADC_{ERI}}$ SNDR	# Functions
fminsearch	60.75 dB	43885
fminunc	84.33 dB	2439
multistart	84.47 dB	34814

When operating in transient mode, the noise cancellation filter given in (34) can be treated as an N-length finite impulse response (FIR) filter with the appropriate coefficients [12]. Furthermore, these coefficients are simply obtained by computing the N-length impulse response of the transfer function in (34). In order to minimize the noise leakage, the proposed method uses a MATLAB optimization algorithm to find the optimum N coefficients of the FIR filter. The goal of the aforementioned algorithm is set to maximize the $\mathrm{ADC_{ERI}}$ SNDR performance, assuming that a maximum SNDR will correspond to a minimum noise leakage. When computing such performance metric, the influence of the quantization error $E_{\mathrm{ER}}(z)$ is minimized by removing $\mathrm{ADC_{ER}}$ in Fig. 3, thus letting $x_3(N)$ to directly cancel the $\mathrm{ADC_I}$ quantization error. Furthermore, this performance metric is computed at an input signal amplitude where harmonics are not present.

One issue with respect to the use of optimization algorithms is the risk of not finding a global solution, thus leading to a suboptimal set of FIR coefficients. Although all solvers included in the *MATLAB Optimization Toolbox*[19] generally find a local optimum, the so-called "global optimization algorithms," present in the *MATLAB Global Optimization Toolbox* [20], counteract this issue by searching for solutions to problems that contain multiple maxima. The latter type of solvers, however, has the disadvantage of being significantly slower than the former type. Although an exhaustive study of the optimum solver is out of the scope of this paper, several algorithms have been tested in order to evaluate their efficiency in terms of the final solution and the speed to obtain such solution. In this work, the functions *fminsearch*, *fminunc*, and *multistart* were tested. The first two optimizers fall in the category of "minimizers" and attempt to find a local minimum of the objective function near an initial estimate. On the other hand, the last function starts a local solver from multiple start points in order to attempt to find a global optimum. In this work, *fminunc* has been used as such local solver. Default values were used in all evaluated functions with the exception of the maximum number of allowed iterations and the maximum number of allowed function evaluations. These values were increased, thus allowing the algorithm to be stopped when the $\mathrm{ADC_{ERI}}$'s SNDR could not be improved by more than certain tolerance. Moreover, the coefficients obtained from (34) were set as the initial estimate. Table II shows a comparison between the tested algorithms when using a test case with practical values for the nonidealities analyzed in Section V-C. The performance of each algorithm is measured with respect to the $\mathrm{ADC_{ERI}}$'s SNDR when using a 10-b $\mathrm{ADC_{ER}}$, while the speed is measured in the number of functions evaluated in order to reach that solution. It can be seen that *fminunc* is more efficient than *fminsearch*, in terms of both the $\mathrm{ADC_{ERI}}$'s SNDR obtained and the number of functions needed to obtain such result. Moreover, even though it reaches

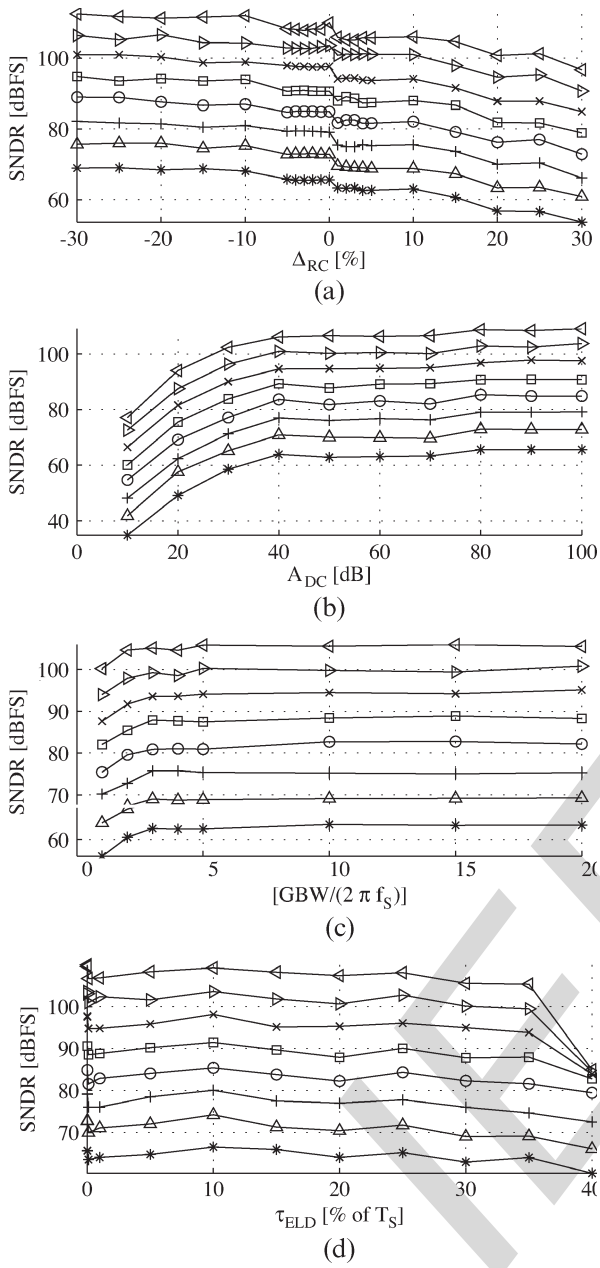

Fig. 10. ADC_{ERI} SNDR performance versus (a) integrators' coefficient deviation, (b) integrators' finite dc gain, (c) integrators' finite GBW, and (d) DAC ELD. (References: ADC_{ER} bits of (⋇) three, (△) four, (+) five, (◯) six, (□) seven, (×) eight, (▷) nine, and (◁) ten).

a similar result as *multistart*, it does it with significantly less number of functions evaluated. Based on these results, *fminunc* is selected to optimize the noise cancellation filter.

To validate the ADC_{ERI} performance when using the proposed filter, similar simulations as in Section V-C are shown in Fig. 10, with the exception of the sensitivity to clock jitter. As shown in Fig. 10(a), the proposed filter can successfully counteract the degradation induced from process variations, obtaining, in comparison with Fig. 9(a), 59 dB of SNDR improvement in the case of $\Delta_{RC} = -30\%$ and $B_{ER} = 10$. Although one can expect large deviations after physical implementation, the previous simulation highlights the possibility to compensate and even cancel the influence of such variations in the digital domain. When comparing Figs. 9(a) and 10(a), it is also worth to notice a different behavior with respect to the sensitivity to process variations. This difference can be understood as follows. With respect to Fig. 9(a), the dominant factor which limits the ADC's SNDR is the noise leakage from analog-digital transfer function mismatches. Accordingly, any deviation in the integrators' coefficients, either positive or negative, will affect the required matching, which, in return, will decrease the ADC's performance. With respect to Fig. 10(a), the optimized digital filter is able to effectively counteract the analog-digital transfer function mismatches. However, as the digital filter is calibrated to match the nonideal analog transfer function, and not otherwise, loop gain errors will still affect the overall SNDR performance of the ADC. Similarly, as in traditional $\Sigma\Delta$ modulators, coefficient deviations will affect the NTF in the following way. A positive variation in the passives will translate into a reduction in the integrators' coefficients, which, in return, will result in a less aggressive NTF and increase the in-band noise, but it will not affect the stability. On the other hand, a negative variation in the passives will increase the integrators' coefficients, resulting in a more aggressive NTF. Although this will initially result in a slight increase in performance, it could potentially lead to instability, depending on the selected NTF, as well as on the magnitude of the input signal. This highlights the importance of proper NTF design so as to withstand the expected spread.

The effects of the proposed noise cancellation filter when considering op-amps' nonidealities are shown in Fig. 10(b) and (c), for finite amplifier dc gain and finite amplifier GBW, respectively. Contrary to the respective simulations shown in Section V-C, now, it is possible to use an op-amp with a GBW product close to $2f_s$ and a dc gain close to 40 dB. While this represents a key feature for this architecture when compared to DT counterparts, it is worth remembering that only the effects described in (44) and (46) have been taken into account. Other nonidealities, such as thermal noise and nonlinear effects, will increase the lower boundary of the required dc gain.

With respect to DAC nonidealities, while the proposed filter could effectively enhance, as shown in Fig. 10(d), the ADC's sensitivity to ELD, depreciable improvement was found with respect to jitter degradation. Taking this into consideration, the choice of the SCR-DAC mean lifetime value τ represents a key design parameter to fully benefit from the ER approach, as it will determine the sensitivity to clock jitter. Moreover, as the jitter standard deviation in Fig. 9(e) is expressed with respect to the sampling frequency, this figure could be used to estimate the maximum frequency of operation for a given clock with certain absolute jitter standard deviation. As in traditional CT $\Sigma\Delta$ ADCs, jitter-induced degradations could also be counteracted by using multibit feedback DAC. This approach, however, would increase the complexity of the digital filter and may require an extra calibration circuitry to reduce the DAC mismatches.

Similar considerations apply with respect to the input referred circuit noise, as well as for the offset errors, in the case of converting dc inputs. As in such cases where an optimized filter obtains no improvement, the degradations induced by these nonidealities should be kept within the intended margin so as not to degrade the ADC's resolution.

VI. Conclusion

The theoretical analysis and circuit-level issues of ER incremental ADCs have been presented for CT high-order SL ΣΔ modulators. A general approach, applicable to any loop filter topology, quantizer's number of bits, and DAC's coding scheme, has been proposed so as to obtain key features of the building blocks and qualitatively analyze the loop filter influence as well as mismatches between analog and digital transfer functions. It was shown that, as in DT counterparts, feedforward loop filter topologies are preferable as they reduce the quantization error of the incremental section of the ADC, increasing, in turn, the ADC's overall performance. It was also found that, although CIFF+IFF topology does not provide independence between the input signal and the quantization error when using non-NRZ coding schemes, their correlation is minimized if ER is used. A third-order single-bit ERIΣΔ ADC has been used to illustrate the theoretical analysis and quantify the impact of critical circuit nonidealities. It was found that ERIΣΔ ADCs are highly sensitive to nonidealities, particularly if a large number of bits are used in the ER ADC. However, as most of the degradation stems from noise leakage due to analog-digital transfer function mismatches, this can be counteracted in the digital domain, as in cascaded ΣΔ modulators, by optimizing the noise cancellation filter so as to match the nonideal analog transfer function. When such matching is restored, the ADC can effectively benefit from relaxed amplifier's finite GBW and finite dc gain, allowing, as a consequence, a power-aware implementation. Furthermore, the test case results show the importance of nonidealities that could not be counteracted, such as thermal noise and jitter, and may influence both system- and circuit-level decisions. The theoretical analysis and test case both highlight the potential of CT ERIΣΔ ADCs for low-power multichannel applications and hint the designer about possible pitfalls in order to reach a successful implementation.

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Julian Garcia (S'10) received the B.S. degree in electrical and electronic engineering from Universidad Catolica de Cordoba, Cordoba, Argentina, in 2001 and the M.Sc. degree in electrical engineering with specialization in system-on-chip design from the KTH Royal Institute of Technology, Stockholm, Sweden, in 2007, where he is currently working toward the Ph.D. degree in the Integrated Devices and Circuits Unit. His doctoral work focuses on the design of low-power continuous-time sigma-delta modulators.

Saul Rodriguez (M'06) received the B.Sc. degree in electrical engineering from the Army Polytechnic School (ESPE), Quito, Ecuador, in 2001 and the M.Sc. degree in system-on-chip design and the Ph.D. degree in electronic and computer systems from the KTH Royal Institute of Technology, Stockholm, Sweden, in 2005 and 2009, respectively.

He is currently a Postdoctoral Researcher with the Integrated Devices and Circuits Unit, KTH. His research area covers from high-speed CMOS circuit design for wideband radio front ends to ultralow-power circuits for medical applications.

Ana Rusu (M'01) received the Diploma Engineer (M.S. degree) in electronics and telecommunications engineering from the Technical University of Iasi, Iasi, Romania, in 1983, the Ph.D. degree in electronics engineering from the Technical University of Cluj-Napoca, Cluj-Napoca, Romania, in 1998, and the Docent in circuit theory from the KTH Royal Institute of Technology, Stockholm, Sweden, in 2006.

Since September 2001, she has been with KTH, where she is currently a Professor in the Integrated Devices and Circuits Unit, School of Information and Communication Technology. Her research interests span from low-/ultralow-power high-performance circuit and system design for mobile communications and biomedical devices to application development. Her recent research areas also include high-frequency circuits for spin torque oscillator technology and circuits using emerging technologies, such as graphene and SiC. She develops applications for smartphone-based traffic information system and implantable system-on-chip biosensors. She has participated in several national and international research projects and has authored or coauthored more than 100 international scientific publications in journals, conference proceedings, books, and book chapters.