On Defect Oriented Testing for Hybrid CMOS/memristor Memory

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***Abstract*—Hybrid CMOS/memristor memory (hybrid memory) technology is one of the emerging memory technologies potentially to replace conventional non-volatile flash memory. Existing research on such novel circuits focuses mainly on the integration between CMOS and non-CMOS, fabrication techniques and reliability improvement. However, research on defect analysis for yield and quality improvement is still in its infancy stage. This paper presents a framework of defect oriented testing in hybrid memory based on electrical simulation. First, a classification and definition of defects is introduced. Second, a simulation model for defect injection and circuit simulation is proposed. Third, a case study to illustrate how the proposed approach can be used to analyze the defects and translate their electrical faulty behavior into fault models - in order to develop the appropriate tests and design for testability schemes - is provided. The simulation results show that in addition to the occurrence of conventional semiconductor memories faults, new unique faults take place, e.g., faults that cause the cell to hold an undefined state. These new unique faults require new test approaches (e.g., DfT) in order to be able to detect them.**

***Keywords*-memory defects; fault models; defect oriented testing; memristor;**

I. Introduction

Hybrid CMOS/memristor memory (hybrid memory) technology is one of the promising emerging memory technologies potentially to replace conventional non-volatile flash memory. In contrast to floating gate in flash, hybrid memory uses memristor as the storage element [1]–[4]. Moreover, the cell array can be stacked on the top of the CMOS peripheral circuits creating three-dimensional ICs; the interconnects between the top and bottom layer are realized using CMOS-to-nano vias (CNVs) [2]. With such novel devices and advanced circuit architecture, hybrid memory is able to offer appealing potentials such as enormous storage capacity, low power consumption, simple fabrication for cell array, etc [1]–[4]. Companies such as Hewlett-Packard and Hynix are working on such a memory technology, and they expect to deliver a product with 20 GBytes/cm^2 by 2013 [5].

Because of the above-mentioned potentials and commercialization efforts, the research on such a memory technology is growing. To this end, most of the work published so far focuses mainly on the integration between CMOS and non-CMOS, fabrication techniques and reliability improvement using fault tolerance schemes [1]–[7]. However, research on defect analysis, testing and design for testability for such devices is still in its infancy stage. Understanding the faulty behavior of the memory devices in the presence of defects will enable the development of appropriate fault models and efficient test schemes; thus, improve the outgoing product quality.

To the best knowledge of the authors, this paper is the first to address defect oriented testing for hybrid CMOS/memristor memories. The paper presents a classification and definition of possible defects in a hybrid memory system. In addition, an accurate and appropriate electrical simulation model is provided; the model can be used for defect injection and circuit simulation in order to understand the faulty behavior and develop accurate fault models. A case study will be presented to illustrate the simulation approach and how the faulty behavior can be analyzed and modeled.

The rest of the paper is organized as follows. Section II briefly overviews hybrid memory architecture including its structure and operation. Section III introduces a taxonomy of hybrid memory defects. Section IV describes the hybrid memory simulation model developed for the defect analysis. Section V presents a case study to illustrate the simulation methodology and fault modeling development. Section VI concludes this paper.

II. Hybrid Memory Architecture

This section reviews a hybrid memory architecture starting with its structure; and thereafter, its write and read operation.

A. Structure of hybrid memory

Fig. 1(a) shows the generic structure of a hybrid memory [2]. The memory consists of three main parts: (i) non-CMOS cell array, (ii) CMOS-to-nano vias (CNVs), and (iii) CMOS peripheral circuits. The top layer is the cell array formed by two sets of parallel nanowires crossing perpendicularly with bistable two-terminal devices (e.g., memristor) sandwiched at each crosspoint; the middle layer is the CNVs made of metal (e.g., copper, tungsten, etc.); the bottom layer consists of the peripheral circuits (e.g., decoder, sense amplifier, etc.) structured from CMOS.

1081-7735/11 $26.00 © 2011 IEEE
DOI 10.1109/ATS.2011.66

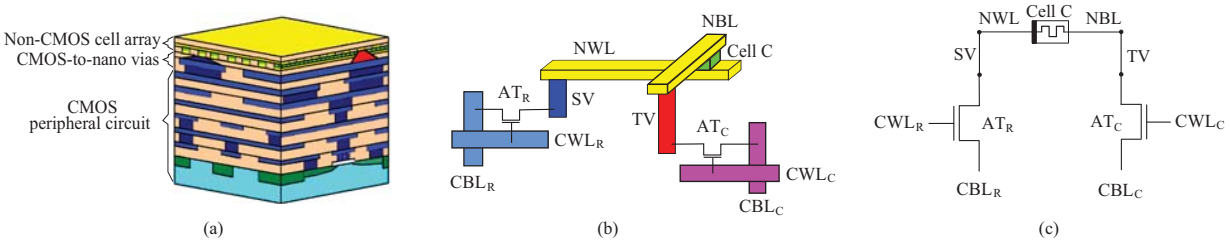

Figure 1. (a) Hybrid memories structure (b) a single memory cell connection (c) electrical equivalent circuit

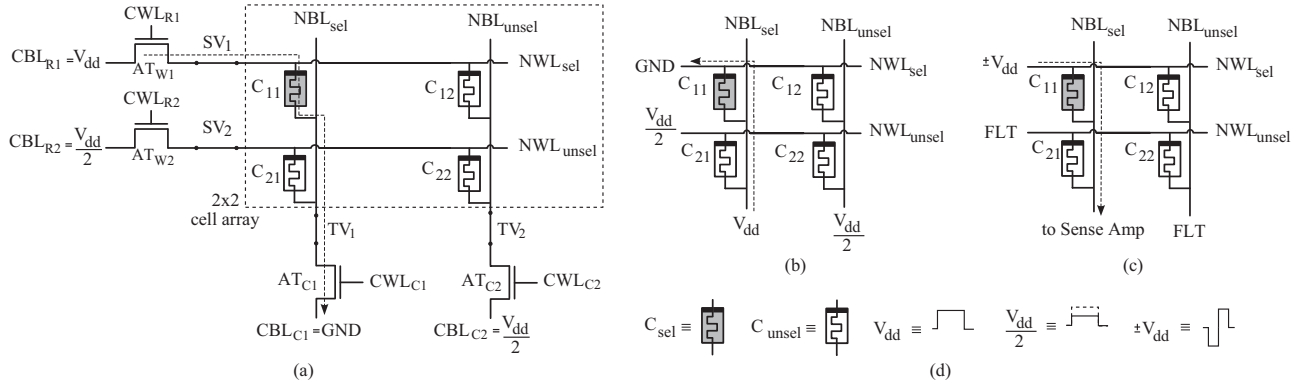

Figure 2. (a) Write 1 operation (b) write 0 operation (c) read operation (d) write and read voltages

Fig. 1(b) illustrates the connection of a single memristor memory cell (*C*), which is divided into two groups: (i) the row group and (ii) the column group. The row group consists of the components connected to the lower-side terminal of the memory cell; these include CMOS word line (CWL_R), CMOS bit line (CBL_R), access transistor (AT_R), short CNV (*SV*) and nanowire word line (*NWL*). Conversely, the column group comprises the components connected to the upper-side terminal of the memory cell; these include CMOS word line (CWL_C), CMOS bit line (CBL_C), access transistor (AT_C), tall CNV (*TV*) and nanowire bit line (*NBL*). The electrical equivalent circuit of this connection is shown in Fig. 1(c).

B. Write and read operations

The selected cell is written and read by biasing sufficient voltages across the cell. Fig. 2(a) shows a 2×2 cell array with the access transistors where a write 1 operation is applied to cell C_{11}; while Fig. 2(b) and Fig. 2(c) depict the biasing voltage required for write 0 and read operation, respectively. Fig. 2(d) illustrates the notations used in those figures such as $C_{sel}(C_{unsel})$ denoting the selected (unselected) cell, V_{dd} ($\frac{V_{dd}}{2}$) denoting write voltage for selected (unselected) cell and $\pm V_{dd}$ denoting read voltage. This read voltage has two different voltages: $-V_{dd}$ in the first half, whereas $+V_{dd}$ in the second half.

For write 1 operation to C_{11}, its word line NWL_{sel} is set to V_{dd} (by setting CBL_{R1} to V_{dd} and activating the access transistor AT_{R1}) and its bit line NBL_{sel} to *GND* (by setting CBL_{C1} to *GND* and activating the access transistor AT_{C1}) [10]. With this biasing condition, the write voltage

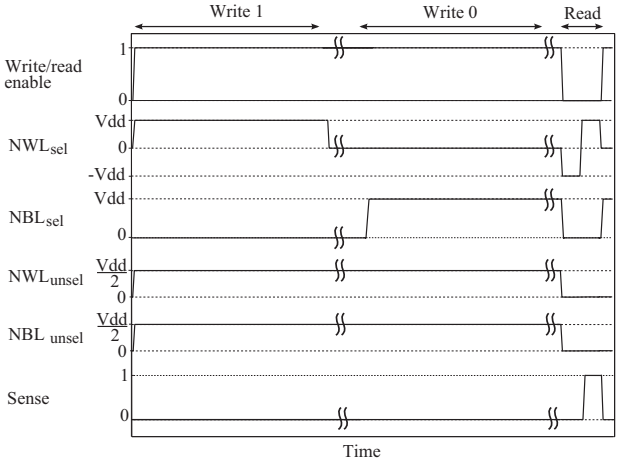

Figure 3. Timing diagram of write and read operations

is equal or larger than C_{11} threshold voltage, i.e., $V_{dd} \geq V_{th}$, enabling the write operation. At the same time, the unselected NWL_{unsel} and NBL_{unsel} are biased with $\frac{V_{dd}}{2}$. This second biasing condition causes no voltage drop across the unselected cells disabling any changes to the stored data.

Write 0 operation is performed by biasing C_{11} with V_{dd} from NBL_{sel}, while grounding NWL_{sel}; at the same time, NWL_{unsel} and NBL_{unsel} are biased with $\frac{V_{dd}}{2}$ (see Fig. 2(b)) [10]. For a read operation, C_{11} is biased with $\pm V_{dd}$ from NWL_{sel}, while connecting NBL_{sel} to sense amplifier; at the same time, both NWL_{unsel} and NBL_{unsel} are left floating denoted with *FLT* in Fig. 2(c). Fig. 3 illustrates the timing diagram for the three operations described above.

Table I
DEFECT CLASSIFICATION

Component	Classification	Location	Notation
Cell array	Open	Within cells	*OC*
		At nanowire bit lines (NBLs)	*OB*
		At nanowire word lines (NWLs)	*OW*
	Bridge	Between NBLs	*BB*
		Between NWLs	*BW*
		Between NBLs and NWLs	*BBW*
Via	Open	Within short CNVs	*OSV*
		Within tall CNVs	*OTV*
	Bridge	Between short CNVs	*BSV*
		Between tall CNVs	*BTV*
Peripheral circuits	Open	At gate, source and drain of transistor, interconnects	*OPC*
	Bridge	Among gate, source, drain and substrate of transistors, interconnects	*BPC*
	Short	At gate, source and drain of transistors, interconnects	*SPC*

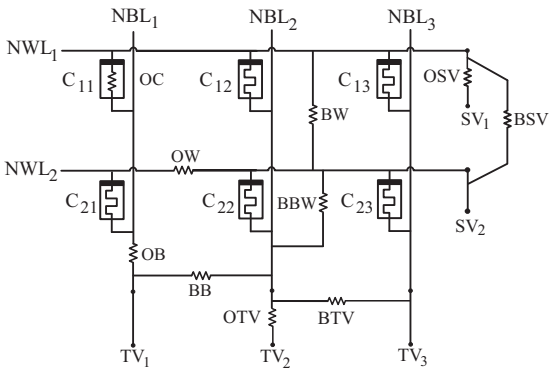

Figure 4. Possible opens and bridges in cell array as well as possible bridges in CNVs

III. DEFECTS CLASSIFICATION AND DEFINITION

Defects in memory circuits are physical structures that deviate from the intended layout design and caused by imperfection in the fabrication process. They introduce unintended disconnections or connections in the memory. Defects such as broken or missing metal lines, extra metal lines, etc. can be modeled at the electrical level using a resistor as follows [8]:

- **Open** – This is an unintended series resistance (R_{op}) within a connection in the range of $0\Omega < R_{op} \leq \infty\Omega$.
- **Bridge** – This is an unintended parallel resistance (R_{br}) between two connections in the range of $0\Omega < R_{br} \leq \infty\Omega$.
- **Short** – This is an unintended resistive path (R_{sh}) between a node and supplied voltage V_{dd}, or ground *GND*. The short resistance can be in the range of $0\Omega < R_{sh} \leq \infty\Omega$.

Table I gives the classification of defects in the three main parts of hybrid memory. Of all three parts, only defects in the cell array and CMOS-to-nano vias (CNVs) are discussed in this paper. This is because these two parts are parts that distinguish hybrid memories from the existing semiconductor memories. Defects in the peripheral circuits are similar to that in conventional RAMs [15], [16]. In the rest of this section, defects within the cell array and in CNVs will be discussed.

A. Defects within cell array

Defects in the cell array can be either opens or bridges; see Table I.

1) Open within memory cells: Opens can occur within the memory cells (i.e., memristor), at nanowire bit lines (NBLs) or nanowire word lines (NWLs). Such opens increase the connection resistivity of the affected locations. For example in Fig. 4, opens within the cell C_{11} (denoted as *OC*) are due to, e.g., insufficient dopant [12] that will cause its resistance to be extremely high; hence preventing writing an appropriate value in it. On the other hand, opens in NBLs (*OB*) and NWLs (*OW*) are due to, e.g., missing material, broken nanowire, etc. as a result of excessive force of nanoimprint lithography process, doping variation in the nanowire, and device width fluctuation as a result of variation in nanoimprint lithography and patterning process [4], [13]. For example in Fig. 4, *OB* (*OW*) at *NBL*$_2$ (*NWL*$_2$) affects both write and read operations to C_{21} (C_{22}).

2) Bridges between NBLs, between NWLs, and between NBLs and NWLs: Bridges create an unintended connection between NBLs (*BB*), between NWLs (*BW*) or between NBLs and NWLs (*BBW*); see Fig. 4. This defect type can occur due to, e.g., a broken nanowire or an unintended longer nanowire that is connected to its adjacent nanowire, etc. [4]. For example, *BB* connects *NBL*$_2$ to *NBL*$_1$ causing, e.g., a disturbance to C_{21} when write operation is performed to C_{22}. Likewise, *BW* causes a disturbance to C_{22} when write operation is performed to C_{12}. On the other hand, *BBW* that bypasses the victim cell C_{22} may affect the read operation to the cell.

B. Defects in CMOS-to-nano vias (CNVs)

Defects in CNVs can be either opens or bridges. Note that this classification and definition is based on through silicon vias (TSVs) in the existing 3D-ICs [14], not the real CNVs in hybrid memories. This is because of two main reasons: (i) lack of literatures reporting this type of defect for hybrid memories, and (ii) the structure and fabrication of the CNVs are very similar to that of TSVs.

1) Opens in tall and short CNVs: Opens in tall CNVs (*OTV*) and short CNVs (*OSV*) may occur due to, e.g., broken or crack as the result of excessive polishing during fabrication, void after filling, misalignment, poor contact between the top-edge of tall (short) CNVs and NBL (NWL), etc. [14]; see Fig. 4. Opens in these vias may impact the write and read operations to the victim cell.

2) Bridges between tall CNVs and between short CNVs: A bridge between tall CNVs (*BTV*) and between short CNVs (*BSV*) occurs due to severe misalignment as a result of, e.g., imprecise mask [14]; see Fig 4. Bridges between these vias may impact the write and read operations to the victim cell.

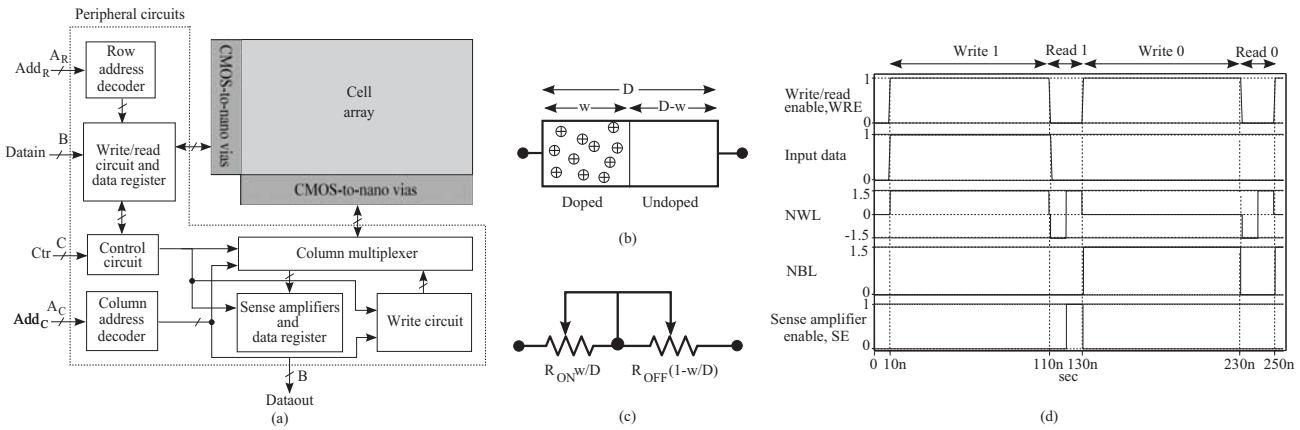

Figure 5. (a) Block diagram of hybrid memory (b) HP's memristor model (c) HP's memristor electrical equivalent circuit (d) control signal timing

IV. Simulation Model

This section introduces the hybrid memory model developed for defect injection and simulation using HSPICE and Verilog-AMS. First, the block diagram of SPICE memory model will be described. Then, the electrical model used for memristor will be explained. Finally, the write/read timing requirements and logic state definition will be covered.

A. Hybrid memory model

Fig. 5 depicts the block diagram of the hybrid CMOS/memristor memory proposed in [11]. The memory comprises: (i) CMOS peripheral circuits, (ii) non-CMOS cell array, and (iii) CMOS-to-nano vias (CNVs). The peripheral circuits consist of the functional units that are similar to those used in existing semiconductor memories. Both row and column decoders operate together to access the selected memory cell in the cell array. The write/read circuits supply appropriate voltages for write (depending on the input data value in data register) and read operations. Sense amplifier senses read current, converts into voltage and amplifies prior to sending the output data to data register. Column multiplexer connects the nanowire bit lines in the cell array to the write circuit; it also connects the cell array to sense amplifier during read operation. All these operations are controlled by the control circuit. Note that the nanowires in the cell array and CNVs are assumed to be simple interconnects where the resistance is negligible.

B. Memristor device model

A memristor is a two-terminal nanodevice that can be used to represent logic data [9]. Interestingly, its resistance (referred to as *memristance*) is retained even when power is switched off, thus memristor can be used as non-volatile storage element for memory applications. Based on the theoretical formulation by L. Chua in 1971, a group of Hewlett-Packard (HP) researchers developed the memristor prototype and the electrical model in 2008 [9]. The HP's memristor is fabricated using a thin film of titanium dioxide that consists of two layers with different oxygen atoms doping rate: *doped* and *undoped* as shown in Fig. 5(b). The doped region has a width of w and corresponds to a low memristance R_{ON}, while the undoped region has a width of *D–w* and corresponds to a high memristance R_{OFF} where D the total width of the memristor. Fig. 5(c) shows the equivalent electrical circuit of a memristor modeled as a coupled variable resistor [9].

The voltage-current relation of memristor is defined as follows [9].

$$v(t) = i(t)\Big(R_{ON}\frac{w(t)}{D} + R_{OFF}(1-\frac{w(t)}{D})\Big) \tag{1}$$

where $w(t)$ is the width of the doped region of a memristor that changes with time. According to [12], $w(t)$ is normalized with respect to D and is referred to as the *memristor internal state*; it is given as follows.

$$\frac{w(t)}{D} = 1 - \sqrt{1 - \frac{2\mu_v \Phi(t)}{\beta D^2}} \tag{2}$$

where $\Phi(t)$=$\int_0^T V(t)\,\mathrm{d}t$ is the *injected* flux for T period, μ_v is the average dopant mobility and β=$\frac{R_{OFF}}{R_{ON}}$.

C. Write/read timing requirement and logic state definition

To ensure that an ideal logic state is written, an ample write time (T_w) is required; it is expressed as follows [11].

$$T_w = \left| \frac{\phi(t)}{V_w R_{OFF}^2} \times (R_{OFF}^2 - R_{ON}^2) \right| \tag{3}$$

where $\phi(t)$=$\frac{(\beta D)^2}{2\mu_v(\beta-1)}$ is the *effective* flux for $0<D\leq 1$ and V_w is write voltage. Based on the memristor model specifications such as R_{ON}=100Ω, R_{OFF}=100kΩ, D=3nm, u_v=$3\times10^{-8}\mathrm{m^2v^{-1}s^{-1}}$ and V_w=1.5V [11], [12], write time T_w=100ns is obtained. On the other hand, read time is set to 20ns; this short time is set to alleviate too much change in the memristor internal state that might lead to soft errors [11].

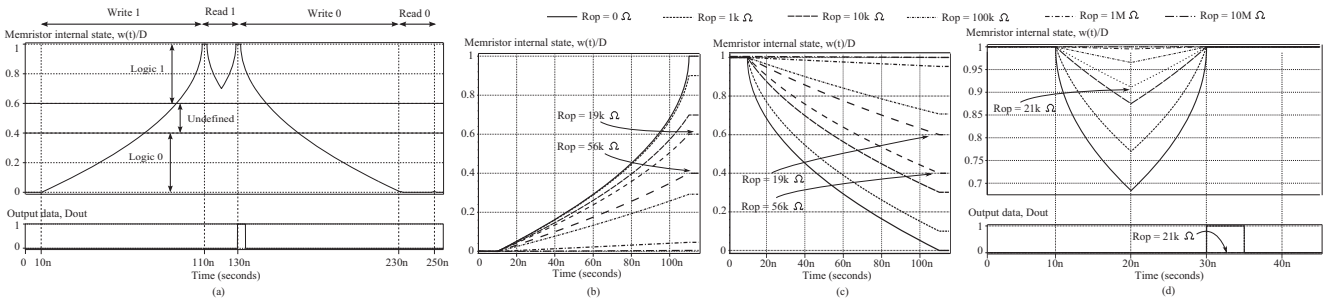

Figure 6. (a) Defect-free cell behavior under write and read operations of logic 1 and 0 (b) open-resistive cell behavior under $0w1$ operation (c) open-resistive cell behavior under $1w0$ operation (d) open-resistive cell behavior under $1r1$ operation

Fig. 5(d) shows the control signal timing for write 1, read 1, write 0 and read 0 operations. At t=10ns, the *Write/read enable (WRE)* signal is set to initiate a write operation; at the same time, *Input data* of logic 1 sets *nanowire word line (NWL)* voltage to 1.5V and *nanowire bit line (NBL)* voltage to 0V. Subsequently, from t=110ns to 130ns, the WRE signal is reset for read operation. During this read operation, NWL voltage with value of $-$1.5V is applied from t=110ns to 120ns followed by 1.5V from t=120ns to 130ns. The *Sense amplifier enable (SE)* signal is activated from t=120ns to 130ns for sensing the read current. In a similar way, write and read operations are performed for logic 0; the only difference is that for write 0 operation, NBL voltage is set to 1.5V and NWL voltage is set to 0V.

For write/read data integrity purpose, the logic state definition as proposed in [11] is used in this paper. Logic 1 is defined for $0.6 \leq \frac{w(t)}{D} \leq 1$; whereas logic 0 is defined for $0 \leq \frac{w(t)}{D} \leq 0.4$. A safety margin $0.4 < \frac{w(t)}{D} < 0.6$ is set as undefined logic state.

V. Case Study: Single-cell open defects

This section presents a case study for open defects that impact the behavior of a single cell. Open defects are of interest in this paper because these defects occur most frequent in deep sub-micron circuits [17], and it is expected that the situation will be the same for hybrid nanoscale circuits as well. In the rest of this section, first the simulation methodology will be explained, then the simulation results for defect-free memory will be presented. Thereafter, the simulation results of open defects and their analysis will be provided.

A. Simulation Methodology

Before performing defect injection and circuit simulation, the used simulation model has to be verified. Therefore, a defect-free simulation has been performed using the sequence S=$w1, r1, w0, r0$; $w1(w0)$ denotes a write $1(0)$ to the cell under consideration, while $r1(r0)$ denotes a read operation with the expected value $1(0)$. The sequence S is applied after initializing the cell to 0.

Next, a test of defects to be simulated is selected. The opens considered for this simulation are open within memory cell *OC*, open at nanowire word line *OW*, open at nanowire bit line *OB*, open in short via *OSV* and open in tall via *OTV*.

It is worth noting that the values of the open resistance R_{op} are assumed to be $0\Omega \leq R_{op} \leq \infty\Omega$. Each time a single open is injected in the SPICE memory model and the simulation is performed. The considered memory operations are restricted to the following sequences:

- $0w1$ – write 1 to a cell initialized to 0.
- $1w0$ – write 0 to a cell initialized to 1.
- $1r1$ – read an expected value 1 from a cell.
- $0r0$ – read an expected value 0 from a cell.

B. Defect-free simulation result

Fig. 6(a) shows the defect-free simulation results of the sequence S=$w1, r1, w0, r0$. The figure consists of two graphs; the top graph shows the internal state of the cell and the bottom graph depicts the output data value sent to data register after sensing the sense amplifier.

From t=10ns to 110ns, the write voltage causes $\frac{w(t)}{D}$ to increase from 0 to 1. At t=110ns, the ideal logic 1 has been written and stored. Subsequently, from t=110ns to 130ns, a read operation is performed. Due to the alternating read voltage, $\frac{w(t)}{D}$ decreases from 1 to 0.64 (from t=110ns to 120ns) and thereafter it increases to the original state at t=130ns. Note that during the read operation, the nanowire word line of the cell is put to two different voltage values; in the first half to $-V_{dd}$ and in the second half to $+V_{dd}$; see Fig. 5(d). During the second half of the read operation, the read current is sensed, converted to voltage and amplified. At t=130ns, the read voltage is sent to the output data buffer. During write 0 operation, $\frac{w(t)}{D}$ reduces from 1 to 0 putting the cell in logic state 0.

C. Open defect simulation results

Fig. 6(b) shows the simulation results of $0w1$ sequence for different R_{op} values injected within the cell initially set to logic 0. It shows that the maximum value of the internal state at the end of write operation decreases as R_{op} increases.

Table II
OBSERVED FUNCTIONAL FAULT MODELS DUE TO OPEN DEFECTS IN MEMORY CELL ARRAY

Open resistances (Ω)	**Faulty behaviors**	**Fault models**
R_{op}>21k	The cell returns an incorrect logic value by a read 1 operation; the stored value corresponds to logic 1	IRF_1
19k<R_{op}≤56k	The cell is set to an undefined state by a write 1 operation; the stored value corresponds to arbitrary logic	UWF_1
R_{op}>56k	The cell fails to undergo an up-transition (down-transition) when write 1 (write 0) is performed	TF_1 (TF_0)
19k<R_{op}≤56k	The cell is set to an undefined state by a write 0 operation; the stored value corresponds to arbitrary logic	UWF_0
R_{op}>10M	The cell always stores logic 1 (logic 0)	SAF_1 (SAF_0)

When 19kΩ<R_{op}≤56kΩ, the cell enters an undefined state since 0.6<$\frac{w}{D}$<0.4. When R_{op}>56kΩ, $\frac{w}{D}$≤0.4 meaning that the write operation fails to set the defective cell to logic 1. The same faulty behaviors are observed when the open resistances are injected at NWL.

Fig. 6(b) shows the simulation results of $1w0$ sequence for different R_{op} values injected within the cell initially set to logic 0. It clearly shows that depending on the defect value, the cell may fail to undergo a down write transition or enter the undefined state. The same faulty behaviors are observed when the open resistor R_{op} are injected at NWL.

Fig. 6(b) shows the simulation results of $1r1$ sequence for different R_{op} values injected. The figure shows that the victim cell returns an incorrect logic value while keeping the correct stored data when R_{op}>21kΩ. The same faulty behaviors are observed when the open resistor R_{op} are injected at NWL.

The sequence $0r0$ has also been performed for both opens within the cell and at NWL, and the results show no faulty behavior.

It is worth noting that due to the symmetrical structure of the memory cell (see Fig. 1), it is not required to perform the simulation for all opens in order to derive the faulty behavior. For example, an open at NBL has a similar faulty behavior to that of an open at NWL as well as an open at tall CMOS-to-nano via.

D. Simulation analysis

The observed faulty behaviors of the victim cell are summarized in Table II including the open resistance values and corresponding fault models. The analysis shows that not only the traditional memory fault models such as *Transition Faults* (TF_1 and TF_0), *Stuck at Faults* (SAF_1 *and* SAF_0) and *Incorrect Read Faults* (IRF_1) [8] exist, but also new unique ones. The new unique ones are:

- UWF_0 – The cell is set to an undefined state by a write 0 operation.
- UWF_1 – The cell is set to an undefined state by a write 1 operation.

These faults cause the victim cell to store an arbitrary value, either logic 1 or 0. The defects that induce such faults are hard to detect with only a write and read sequence. Special design for testability scheme may be required; this is an ongoing work.

VI. CONCLUSIONS

The paper presented a framework of defect oriented testing in hybrid CMOS/memristor memory. After giving the classification and definition of the defect, the electrical model of the memory developed for defect injection and circuit simulation was given. A case study of open defects at cell array and CMOS-to-nano vias has been demonstrated. The simulation results show that in addition to the occurrence of conventional semiconductor memories faults, new faults take place. For example, the cell holds an undefined state. This new faults will require new test approaches (e.g., DfT) in order to be able to detect them.

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