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# On-demand tuning of charge accumulation and carrier mobility in quantum dot solids for electron transport and energy storage devices

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## Abstract

Assemblies of colloidal quantum dots (CQDs) are attractive for a broad range of applications because of the ability to exploit the quantum confinement effect and the large surface-to-volume ratio due to their small dimensions. Each application requires different types of assemblies based on which properties are intended to be utilized. Greater control of assembly formation and optimization of the related carrier transport characteristics are vital to advance the utilization of these materials. Here, we demonstrate on-demand control of the assembly morphology and electrical properties of highly crosslinked CQD solids through the augmentation of various assembly methods. Employment of electric-double-layer (EDL) gating on these assembly structures (i.e., an amorphous assembly, a hierarchical porous assembly, and a compact superlattice assembly) reveals their intrinsic carrier transport and accumulation characteristics. Demonstrations of high electron mobility with a high current modulation ratio reaching  $10^5$  in compact QD films and of a record-high areal capacitance of  $400 \mu\text{F}/\text{cm}^2$  in an electric-double-layer supercapacitor with very thin ( $<100 \text{ nm}$ ) QD hierarchical porous assemblies signify the versatility of CQDs as building blocks for various modern electronic devices.

## Introduction

Colloidal quantum dot (CQD) solids render flexible and low cost solution-processed materials with unique size-dependent properties. The small size of the individual constituent QDs leads to the quantum confinement effect of the carrier wavefunction, which is reflected in the size dependency of the electronic band gaps and the formation of discrete energy levels<sup>1</sup>. Furthermore, these CQDs have a sizeable surface-to-volume ratio. Therefore, these material systems are attracting attention for a broad range of applications that exploit these merits, which range from optical and optoelectronic devices (e.g., photovoltaics<sup>2–4</sup>,

photodetectors<sup>5</sup>, and light emitters<sup>6</sup>) to many other potential energy harvesting devices (e.g., thermoelectrics<sup>7,8</sup> and water splitting electrodes<sup>9</sup>) and energy storage devices (e.g., battery and supercapacitor electrodes<sup>10</sup>). Each device requires different types of nanocrystal assemblies based on which the merits will be exploited. The assembly requirements for devices that need high electronic coupling between the QDs can be significantly different from those that require high accumulated charge carrier density.

In most CQD assemblies, chemical posttreatments are necessary to remove the native insulating long-chain ligands and/or replace them with shorter organic/inorganic ligand molecules. These processes reduce the distance between the QDs and promote stronger electronic coupling, which is required for charge carrier transport. The most widely used method to perform this ligand exchange in the solid state is layer-by-layer spin-coating,

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which allows complete ligand exchange in each layer<sup>11,12</sup>. Together with blade coating<sup>13</sup>, this technique gives macroscopically homogeneous and smooth films. However, these films show nanoscale disorder stemming from crack formation due to the volume shrinkage and the constriction of the degrees of freedom with which QDs can move on the solid-state surface that occur upon ligand exchange. These kinds of assembly disorder hamper efficient carrier transport throughout the system. It is crucial to control the assembly structure of QDs to realize the prospect of creating artificial nanostructured assemblies of QDs that show both crystalline-like electronic and transport properties while maintaining the quantum confinement properties, which is still challenging to achieve.

From another viewpoint, quasi-disorder in some of the assemblies may promote better performance for some applications, such as battery electrodes<sup>14</sup>, supercapacitor electrodes, or other electrochemical cells<sup>15</sup>. The existence of controlled holes/pores in QD assemblies can lead to the formation of a high surface area. Furthermore, an individual QD itself has a large surface area-to-volume ratio, which increases with decreasing size of the QD. As a consequence, enhancement of interactions between the surface of semiconductor QDs and electrolytes or ions can be achieved, either as simple physisorption or even deep intercalation of the ions into the QDs<sup>14</sup>. Combining the small size of QDs as the building blocks with control of the porous surface structures when fabricating assemblies can have a multiplier effect in significantly enhancing the performance of electrochemical cells.

Here, we demonstrate on-demand control of thin-film formation of highly crosslinked colloidal QD solids through the optimization of different deposition methods that directly influence the electrical properties of the solids for their potential use as charge transport and charge accumulation materials. We examine the formation of QD assemblies by three different deposition methods: (i) conventional layer-by-layer spin-coating; (ii) a layer-by-layer slow dip-coating method; and (iii) assembly at a liquid/air interface, which result in different assembly morphologies (Fig. 1a). To evaluate the correlations between the assembly structures and their electrical properties, we employ field-effect transistors (FETs) with two different types of gating structures: (i) a conventional solid-state oxide gate, on which the QD assemblies were deposited or transferred; and (ii) an electric-double-layer (EDL) gate using an ionic liquid as the dielectric, which was placed directly on top of identical QD assemblies. Correlations between the assembly structures and interactions at the QD-assembly/gate interface that affect the resultant electron transport and charge carrier accumulation behavior are significantly observed. The hierarchical porous structure of the dip-

coated assemblies displayed high carrier density accumulation comparable to state-of-the-art supercapacitor electrodes<sup>16</sup>, despite only exhibiting modest in-plane carrier transport. In contrast, the compact and well-arranged QDs in the liquid/air interfacial assemblies presented high carrier mobility across the assembly plane due to the minimized amount of disorder and the stronger inter-QD couplings. Lead sulfide (PbS) QDs were used as model materials due to the well-established synthesis process with a narrow size dispersion, the large Böhrradius, and the high abundance of the raw material<sup>17</sup>.

## Materials and methods

### Preparation of QD assemblies

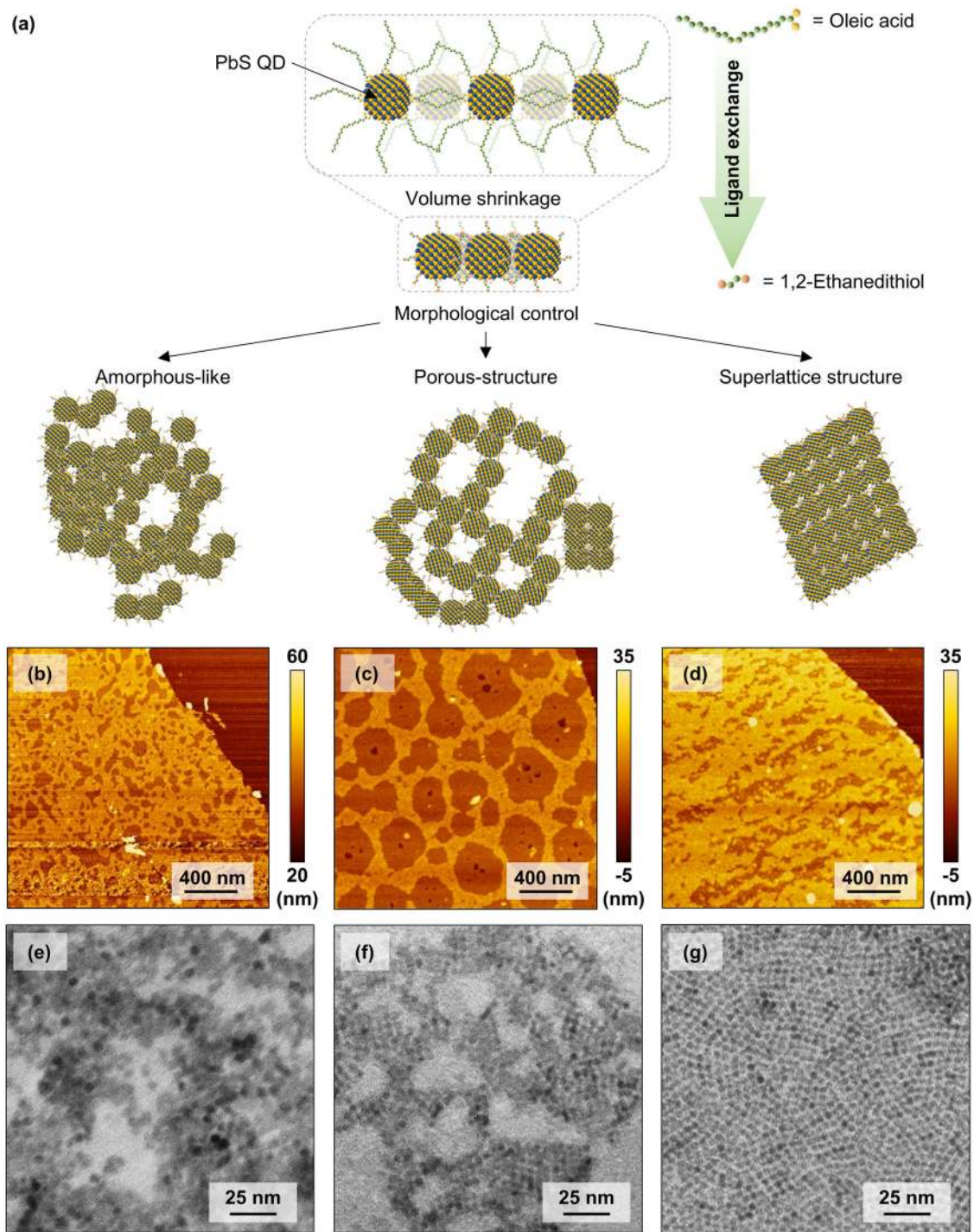
First, we optimized and evaluated the formation of QD assemblies obtained from each method. These assemblies consisted of PbS QDs with a size of  $4.0 \pm 0.7$  nm (see Section A and Fig. S1, Supplementary Information, for the synthesis procedures).

### Spin-coating deposition

For layer-by-layer deposition by the spin-coating method, we followed the well-established procedure, in which ligand exchange is performed with optimized parameters on each QD monolayer (see Fig. S2a, Supplementary Information)<sup>11,12,18</sup>. PbS QD droplets from a 5 mg/ml colloidal solution in chloroform were spin-coated at 4000 rpm on top of a SiO<sub>2</sub>/Si substrate. A 1% v/v 1,2-ethanedithiol (EDT) solution in acetonitrile (ACN) was dropped onto a deposited monolayer of PbS QDs for 3 min to replace the native oleic acid (OA) ligands. The film was then spin-dried at 4000 rpm. Methanol (MeOH) was used to remove any remaining excess ligands and residue on the assembly. The processes were repeated depending on the number of desired monolayers. The final thin film was then baked at 100 °C for one hour to remove any residual solvents. All processes were performed inside a N<sub>2</sub>-filled glovebox (Tr-O<sub>2</sub> < 1 ppm; Tr-H<sub>2</sub>O < 1 ppm).

### Dip-coating deposition

We optimized the dip-coated assembly by adapting prior works<sup>19</sup>, with several critical modifications due to the necessity of conducting a ligand-exchange process for each deposited layer (Fig. S2b, Supplementary Information). The dip-coating process was performed using a dip coater that can perform dips, withdraws, and horizontal translations as slow as 1 nm/s and that supports multiple-barrel operation (NanoSDI ND-0407-SP). Three containers made from polytetrafluoroethylene (PTFE) were prepared to accommodate 7 mg/ml PbS CQDs in toluene, 1% v/v EDT in ACN, and anhydrous MeOH. One cycle of dipping consisted of vertical substrate immersion in the colloidal PbS QDs and EDT solution for ligand exchange,



**Fig. 1 Morphology controls of QD assemblies by deposition method variations.** **a** Schematic of works in which the morphology of ligand-exchanged colloidal quantum dot (CQD) assemblies can be controlled by varying the deposition methods to produce amorphous-like assemblies, hierarchical porous assemblies, and compact superlattice structures. **b** Comparison of atomic force microscopy (AFM) images of the first deposited monolayers of 1,2-ethanedithiol (EDT)-treated PbS QDs prepared by spin-coating, **c** dip-coating, and **d** liquid/air interfacial assembly. Transmission electron micrographs (TEM) of the QD assemblies made by the three different methods: **e** spin-coating, **f** dip-coating, and **g** liquid/air interfacial assembly. These three different deposition methods result in different assembly morphologies. The high magnification TEM images (inset figures) show the distances between individual QDs, which are in the range of 0.5–0.9nm. These distance values imply attachment of the shorter EDT ligands and removal of the native oleic acid ligand.



followed by in MeOH for cleaning, sequentially. The optimum withdrawal speed of the substrate from the PbS QD batch was found to be 50  $\mu\text{m/s}$ . Ligand exchange in the EDT solution was performed for 3 min. After repeating the whole cycle depending on the desired thickness, the completed film was baked at 100 °C for one hour.

#### **Liquid/air interfacial assembly**

We adapted the reported liquid/air interfacial assembly method that demonstrated directed assemblies assisted by selective stripping of the native ligands<sup>20–22</sup>, with some modifications for ligand exchange optimization (Fig. S2c, Supplementary Information). A specially designed PTFE bath was prepared for the assembly process. Depending on the intention, either ACN or ethylene glycol (EG) was used as the “liquid substrate.” Four microliters of a PbS QD solution in hexane (2.5 mg/ml) was dropped on top of the “liquid substrate”. The PTFE container was immediately closed by a glass plate to decrease the evaporation rate of the hexane. After 2 min, 4  $\mu\text{l}$  of a 2 M EDT solution in tetrahydrofuran was injected into the “liquid substrate” to initiate ligand exchange. The QD assembly became a crosslinked monolayer film on the “liquid substrate.” After 3 min, the formed PbS QD assembly was transferred to the substrate by draining the “liquid substrate” using a hermetically connected syringe at the bottom of the PTFE bath. The QD assembly then soft-landed on top of the substrate placed at the bottom of the bath. The deposited assembly was then washed using MeOH and baked at 100 °C for one hour to remove any residual solvents.

#### **Film morphology characterizations**

Atomic force microscopy (AFM) images were acquired using a Hitachi AFM 5100 N in tapping mode (DFM mode). The QD assemblies were prepared on a 500 nm Si/SiO<sub>2</sub> substrate to match the conditions in the devices. Transmission electron microscopy (TEM) images were collected using a JEM-1230 apparatus (JEOL). For deposition of the QDs, TEM grids were mounted on Si/SiO<sub>2</sub> substrates similar to those for the AFM samples. The distance among the QDs was analyzed using ImageJ (National Institutes of Health, USA) (>100 data points each and magnification of 400,000 $\times$ ).

#### **Transistor fabrication and measurements**

We then evaluated the influence of the morphology variations on the electron transport properties by using FET measurements.

#### **SiO<sub>2</sub> solid-gating FETs**

Transistors were fabricated on 230 nm SiO<sub>2</sub>/Si substrates (SiO<sub>2</sub> capacitance = 15 nF/cm<sup>2</sup>) with lithographically patterned interdigitated Au (30 nm) electrodes

with channel widths and lengths of 1 cm and 20  $\mu\text{m}$ , respectively. The substrates for spin-coated samples and dip-coated samples were pretreated using 3-mercaptopropionic acid (3-MPA) to promote better adhesion. For the spin-coated and dip-coated samples, we performed five cycles of spinning and dipping, completed by ligand exchange in each cycle. For the FET with the liquid/air interfacial assembly, the film was deposited via a one-time transfer process. The transistor performance was evaluated at room temperature and in the dark using a low-noise probe station, which was located inside a N<sub>2</sub>-filled glovebox and connected to a semiconductor device analyzer (Keysight B1500A).

#### **EDL Transistors**

To fabricate EDLTs, we dropped 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide ([EMIM][TFSI]) ionic liquid (Sigma Aldrich) on the solid-gated transistor channel, covering the QD film in a specific area, followed by placing platinum foil on top of the ionic liquid. Before application, the ionic liquid was extensively dried to avoid a protic effect on the gating<sup>23</sup>. A tungsten probe was inserted to measure the potential drop due to the formation of an EDL ( $V_{\text{REF}}$ ). Measurement of the transfer curve was performed at a low drain voltage (50–200 mV) with a scan rate of 50 mV/s. The carrier density value was deduced from the gate displacement current measurement (DCM) of the same devices, in which their drain and source electrodes had been shorted to form an EDL capacitor.

#### **Electric-double-layer capacitor fabrication and measurements**

To clarify the impact of the assembly morphology on the amount of carrier accumulation, we performed another comparison via cyclic voltammetry (CV) measurement of the corresponding electric-double-layer capacitors (EDLCs), in addition to DCM. The PbS QD electrodes of the EDLCs were prepared using the same procedures as for fabricating FET devices (spin-coating: five spinning cycles; dip-coating: five dipping cycles; and liquid-air interfacial assembly: two monolayers of QDs) with a 1  $\times$  1 cm<sup>2</sup> active area on 1  $\times$  1.5 cm<sup>2</sup> cleaned FTO substrates. [EMIM] [TFSI] was then dropped on top of the QD assemblies, followed by 1  $\times$  1 cm<sup>2</sup> platinum foil as the counter electrode (CE).

Electrochemical characterization was performed by using a potentiostat galvanostat (VersaSTAT 4, AMETEK Scientific Instruments) with a two-electrode configuration. The working electrode (WE) and sense electrode (SE) probes were connected to the FTO (on which the QDs were assembled). The CE and reference electrode (RE) probes were attached to the Pt foil. The EDLC

devices were scanned over a bias voltage from  $-1.5$  to  $1.5$  V with a scan rate of  $10$ – $500$  mV/s.

Electrochemical measurement with the three-electrode configuration was also conducted.  $\text{Ag}/\text{Ag}^+$  was used as the reference electrode, and a  $2$  M [EMIM][TFSI] solution in ethyl acetate was used as the electrolyte. CV measurement was performed from  $-1$  to  $1$  V with a scan rate of  $10$ – $500$  mV/s. Potentiostat-mode electrochemical impedance spectroscopy (EIS) was also performed with a root-mean-square voltage ( $V_{\text{rms}}$ ) of  $10$  mV and scanning from  $1$  MHz to  $1$  mHz.

## Results and discussion

### Morphological control and assembly formation

Figure 1b shows the typical morphology of the spin-coated first layer of a PbS QD assembly, with EDT replacing the native OA ligands. One spin-coating cycle and the subsequent ligand exchange result in one QD monolayer with patches of a second QD monolayer. The electron micrographs of these monolayers (Fig. 1e) show a holey amorphous-like assembly. The average interdot distance is found to be  $1.3 \pm 0.4$  nm (edge-to-edge) (Fig. S3c, Supplementary Information), which is a factor-of-three longer than the length of the EDT molecule ( $l \approx 0.45$  nm). Since the solid substrate constricts the QD degrees of freedom during the volume shrinkage of the whole film, glassy amorphous-like structures are commonly obtained with patches of cracks or holes. The general observation of any spin-coated films suggests that ligand exchange alone is not enough to organize the whole assembly, and the original assembly order before ligand exchange plays a more critical role.

The slow withdrawal speed and the gradual evaporation rates in the dip-coating technique are expected to produce ordered structures better than the spin-coating technique. Among the parameters found to be crucial for the assembly of the QDs, the withdrawal speed of the substrate from the QD colloids is the most significant one affecting the assembly structures (Fig. S4, Supplementary Information). A low withdrawal speed provides sufficient time for nanoparticles to self-assemble on the substrate with a close-packed hexagonal structure (Fig. S3d, Supplementary Information), consistent with previous works using large nanoparticles<sup>24</sup>. Other parameters, i.e., the QD solution concentration and OA density on the QD surface, are found to be less critical.

We observed hierarchical porous structures in the assemblies deposited by dip-coating (Fig. 1c). This porous structure formed even under the most optimized parameters for the formation of the QD assembly. Nanoscopically, as shown in Fig. 1f, the dip-coated assemblies of QDs are more organized than those prepared by spin-coating. The distances among the individual QDs are smaller than those in the spin-coated assemblies, with an

average value of  $0.8 \pm 0.2$  nm and a narrower distribution (Fig. S3f, Supplementary Information). In this dip-coating method, short-range domains of a well-ordered and holey porous assembly are established before the ligand-exchange process (Fig. S3d, Supplementary Information). Since the withdrawal speed was very slow ( $50$   $\mu\text{m}/\text{s}$ ), the QDs had enough time to diffuse onto the substrate surface and assemble more finely. As the deposited QD assembly started to be submerged into the short-ligand solution, the distance between the QDs in the assembly shrunk due to the substitution of the long OA by the short EDT. As a consequence, the final assembly has more pores on both the micrometer scale (Fig. 1c) and the nanometer scale (Fig. 1f).

In liquid/air interfacial assembly, the rearrangement of the QDs and the ligand exchange process can be governed more by the higher degrees of freedom of the QD movement in the solution and at the interface (Fig. S2c, Supplementary Information). From the viewpoint of the ligand exchange process, an assembly of floating QDs is more beneficial than an assembly on a solid-state substrate since the QDs will still have all of their degrees of freedom until the new ligands crosslink them. In the liquid/air experiment, we only focused on the optimized formation of one or two monolayers (Fig. 1d).

Figure 1g shows TEM images of the liquid/air interface-assisted PbS QD assembly, which display a well-ordered assembly of PbS QDs with a more compact formation. The average edge-to-edge distance between the QDs is found to be approximately  $0.8 \pm 0.1$  nm (Fig. S3i, Supplementary Information). According to detailed observation, before ligand exchange, the self-assembly of the oleic-acid-capped PbS QDs formed a hexagonal structure, which can be observed for all deposition methods, as depicted in Fig. S3a, S3d, and S3g (Supplementary information) for spin-coating, dip-coating, and liquid/air interfacial assembly, respectively. However, the ligand exchange using EDT transformed the assembly into a predominantly square structure, similar to in the dip-coating assembly (Fig. 1f). This phenomenon is related to the facet orientation of the QDs, in which the ligand binding on the QD surface plays a role. Furthermore, the square structure of the assembly is driven by the interaction of the (100) facets among the individual QDs<sup>20,22,25,26</sup>. The movement of the QDs on the liquid surface could also be affected by the interaction between the ligand and the organic solvent itself. We also evaluated various organic solvents to control the self-assembly of the QDs. The utilization of EG led to a different assembly structure, which was an incomplete square structure in the form of a one-dimensional assembly (Fig. S5 Supplementary Information). This one-dimensional-like assembly can be attributed to the interaction among the (100) facets of the QDs along the

entire line with the (111) facets facing the solvent, as previously reported<sup>21,22</sup>.

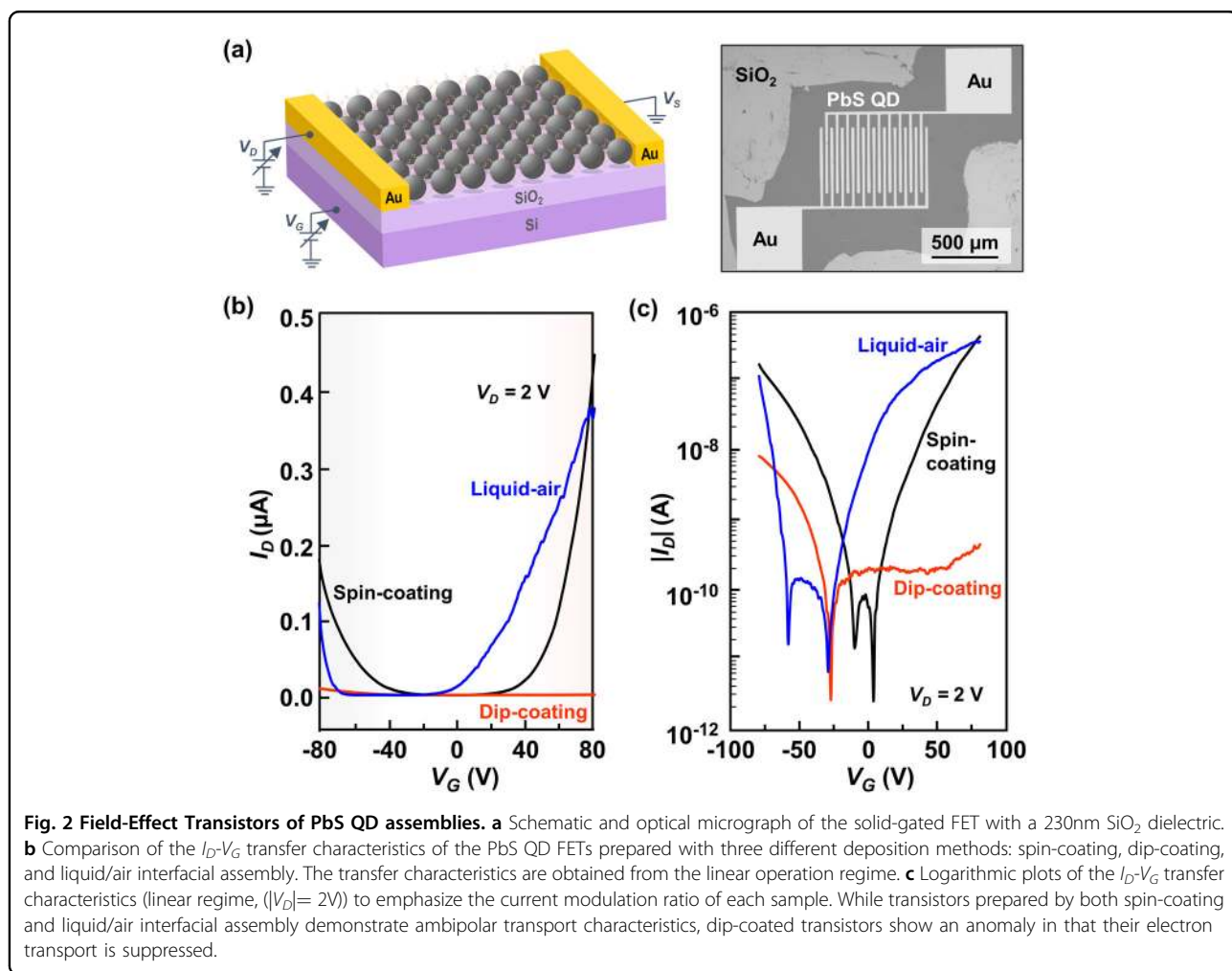
The abovementioned results infer that the formation of the QD assemblies under the different deposition methods resulted in efficient ligand-exchange and native ligand stripping processes, which can be examined via optical characterization of the formed assemblies by UV-VIS-NIR spectroscopy and Fourier transform infrared (FTIR) spectroscopy, as shown in Fig. S6 in the Supplementary Information along with the explanation. The main differences mostly lie in the morphology, where spin-coating led to an amorphous-like structure and dip-coating generated a porous assembly morphology, while, in contrast, the liquid/air interfacial assembly provided an assembly with a much more well-ordered structure.

**FETs of various QD assembly morphologies**

Conventional solid-gated FETs with the SiO<sub>2</sub>/Si gate structure and interdigitated Au electrodes were initially employed to examine the carrier transport of the assemblies (Fig. 2a). The FETs fabricated using the spin-

coating and dip-coating techniques comprise five-monolayer PbS QD assemblies, obtained from the five-cycle layer-by-layer processes. We decided to use this thickness because the morphology of the single deposited monolayer usually consists of large numbers of cracks and voids (Fig. 1), which the subsequent monolayers need to infill (see Fig. S7a–d in Supplementary Information). The five-monolayer film is known to be sufficient for reliable transport measurements<sup>12</sup>. In contrast, the FETs prepared with the liquid/air interfacial assembly consist of QD assemblies of only 1–2 monolayers. The dense and compact assembly of the film fabricated at the liquid/air interface has only minimal cracks. Thus, the carrier percolation in 1–2 monolayers is found to be adequate.

Figure 2b, c shows a comparison of the  $I_D$ - $V_G$  transfer characteristics of the PbS QD FETs fabricated by the spin-coating, dip-coating, and liquid/air interfacial assembly. The transfer characteristics of the FET with the spin-coated film demonstrate ambipolar transport characteristics with a high on/off ratio of more than 10<sup>3</sup>



for both charge carriers, consistent with previous reports<sup>11,12,27,28</sup>. Although the deposited film is much thinner, the FET with the liquid/air interface-assembled film also demonstrates ambipolar transport behavior with high on/off ratios for both electron and hole transport. This is the first demonstration of a solid-gated FET with liquid/air interface-assembled QDs that exhibits *n*-type electron transport. The threshold voltage for electron accumulation in the liquid/air interface-assembled FET is much lower than that in the spin-coated device. Furthermore, its subthreshold swing for hole accumulation is much steeper than that of its spin-coated counterpart.

However, the FETs with the film deposited by dip-coating performed differently. They demonstrate much lower electron and hole conductivities. These low conductivities are caused by the porous structure in this dip-coated sample, which is persistent even when the number of deposited layers (dipping cycle) is increased (Fig. S7e–h, Supplementary Information). Furthermore, the electron transport arm of the FET operation is entirely suppressed. This suppression of carrier transport in the semiconductor FET can be attributed to the formation of trap states at the semiconductor/SiO<sub>2</sub> interface<sup>29,30</sup>. This phenomenon also occurs in several PbS QD-based FETs<sup>18,27</sup>. The observation of distinct threshold voltage values for both hole and electron accumulation in these devices (Fig. S8, Supplementary Information) highlights the variations in the semiconductor/SiO<sub>2</sub> interface conditions for each type of assembly. The distinct ways of QD attachment to the substrate in the different methods modify the formation of trap states, particularly for electrons, at the QD/SiO<sub>2</sub> interface.

Quantitatively, the carrier mobility values of the SiO<sub>2</sub>-gate FETs were extracted from the slope of the  $I_D$ - $V_G$  transfer characteristics (Fig. 2b) in the linear operation regime ( $|V_{DS}| = 2$  V) (Fig. S9, Supplementary Information) using the textbook equation<sup>31</sup>. The FET with liquid/air interface-assembled QDs demonstrates electron mobility ( $\mu_e$ ) and hole mobility ( $\mu_h$ ) values as high as  $1.37 \times 10^{-2} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  and  $3.79 \times 10^{-3} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ , respectively. In contrast, the FETs with dip-coated assemblies can only show  $\mu_h$  as high as  $1.48 \times 10^{-3} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ , with a nonextractable electron mobility. The carrier mobility values in these liquid/air interface-assembled films and dip-coated films are found to be lower than those in the control spin-coated devices ( $\mu_e = 4.75 \times 10^{-2} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  and  $\mu_h = 6.49 \times 10^{-3} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ ), despite the better ordering of the QD assemblies. This finding indeed suggests that the charge carrier transport properties in the FETs with these QD assemblies are strongly affected by the trap states formed at the QD/insulator interface that can occur due to the different ways of QD attachment to the substrate.

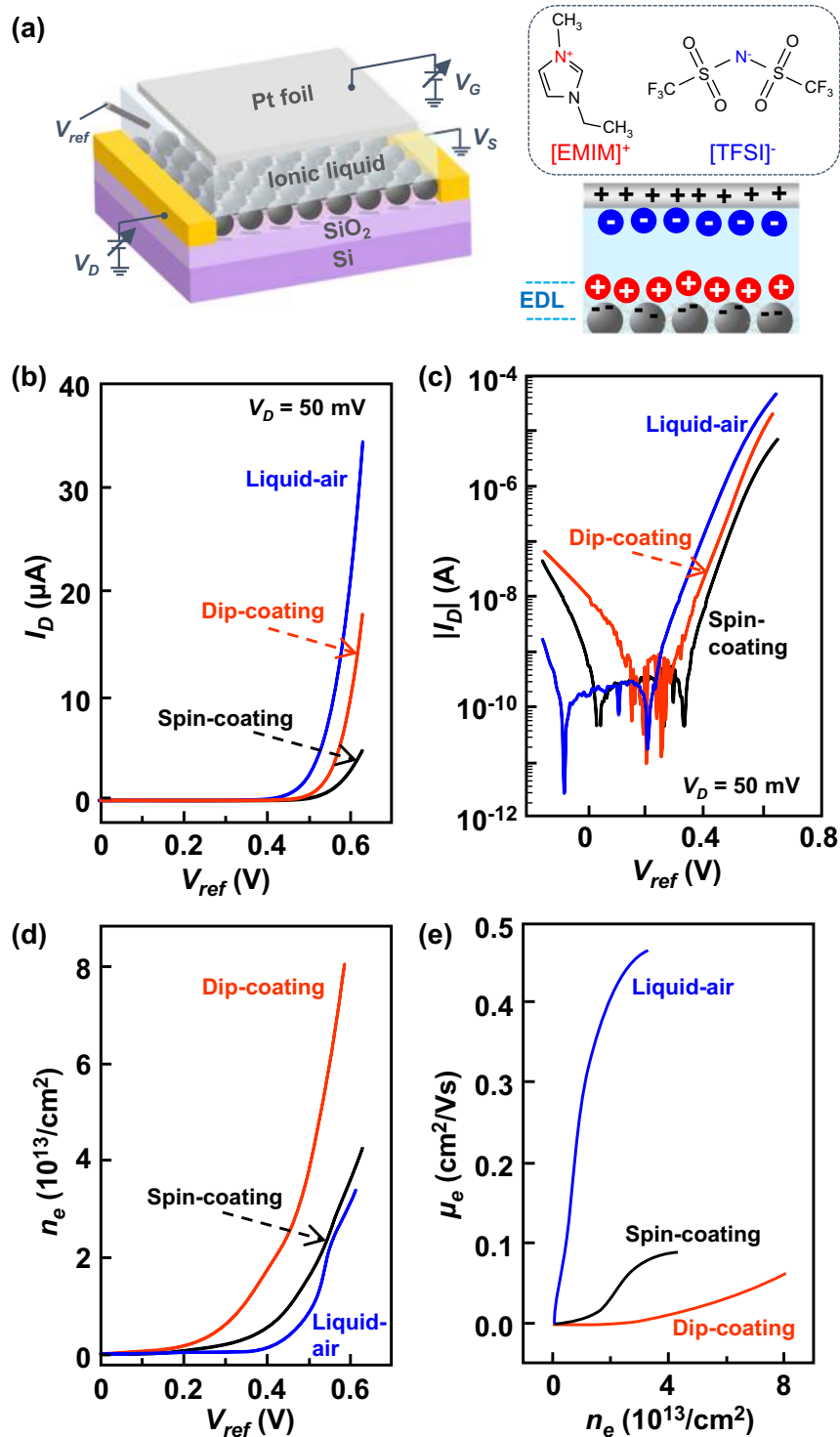
### Intrinsic planar charge carrier transport as probed by EDL transistors

To fairly compare the charge carrier transport properties of these assemblies, it is vital to minimize any external influence (i.e., interfacial trap states). To fill these states and intrinsically measure the charge transport, we employed the EDL transistor technique. The use of a liquid electrolyte (i.e., ionic liquid) promotes the formation of an EDL at the QD/electrolyte interface, which is analogous to a parallel plate capacitor with a molecular (1 nm) gap<sup>32</sup>. Therefore, a very high carrier density can accumulate on the QD assembly surface. This high carrier density accumulation (up to  $10^{14}/\text{cm}^2$ ) can fill most of the carrier trap states<sup>33,34</sup>. In particular, for these very thin QD monolayers, EDL gating is able to suppress the additional carrier traps that are formed at the interface between the assemblies and the oxide substrate<sup>12</sup>. Moreover, the liquid nature of the molten salt used as the electrolyte makes it behave as a conformational gate; thus, its gate coupling will be similar regardless of the morphological condition of the assembled films. The [EMIM] [TFSI] ionic liquid is used as the electrolyte gate<sup>12,34–36</sup> by placing it on the QD film channel of the identically bottom-gated FETs (Fig. 3a).

Distinct transistor properties emerge from the EDL gating measurements. Figure 3b shows a comparison of the  $I_D$ - $V_G$  transfer curves for the electron enhancement operation of the EDLTs that use spin-coated, dip-coated, and liquid/air interface-assisted QD assemblies as their active channels.  $V_{\text{REF}}$ , which represents the potential drop due to the EDLC, is used instead of the applied gate voltage  $V_G$  due to its stronger relevance for the quantification of the accumulated carrier density. The ambipolar transport behavior is evident in all EDLTs of different PbS QD assemblies, with all devices showing electron and hole injection with distinct linear and saturation regimes for both charge carriers (Fig. S10, Supplementary Information).

A substantial enhancement of electron transport is observed in the EDL transistor with the dip-coated QD assembly. This enhancement was not observed in the corresponding solid-gated FETs. The different electron transport behaviors in the dip-coated QD assemblies when measured with the two types of gating suggest that a large number of electron trap states formed at the interface between the SiO<sub>2</sub> and the dip-coated QD assemblies. The use of EDL gating filled these trap states. While one possible origin of these electron trap sites is the silanol end group of the SiO<sub>2</sub> surface<sup>37</sup>, it is unlikely to be the majority trap site due to the similar potential issues in the other kinds of assemblies and the total device processing in air-free conditions. These trap sites are strongly related to how the assembly formed and attached to the substrate. One of the potential mechanisms is that the porous





**Fig. 3 Electric-Double Layer Transistors.** **a** Schematic of an electric-double-layer transistor (EDLT) of PbS QDs using [EMIM][TFSI] ionic liquid as the electrolyte gate to probe the intrinsic carrier transport across different types of assemblies. **b** Comparison of the linearly plotted  $I_D$ - $V_{REF}$  transfer characteristics of the ionic-gated FETs with PbS QDs assembled by different methods, showing a gradual increase in the electron conductivity with the enhancement of the QD assembly order. **c** Logarithmic plot of the transfer characteristics to emphasize the current modulation ratios. Different from the observations of the solid-gate FETs, the EDLT with the dip-coated assembly demonstrates a substantial electron enhancement. **d** Comparison of gate-voltage-dependent electron densities accumulated by EDL gating of QD assemblies prepared by three different methods. The carrier density value was deduced from the gate displacement current measurement. **e** Carrier-density-dependent electron mobility of the three EDLTs. While the EDLT with the liquid/air interfacial assembly demonstrates the highest electron mobility, the transistor with the dip-coated QD assembly affords the highest maximum accumulated carrier density.



structure of the assemblies would allow relatively large numbers of QDs that possess dangling sulfur bonds to not undergo crosslinking by EDT, which can act as electron trap sites. In addition, the capillary effect in the dip-coating process may allow some free EDT molecules to adsorb into the assemblies and persist, acting as electron traps. Further clarification of the origin of the trap sites is still an important subject to be investigated.

The use of EDL gating also promotes enhancement of the on/off current modulation ratio of the transistors (Fig. 3c). Both EDLTs that used spin-coated and dip-coated QD assemblies demonstrate on/off ratios up to  $10^4$ . In contrast, the liquid/air interfacial assembly channel achieves the highest on/off ratio, including among other devices<sup>11,12,18,38</sup>, reaching more than  $10^5$ . Importantly, all devices show almost identical off-current levels with a distinct insulating region. Both spin-coated and liquid/air interface-assembled devices show similar widths of the insulating region. The dip-coated device has a narrower insulating area, which originated from the large number of trap states in this system for both charge carrier accumulations. The subthreshold swings for the electron side deduced from Fig. 3c are found to be 66.35, 68.49, and 67.33 mV/dec for the spin-coated, dip-coated, and liquid/air interfacial assembly devices, respectively. These values are close to that of the ideal trapless transistor<sup>39</sup>, which indicates the effectiveness of trap filling of the PbS QD assemblies by EDL gating.

We performed a displacement current measurement (DCM) to determine the accumulated charge carrier density due to the EDL gating<sup>11,32,34,38</sup>. Different from the conventional solid gate, the capacitance of the EDL gate strongly depends the applied gate voltage. The gate DCM was performed on identical transistor devices for each type of QD assembly (Fig. S11 and the explanation in the Supplementary Information). Figure 3d shows the carrier density versus  $V_{REF}$ , which was extracted from the DCM. Through the use of the [EMIM][TFSI] ionic liquid, we can accumulate electrons up to  $4.2 \times 10^{13}$ ,  $8.0 \times 10^{13}$ , and  $3.4 \times 10^{13} \text{ cm}^{-2}$  for the spin-coated, dip-coated, and liquid/air interfacial assembly devices, respectively. The highest carrier density accumulation was demonstrated for the dip-coated assembly, which has a porous structure. In contrast, the more compact liquid/air interfacial assembly is only capable of accumulating a much lower carrier density for the same applied  $V_G$ .

Utilizing the gate-dependent carrier density deduced from the abovementioned DCM measurement, the electron mobility in the planar direction of the channel can be estimated via Ohm's law<sup>34</sup>. Figure 3e plots the gate-dependent electron mobility versus the associated accumulated electron density of the three different EDLTs with different types of assemblies. The terminus of each plot is the maximum accumulated carrier density at the

same applied  $V_G$ . We obtained three distinct trends in these relationships. In the dip-coated samples, the charge carrier mobility continues to increase with increasing accumulated carrier density. In both the spin-coated samples and the liquid/air interface-assembled samples, the electron mobility increases and then plateaus in the vicinity of the maximum accumulated carrier density. The maximum electron mobility of each device was obtained to be as high as  $8.7 \times 10^{-2}$ ,  $6.3 \times 10^{-3}$ , and  $0.46 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  for the spin-coated, dip-coated, and liquid/air interfacial assembly devices, respectively.

The deposition methods of colloidal QD assemblies should be carefully selected depending on the applications that will be pursued. Different deposition methods give us not only different morphologies of the assembly but also different electronic characteristics. To prove that the morphology of the QD film deposited by the liquid/air interfacial assembly is more compact than those of the spin-coated and dip-coated assemblies, we performed similar EDLT measurements on two-monolayer spin-coated and dip-coated films (Figs. S12, S13 and the explanations in the Supplementary Information). The two-monolayer-thick spin-coated assemblies show a lower electron conductivity compared to their five-monolayer-thick assemblies (Fig. S13a, Supplementary Information). Conversely, the higher conductivity in the liquid/air interfacial assembly than in the spin-coated assembly shows the critical role of the assembly order in the electron transport in the two-dimensional plane.

On the other hand, the two-monolayer-thick dip-coated assembly shows suppressed electron transport due to the substantial leakage current (Fig. S13c, Supporting Information). This leakage current corresponds to the direct contact of the ionic liquid with the Au electrode, as it can deeply penetrate through the pores of the assembly. However, as the thickness of the dip-coated assembly is increased, this leakage current can be reduced (Fig. S12c, Supplementary Information), and the formed assembly is sufficient to simultaneously transport the electrons. Therefore, it has been shown that each deposition technique gives a different assembly structure for which a minimum thickness of the assembly is required to make the device work properly.

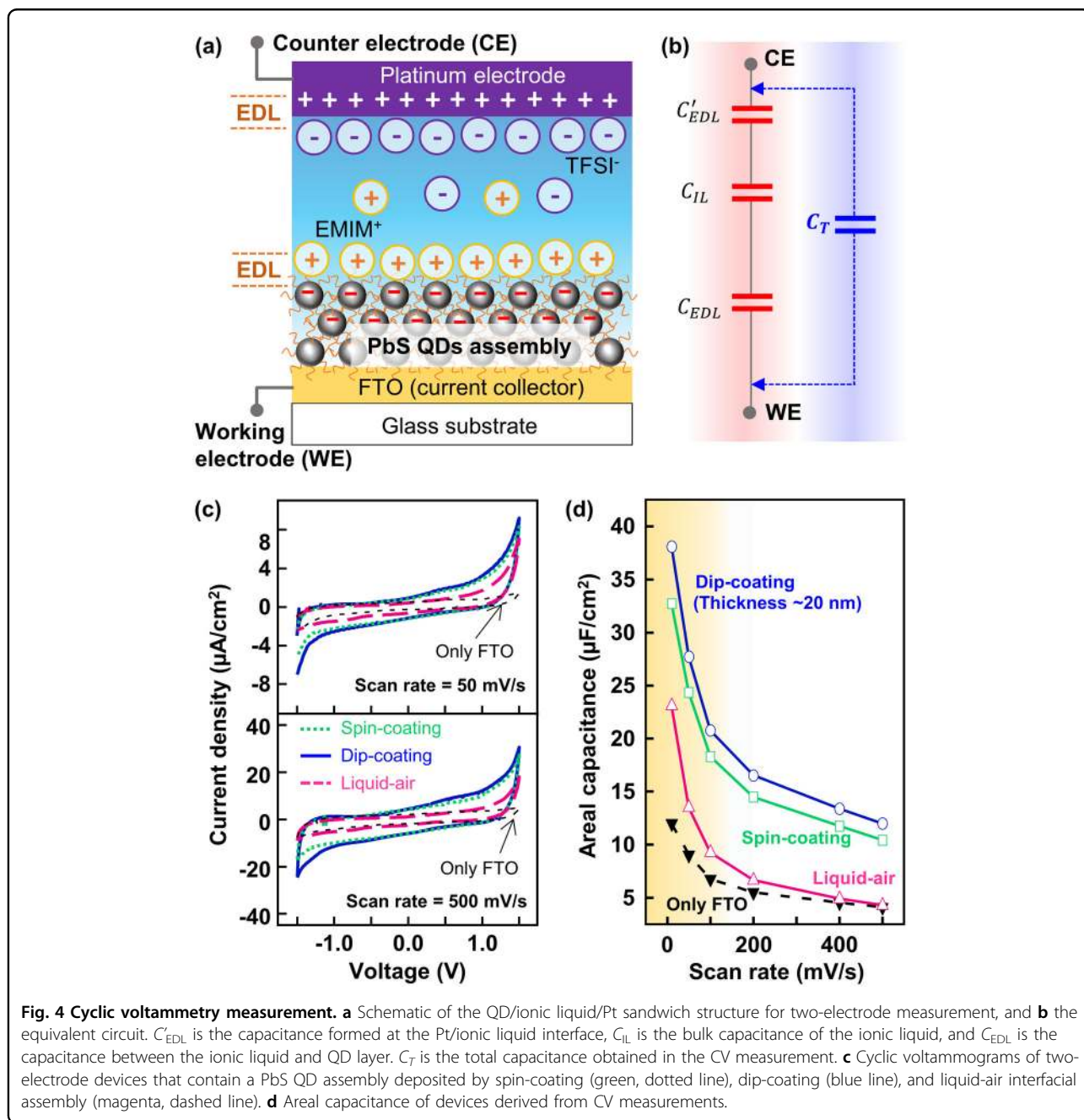
#### Capacitance measurement of QD assemblies by two-electrode cyclic voltammetry

While the porous assembly of the dip-coated film cannot provide the best example of a planar charge transport film, it offers a different figure of merit. Among the types of assemblies, it demonstrates the capability to accumulate the highest carrier density. To clarify the impact of the assembly morphology on the amount of carrier accumulation, we performed another comparison via CV measurement of the EDLTs, in addition to DCM with a

larger area of observation ( $1 \times 1 \text{ cm}^2$ ). For this purpose, we prepared a two-electrode EDL-capacitor structure that consists of PbS QD electrodes, [EMIM][TFSI] as the electrolyte and platinum foil as the CE (Fig. 4a). The equivalent circuit of the system, operating at low frequency (Fig. 4b), highlights the components contributing to the measured capacitance. The total capacitance value obtained from this CV measurement comprises contributions from two serial EDL capacitances (formed at the Pt/ionic liquid interface ( $C'_{EDL}$ ) and ionic liquid/PbS QD interface ( $C_{EDL}$ )) and the bulk ionic liquid capacitance

( $C_{IL}$ )<sup>32</sup>.  $C_{EDL}$ ,  $C'_{EDL}$ , and  $C_{IL}$  depend on the working frequency of the voltage sweep<sup>40</sup>. Additionally, the  $C_{EDL}$  at the PbS QD/ionic liquid interface is also affected by the quantum capacitance due to the sharp electronic density of states (DOS) of the PbS QDs arising from their low dimensionality.

Figure 4c shows the typical characteristics of EDL cyclic voltammograms with a symmetrical shape of the  $I$ - $V$  curve in the forward and backward scan directions. The areal capacitance ( $C_{areal}$ ), which is the volumetric capacitance per area of materials (electrode), for each scan rate



**Fig. 4 Cyclic voltammetry measurement.** **a** Schematic of the QD/ionic liquid/Pt sandwich structure for two-electrode measurement, and **b** the equivalent circuit.  $C'_{EDL}$  is the capacitance formed at the Pt/ionic liquid interface,  $C_{IL}$  is the bulk capacitance of the ionic liquid, and  $C_{EDL}$  is the capacitance between the ionic liquid and QD layer.  $C_T$  is the total capacitance obtained in the CV measurement. **c** Cyclic voltammograms of two-electrode devices that contain a PbS QD assembly deposited by spin-coating (green, dotted line), dip-coating (blue line), and liquid-air interfacial assembly (magenta, dashed line). **d** Areal capacitance of devices derived from CV measurements.

is estimated using:<sup>41</sup>

$$C_{\text{areal}} = \frac{1}{2(E_2 - E_1)\nu} \int_{E_1}^{E_2} j(E) \cdot dE \quad (1)$$

where  $E_2 - E_1$  is the applied bias window (in this case, 3 V),  $\nu$  is the scan rate, and  $\int_{E_1}^{E_2} j(E) \cdot dE$  is the integration of the  $I$ - $V$  curve. Thus, the dip-coated devices show the highest areal capacitance for the shown scan rate range, followed by the spin-coated devices and liquid/air interfacial assembly devices (Fig. 4d). At a low scan rate (below 100 mV/s), ions reach the surface of QDs and electrostatically interact. Because of this very strong electrostatic interaction (the formation of an EDL), the quantum capacitance ( $C_Q$ ) of the PbS QDs becomes more significant, thus enhancing the recorded total capacitance. In contrast, at a high voltage sweep rate, the bulk capacitance ( $C_{\text{IL}}$ ) starts to become dominant since the formation of an EDL on the surface of QDs is hampered<sup>32,40,42</sup>, so the obtained total capacitance decreases. Within the shown scan rate range, the  $C_{\text{EDL}}$  at the ionic liquid and PbS QD interface is the crucial factor that leads to the differences in the capacitance values of all the devices.

The formation of a hierarchical porous ultrathin PbS QD film significantly enlarges the surface area of the assembly to accommodate the formation of an EDL, resulting in the highest total areal capacitance of up to 40  $\mu\text{F}/\text{cm}^2$  at a voltage sweep rate of 10 mV/s (Fig. 4d). In contrast, the lowest  $C_{\text{areal}}$  was demonstrated by the liquid/air interfacial assembly devices. This result is consistent with the trend obtained from the DCM of the corresponding EDLTs. In this least holey structure, i.e., the liquid/air interface-assembled film, ions have difficulty penetrating deeper into the subsequent layers. Hence, the EDL formed only on the surface of the topmost QD assembly, resulting in a smaller area of the EDL interface<sup>43</sup>. These results highlight the strong relationship between the morphological structure and the formation of the EDL.

### Prospect of utilizing quantum dot assemblies as energy storage materials

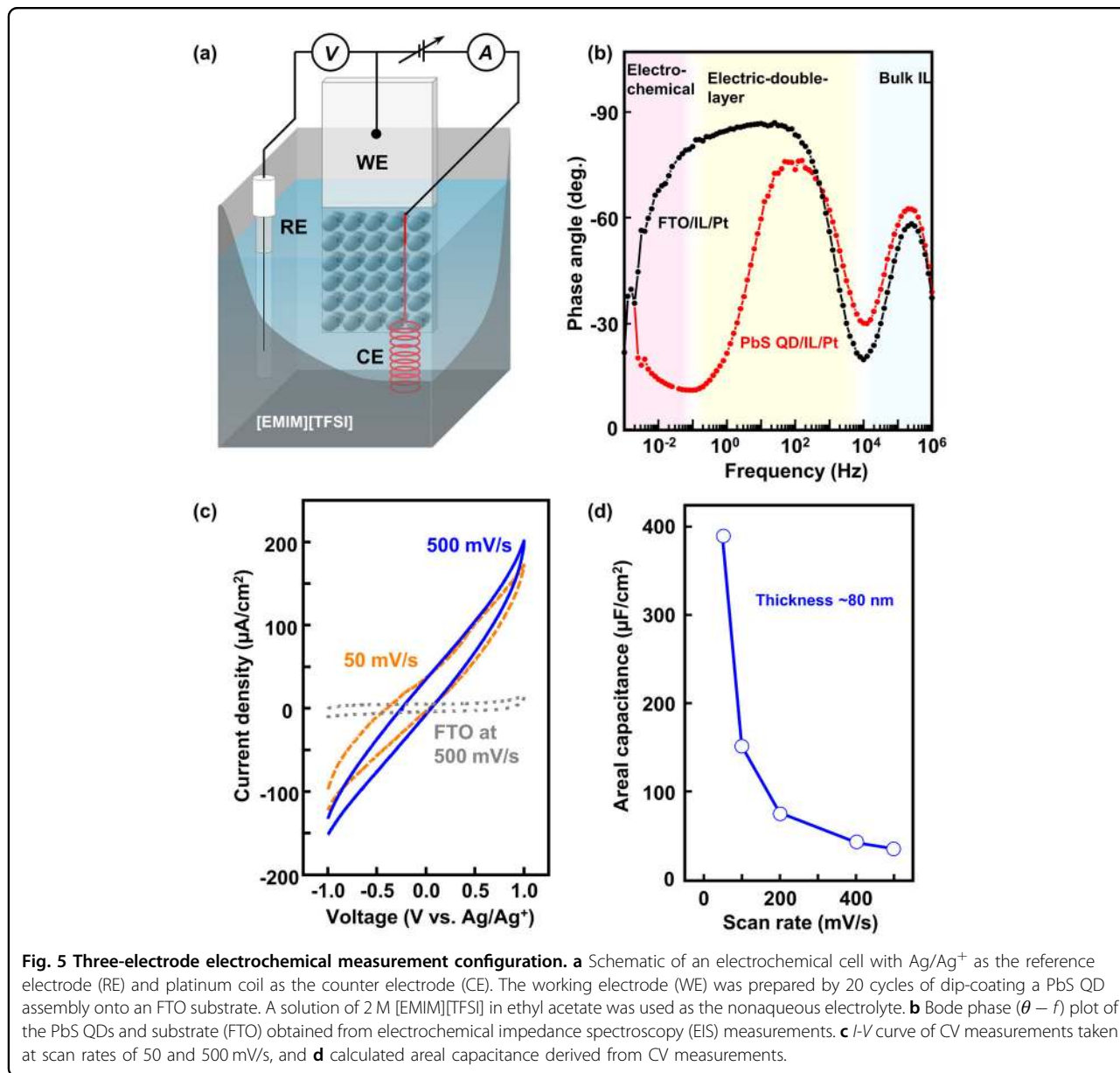
The high areal capacitance obtained for the above-mentioned hierarchical porous dip-coated assembly ( $C_{\text{areal}} = 40 \mu\text{F}/\text{cm}^2$ ) is comparable with that of graphene-based EDL supercapacitors<sup>44</sup> and some other reported state-of-the-art supercapacitors<sup>16</sup>, including those with ZnO nanocrystal electrodes<sup>10</sup>. Different from the other supercapacitor electrodes that consist of micrometer-thick films, the abovementioned PbS QD EDLC electrode consists of an only five-monolayer assembly (total thickness of less than 25 nm). The areal capacitance of EDLCs is expected to be proportional to the assembly thickness

because of their porous structure. The EDL capacitance depends on the surface area where ions make contact with the QD surface. Hence, this last part discusses the prospect of using a QD/IL combination for an energy storage device.

We performed capacitance measurements on a scaled-up dip-coated PbS QD assembly consisting of 20 deposited monolayers to demonstrate the influence of the assembly thickness on the areal capacitance. Half-cell analysis was conducted on the electrode by applying a three-electrode configuration, as illustrated in Fig. 5a. On the electrolyte side, we maximized the ionic conductance of the electrolyte by dissolving the IL into anhydrous ethyl acetate to reduce the viscosity. Although ionic diffusion can be improved, dissolving an IL in organic solvents will change its electrochemical windows<sup>45,46</sup>. Therefore, to demonstrate the boundary of the bulk EDL electrochemical regime in the IL-based electrolyte/PbS QDs, we performed EIS measurements.

Figure 5b shows the impedance phase based on the  $ac$  voltage response in the frequency domain (Bode phase ( $\theta$  -  $f$ ) plot) of an FTO/IL/Pt reference cell and the FTO/PbS QD/IL/Pt cell. From the oscillation in this Bode phase plot, we can distinguish different capacitive regimes in these cells. The large phase angle (in the negative direction) indicates a strong capacitive region. In the measurement of the FTO/IL/Pt reference cell (Fig. 5b, black line), two distinguishable capacitive regimes can be identified. The first is the bulk ionic liquid capacitive regime, in the fast charging region (10 kHz–1 MHz), which originates from the inter-cation-anion polarization in the bulk IL between the platinum electrode and the WE. The second is the very high capacitive behavior ( $\theta \approx -90^\circ$ ) at low frequency (1 mHz–10 kHz). The origin of this high capacitive regime is the formation of an EDL due to the electrode/IL interaction at the interface. In contrast, the PbS QD/IL/Pt (red line) shows a narrower EDL capacitive regime (0.1 Hz–10 kHz) with an additional feature in the lower frequency domain (below 0.1 Hz), which is attributed to the electrochemical reaction at the PbS QD/IL interface<sup>40</sup>. From this EIS measurement, we can determine the frequencies or the scan rates (in the CV measurement) at which the device still operates as a full EDLC. The applied scan rates of 50 mV/s up to 500 mV/s found to be within the EDL regime correspond to EIS frequency values between 0.9 and 9 Hz. This correspondence suggests that the applied scan rate in the CV measurement had minimal influence on any electrochemical reactions.

Furthermore, the symmetric  $I$ - $V$  curves in the CV measurement (Fig. 5c) are consistent with the typical two-electrode configuration result (Fig. 4c), signifying EDL formation. The current density for the charging process of this thick assembly is significantly higher than those of five-monolayer assemblies with pure IL. The extracted



$C_{\text{areal}}$  of this thick ( $\sim 80$  nm) assembly reaches  $\sim 400 \mu\text{F}/\text{cm}^2$  at a 50 mV/s scan rate (Fig. 5d). This result demonstrates that the hierarchical porous structure persists even for EDLCs with thicker films.

The use of CQDs as the building block of electrodes and the selection of an appropriate ionic liquid will further provide the capability to utilize the enormous quantum capacitance of the QD system by filling the discrete energy levels<sup>11,12,20</sup>. This would provide new strategies to design new types of supercapacitor electrodes. The present work still utilizes a lead chalcogenide (PbX) system, which contains a heavy element. However, once the properties of any other synthesized nanocrystals with lighter elements achieve a quality comparable to that of

the PbX system, the strategies presented here will be beneficial for their exploitation.

### Conclusions

In summary, we have demonstrated a strong relationship of the QD assembly morphology with the electrical properties. Different deposition techniques can generate various QD assembly structures, as shown for the spin-coating, dip-coating, and liquid/air interfacial assembly methods, which provided us with a variety of assemblies: amorphous-like, hierarchical porous, and compact well-ordered assembly structures. By employing EDLTs, the intrinsic electron transport in the planar direction of these structures was found to be strongly affected by the



structure of the assembly, as well as the influence of the various deposition methods on the charge trap state formation. At the same time, the charge carrier accumulations for the various assembly morphologies were also quantified. The high carrier accumulation in the dip-coated assembly due to the formation of a hierarchical porous structure promotes the potential utilization of QD films in energy storage applications (i.e., supercapacitor electrodes). A record-high areal capacitance of the EDLC built from a few-monolayer dip-coated QD assembly was demonstrated. On the other hand, when an adequate carrier mobility is required for many other electronic devices (i.e., FETs, solar cells, thermoelectric devices and photodetectors), the upscaling and stacking of the QD ultrathin film fabricated by the liquid/air interfacial assembly is vital. This on-demand morphology control of CQD assemblies plays an essential role in enabling further exploitation of the quantum confinement properties of QDs in many electronic device applications.

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#### Author contributions

S.Z.B., F.J., and Y.I. conceived the project; R.D.S. performed the experiments, especially fabrication of the quantum dot assemblies and devices, as well as performed measurements; S.Z.B. constructed most of the experimental setups; L.L. synthesized the colloidal quantum dots and contributed to some of the electron microscopy imaging; R.D.S. and S.Z.B. analyzed the data; R.D.S. and S.Z.B. wrote the manuscript with significant input from F.J., N.M., and Y.I.

#### Conflict of interest

The authors declare that they have no conflict of interest.

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