On Design, Cost and Reliability Analysis of a Fault-Tolerant Multistage Interconnection Network Layout with Six Disjoint Paths

Vipin Sharma (vipin.sharma224@gmail.com)
Jamia Millia Islamia
Abdul Q. Ansari
Jamia Millia Islamia
Rajesh Mishra
Gautam Buddha University
Gaurav Khanna
Jaypee Institute of Information Technology

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Abstract

Multistage interconnection networks (MINs) provide an efficient solution for communication between one or more processors and memory modules. These networks are suitable for computationally extensive applications. Although there exist a wide variety of fault-tolerant MIN designs, however there is always a scope of improvement in the design of MINs, which comes with challenges and trade-offs. More specifically there is always a need for fault-tolerant, reliable, and cost-effective designs of MINs, which can tolerate multiple switches and link failures. This always motivates a researcher to focus on various design options and architectural models to enhance performance of the MINs.Designing fault-tolerant MINs requires more disjoint paths from each source–destination (S-D) node pair capability to use all available paths effectively. This paper proposes a new MIN layout viz; 6DP-MIN, which provides six disjoint paths and 14/12 redundant paths for different S-D node pairs. This proposed 6DP-MIN is a modification of gamma interconnection network (GIN). Performance of the proposed design layout (6-Disjoint Path MIN) has been evaluated in terms of fault-tolerance capability, all available paths, reliability (two-terminal, broadcast, and network), and cost per unit. The results have been compared with other variants of GINs such as SEGIN, SEGLNIN, 3-Disjoint gamma interconnection network, 3- disjoint path multistage interconnection networks, and 4-DGINs. The results suggests that the proposed 6DP-MIN is highly fault-tolerant and reliable with regards to other MINs used for comparison.

1. Introduction

An interconnection network (IN) is a group of links and switching elements that connects one or more memory modules and processors for communication and computing purposes. For parallel and distributed systems, INs play an essential role in enhancing the distributed system's speed, efficiency, and computational power. Hence, IN is the heart of parallel systems. Thus, a well-designed IN is required to transfer data efficiently; otherwise,parallel systems negate the advantages of high speed, parallel processing and high computational power. Therefore, the design of INs has always been an active research area for parallel and distributed systems.

So far, many interconnection topologies have been presented [1], [2]. In these topologies, crossbar switches are used and arranged in different stages. Based on various topologies, classification of interconnection networks is shown in Figure 1. Arrangements of crossbar switches are recognized as multistage interconnection networks (MINs). MINs are a subset of interconnection networks (INs) which offer an efficient, low-cost, and attractive solution for the communication between memory modules and processors and interconnection among different system components. These MINs can be divided into two categories: single path and multipath. A single path MIN has only a single path between source and destination node pairs, while a multipath MIN has more than one path between each source and destination node pair.

Reliability is also an important parameter when designing a MIN. The reliability of a MIN [4] is the probability that a network work without failure for a predefined period and environmental conditions. There are various methods [3]such as the decomposition method [4], [5], reliability block diagram [6], continuous-time Markov chain (CTMC) [7], reliability bounds [8], [9], monte carlo simulation [10] are discussed by the researcher for evaluation of reliability. Besides reliability, fault tolerance is also an important parameter to determine the performance of MINs. Reliability also improves by improving the fault tolerance capability of the MINs.

Table 1: Comparison of various topologiesbased on their features.

	Bus	Crossbar	Multistage Interconnection networks
Speed	Low	High	High
Cost	Low	High	Moderate
Complexity	Low	High	Moderate
Reliability	Low	High	High
Configurability	High	Low	Moderate

Rest of the paper is divided as: Section 2 provides background and motivation for the present work, Section 3 explain the layout of proposed design (6DP-MIN), Section 4 includes performance analysis in terms of terminal reliability, network reliability and broadcast reliability evaluation (using SDP) and hardware cost for six 6DP-MIN, this part also presents a comparative table of performance metrics for 6DP-MIN, Section 5 is about the conclusion of this work, followed by references.

2. Background And Motivation

This section will provide brief overview of various fault-tolerant MINs which are existing in literature and motivation for present work

2.1 Background

Let us explore the importance of disjoint paths available in MINs. Literature has a variety of fault-tolerent MINs layout [11], [12],[13], [14]. These papers provides different performance parameters for designing of MINs for future generation parallel and distributed systems. Most of the discussion in MINs designing is centered towards the fault-tolerant capability of designs. The basic idea for the fault-tolerance of the MIN is to create more redundant paths between any (S-D) node pair so that redundant paths can be used when any switch gets failed. Fault tolerance in MINs [3], [11], [15] is achieved by many researchers using various methods like combining switching elements, increasing the number of stages, providing dynamic rerouting techniques between the stages, changing the interconnection patterns, increasing disjoint paths and backtracking, etc.

There are many other MINs like the Delta network [11], Omega network [12], Banyan network [14], Butterfly network [16], and many more, which provide single disjoint path between any S-D node pairs.

2.1.1 Two disjoints paths MINs

A large number of two disjoint paths MINs also exists in literature likes: Benes network[17], PHI network[18], PM22i interconnection network [19]. Various hybrid network of GIN also provides two disjoint paths for example Extra Stage GIN [20], Partially and Fully Chained GIN [19], and Balanced GIN [21] two disjoint paths network.

SEGINs [22] and SEGLNIN [15] are recently developed two disjoint path networks with fault-tolerant capability. SEGIN utilizes a shuffle exchange pattern with $n + 1$ number of stages here $n = \log_2 N$ and N is the number of inputs and outputs. In Fig. 2, a SEGIN of size 8x8 is shown.

Each stage has N/2 switching elements with a size of 2x2 at the initial and final stages, while 2x3 and 3x2 sizes switching elements exist at intermediate stages. SEGIN-1 and 2 are topologically different, but the reliability for both isthe same. SEGINs network provides two disjoint paths and three redundant paths for all tag values. SEGLNIN is obtained by slight modification in SEGIN. The connection diagram of 8x8 SEGLNIN is shown in Fig. 3.

Here, each stage has N/2 switching elements, and switch sizes are 2x2 at the first stage, 2x3 and 3x2 at the second and third stage, while the size of switching elements is 3x2 at the last stage. SEGLNIN provides two disjoint paths for each source and destination node pair, but the total number of paths is not uniform for all tag values; for some tag values, it has four paths, and in some cases, it has five paths.

2.1.2 Three disjoint paths MINs

There are various three disjoint networks also available in literature like three disjoint path MIN [23], 3DGIN [24], Pars network [25], 3DMIN [26]. These classes of MINs have multiple redundant paths, but they all have three disjoint paths for any S-D node pairs.

In [23], three disjoint paths MIN, which has shown in Fig. 4, is obtained by modification of GIN [8] and 3DGIN [24]. This MIN provides three disjoint paths for each source-destination node pair, but it has different paths for different tag values. Figure 4 represents a connection diagram of 8x8 size three disjoint path MIN with $\log_2 N + 1$ stages, here N is the number of inputs and outputs. It has an N/2 number of switching elements in each stage. Here, stages 0 and 3 have switches of switching sizes 2x3 and 3x2, respectively, while intermediate stages have switches of 3x3. For this network total number of paths for each source-destination node pairs are given in Table 2, switch number is represented by S-1,S-2 and so on respectively. but total disjoint paths for each source-destination node value is three. In [23],the two-terminal reliability of the network has been evaluated.Here we are calculating broadcast and network reliability also.

Table 2
Total number of paths for different S-D node pair values for three disjoint path MIN [23].

	Total num of paths for different destination value			
Source Value	S-13	S-14	S-15	S-16
S-1	7	7	6	7
S-2	7	7	7	6
S-3	6	7	7	7
S-4	7	6	7	7

To evaluate broadcast and network reliability of [23], calculate its broadcast path set and networks path set and calculate respective reliability using Matlab program using the sum of disjoint product with MVI technique. The result of these values is given in Table 6.

The connection pattern of 3DGIN is shown in Fig. 5,which is similar to the GIN at intermediate stage but at the initial stage where two switches of size 1x3 are combined into one switch of 2x4, and the rest of the stages are the same as GIN. In this network,three disjoint paths are available for all S-D. But total numbers of paths are different for different routing conditions. It provides 4 number of total redundant paths for routing condition [(S-D) mod 2] is odd (thick lines in Fig. 5 show example of this condition) otherwise 3 number of paths are available (dash lines in Fig. 5 show example of this condition). In [27], two-terminal reliability, all terminal reliability, and network reliability of the 3DGIN have been evaluated.

2.1.3 Four disjoint paths MINs

In contrast with all these MINs, four disjoint paths MINs which are present in literature are 4DGIN-1,2,3 [28], [29], and Reliable Interconnection Networks (RIN) [31] provide better performance in terms of fault tolerance and reliability.

Recently developed four disjoint paths MINs are 4DGIN-1,4DGIN-2 [28] and 4DGIN-3 [29]. The connection diagram of 4DGIN-1 is shown in Fig. 6(i), 4 DGIN-2 is obtained by reversing the 4 DGIN-1, and the connection diagram of 4DGIN-3 is shown in Fig. 6(ii).These three designs of 4DGINs having $\log_2 N + 1$ number of stages from 0 to n.Here $N = 2^n$,N is the number of inputs and outputs of the network. All these networks have the same architectural view but different connection patterns at various stages. In all three networks, the size of the switching element used in the first and last stage is 2x4 and 4x2, respectively, with intermediate stages having switch sizes of 2x3 and 3x2 (stage1 and stage 2). Here, 4 DGIN-1 and 2 have different paths for different tag values, but 4DGIN-3 has an equal number of paths for all tag values of source-destination node pairs explained in [29]. In [28] and [29], cost and reliability are analyzed, and the results are used in Table 6.

2.2 Motivation for Proposed design

Now, keeping past research in mind, existing MINs architectures are having single, double, and triple fault-tolerant capability and provides less number of disjoint paths. Some of the hardware designs are complex and required additional circuitry like mux, demuxand auxiliary links. Other important parameters for performance of MINs that should be focused in designing of MINs are reliability and cost effectiveness.Thus a fault-tolerant, reliable and cost effective designs of MINs always needed for parallel and distributed systems.

However, there is lack of papers investigating all types of reliability parameters, redundant paths, and disjoint paths. All terminal reliability and broadcast reliability need to be calculated for SEGLNIN and 3D-MIN.

3. Layout Of Proposed Design

In this paper, we proposed a 6DP-MIN whose connection pattern diagram for 8x8 size is shown in Fig. 7. The proposed design has (n + 1) number of stages, where $N = 2^n$. N is the number of inputs and outputs of the proposed network. The first and the last stage of the network have switches of sizes 2x6 and 6x2, respectively. This design is an irregular MIN because the number of switching elements are not equal in all stages. Here, stage 0 and stage 3 have N/2 number of switches while intermediate stages have N number of switching elements. Switch sizes at the first and last stages are 2x6 and 6x2, respectively, and switch sizes at the middle stages are 3x3.

The connection between the first two stages (stage 0 and stage 1) are based on interconnection pattern such that the *jth* switch (where *j* = 0,1,2,3) of stage 0 having six output links which are connected to the stage 1 as (a) the first link connected to the $2j-2$ switch, (b) the second link connected to $2j$switch of stage 1, (c) the third link connected to $2j+2$, (d) fourth link connected to $2j-1$, (e) the fifth link connected to $2j+1$, (f) the sixth link connected to $2j+3$ of stage 1 as shown in Fig. 8(i). In Stage 1 and 2 there are seven number of switches having the size of 3x3. These two stages are connected by (a) the first straight link directly connected to jth switch, (b) upward link is connected to $j-2$switch, and (c) downward link connected to$j+2$switch. If the calculated switch number is less than zero in the above cases, then eight is added to the number. It will give the switch number of the next stage if it comes greater than seven, then number 8 is subtracted to get the correct switch number of the next stage which is shown in Fig. 8(ii). In stage 2, the number of switches is seven, and in the last stage, there are four switches. Here each switch has three outputs. For an even number of the switch (*j=even number*), stage 2 is connected to stage 3 as (a) the straight link of the *jth* switch connected to the $\frac{j}{2}$ th switch of stage 3 (b) upward link connected to$(\frac{j}{2}-1)$th switch and (c) downward link connected to $(\frac{j}{2}+1)$th switch of stage 3. If the number of switch *j* is odd, then (a) straight link of the *jth* switch connected to $(\frac{j-1}{2})$th switch of stage 3 (b) upward link connected to $(\frac{j-1}{2}$ – 1)th switch and (c) downward link connected to ($\frac{j-1}{2}$ + 1)th switch of stage 3 is shown in Fig. 8(iii).

To represent the path between various S-D node pairs as shown in Fig. 7, each switch is numbered by 1 to 4 for stage 0, 5 to 12 stage 1, 13 to 20 stage 2, and 21 to 24 in the last stage. Here switches in the first stage will be source nodes, and the last stage is destination nodes. The numbers of total available paths for each S-D node pair are given in Table 3; with the help of this table, we conclude that the total number of disjoint paths for each S-D node pair is six.

Table 3
Total number of paths for different S-D Pairs for 6DP-MIN.

(S-D) node pair	Total available paths	Total number of paths	Disjoints Paths
(1,21)	[1-5- 13–21] ,[1-5- 15–21] ,[1- 5- 19–21], [1- 6- 14–21], [1- 6- 16–21], [1- 6- 20–21], [1- 7- 13–21], [1- 7- 15–21], [1- 8- 14–21], [1- 8- 16–21], [1- 11- 13–21], [1- 11- 19–21], [1- 12- 14–21], [1- 12- 20–21]	14	[1, 5, 13, 21], [1, 6, 14, 21], [1, 7, 15, 21], [1, 8, 16, 21], [1, 11, 19, 21], [1, 12, 20, 21]
(1,22)	[1- 5- 13–22] ,[1- 5- 15–22] ,[1- 6- 14–22], [1- 6- 16–22], [1- 6- 14–21], [1- 7- 13–22], [1- 7- 15–22], [1- 7- 17–22], [1- 8- 14–22], [1- 8- 16–22], [1- 8- 18–22], [1- 11- 13–22], [1- 11- 17–22], [1- 12- 14–22], [1- 12- 18–22]	14	[1, 5, 13, 22], [1, 6, 14, 22], [1, 7, 15, 22], [1, 8, 16, 22], [1, 11, 17, 22], [1, 12, 18, 22]
(1,23)	[1- 5- 15–23] ,[1- 5- 19–23], [1- 6- 16–23], [1- 6- 20–23], [1- 7- 15–23], [1- 7- 17–23], [1- 8- 16–23], [1- 8- 18–23], [1- 11- 17–23], [1- 11- 19–23], [1- 12- 18–23], [1- 12- 20–23]	12	[1, 5, 15, 23], [1, 6, 16, 23], [1, 7, 17, 23], [1, 8, 18, 23], [1, 11, 19, 23], [1, 12, 20, 23]
(1,24)	[1- 5- 13–24] ,[1- 5- 19–24], [1- 6- 14–24], [1- 6- 20–24], [1- 7- 13–24], [1- 7- 17–24], [1- 8- 14–24], [1- 8- 18–24], [1- 11- 13–24], [1- 11- 17–24], [1- 11- 19–24], [1- 12- 14–24], [1- 12- 18–24], [1- 12- 20–24]	14	[1, 5, 13, 24], [1, 6, 14, 24], [1, 7, 17, 24], [1, 8, 18, 24], [1, 11, 19, 24], [1, 12, 20, 24]
(2,21)	[2- 5- 13–21] ,[2- 5- 15–21] ,[2- 5- 19–21], [2- 6- 14–21], [2- 6- 16–21], [2- 6- 20–21], [2- 7- 13–21], [2- 7- 15–21], [2- 8- 14–21], [2- 8- 16–21], [2- 9- 15–21], [2- 9- 19–21], [2- 10- 16–21], [2- 10- 20–21]	14	[2, 5, 13, 21], [2, 6, 14, 21], [2, 7, 15, 21], [2, 8, 16, 21], [2, 9, 19, 21], [2, 10, 20, 21]
(2,22)	[2- 5- 13–22] ,[2- 5- 15–22], [2- 6- 14–22], [2- 6- 16–22], [2- 7- 13–22], [2- 7- 15–22], [2- 7- 17–22], [2- 8- 14–22], [2- 8- 16–22], [2- 8- 18–22], [2- 9- 15–22], [2- 9- 17–22], [2- 10- 16–22], [2- 10- 18–22]	14	[2, 5, 13, 22], [2, 6, 14, 22], [2, 7, 15, 22], [2, 8, 16, 22], [2, 9, 17, 22], [2, 10, 18, 22]
(2,23)	[2- 5- 15–23] ,[2- 5- 19–23], [2- 6- 16–23], [2- 6- 20–23], [2- 7- 15–23], [2- 7- 17–23], [2- 8- 16–23], [2- 8- 18–23], [2- 9- 15–23], [2- 9- 17–23], [2- 9- 19–23], [2- 10- 16–23], [2- 10- 20–23], [2- 10- 18–23]	14	[2, 5, 15, 23], [2, 6, 16, 23], [2, 7, 17, 23], [2, 8, 18, 23], [2, 9, 19, 23], [2, 10, 20, 23]
(2,24)	[2- 5- 13–24] ,[2- 5- 19–24], [2- 6- 14–24], [2- 6- 20–24], [2- 7- 13–24], [2- 7- 17–24], [2- 8- 14–24], [2- 8- 18–24], [2- 9- 17–24], [2- 9- 19–24], [2- 10- 18–24], [2- 10- 20–24],	12	[2, 5, 13, 24], [2, 6, 14, 24], [2, 7, 17, 24], [2, 8, 18, 24], [2, 9, 19, 24], [2, 10, 20, 24]
(3,21)	[3- 7- 13–21], [3- 7- 15–21], [3- 8- 14–21], [3- 8- 16–21], [3- 9- 15–21], [3- 9- 19–21], [3- 10- 16–21], [3- 10- 20–21], [3- 11- 13–21], [3- 11- 19–21], [3- 12- 14–21], [3- 12- 20–21]	12	[3, 7, 13, 21], [3, 8, 14, 21], [3, 9, 15, 21], [3, 10, 16, 21], [3, 11, 19, 21], [3, 12, 20, 21]
(3,22)	[3- 7- 13–22], [3- 7- 15–22], [3- 7- 17–22], [3- 8- 14–22], [3- 8- 16–22], [3- 8- 18–22], [3- 9- 15–22], [3- 9- 17–22], [3- 10- 16–22], [3- 10- 18–22], [3- 11- 13–22], [3- 11- 17–22], [3- 12- 14–22], [3- 12- 18–22]	14	[3, 7, 13, 22], [3, 8, 14, 22], [3, 9, 15, 22], [3, 10, 16, 22], [3, 11, 17, 22], [3, 12, 18, 22]
(3,23)	[3- 7- 15–23], [3- 7- 17–23], [3- 8- 16–23], [3- 8- 18–23], [3- 9- 15–23], [3- 9- 17–23], [3- 9- 19–23], [3- 10- 16–23], [3- 10- 20–23], [3- 10- 18–23], [3- 11- 17–23], [3- 11- 19–23], [3- 12- 18–23], [3- 12- 20–23]	14	[3, 7, 15, 23], [3, 8, 16, 23], [3, 9, 17, 23], [3, 10, 18, 23], [3, 11, 19, 23], [3, 12, 20, 23]
(3,24)	[3- 7- 13–24], [3- 7- 17–24], [3- 8- 14–24], [3- 8- 18–24], [3- 9- 17–24], [3- 9- 19–24], [3- 10- 18–24], [3- 10- 20–24], [3- 11- 13–24], [3- 11- 17–24], [3- 11- 19–24], [3- 12- 14–24], [3- 12- 18–24], [3- 12- 20–24]	14	[3, 7, 13, 24], [3, 8, 14, 24], [3, 9, 17, 24], [3, 10, 18, 24], [3, 11, 19, 24], [3, 12, 20, 24]
(4,21)	[4- 5- 13–21] ,[4- 5- 15–21] ,[4- 5- 19–21], [4- 6- 14–21], [4- 6- 16–21], [4- 6- 20–21], [4- 9- 15–21], [4- 9- 19–21], [4- 10- 16–21], [4- 10- 20–21], [4- 11- 13–21], [4- 11- 19–21], [4- 12- 14–21], [4- 12- 20–21]	14	[4, 5, 13, 21], [4, 6, 14, 21], [4, 9, 15, 21], [4, 10, 16, 21], [4, 11, 19, 21], [4, 12, 20, 21]
(4,22)	[4- 5- 13–22] ,[4- 5- 15–22] ,[4- 6- 14–22], [4- 6- 16–22], [4- 9- 15–22], [4- 9- 17–22], [4- 10- 16–22], [4- 10- 18–22] [4- 11- 13–22], [4- 11- 17–22], [4- 12- 14–22], [4- 12- 18–22]	12	[4, 5, 13, 22], [4, 6, 14, 22], [4, 9, 15, 22], [4, 10, 16, 22], [4, 11, 17, 22], [4, 12, 18, 22]
(4,23)	[4- 5- 15–23] ,[4- 5- 19–23], [4- 6- 16–23], [4- 6- 20–23], [4- 9- 15–23], [4- 9- 17–23], [4- 9- 19–23], [4- 10- 16–23], [4- 10- 20–23], [4- 10- 18–23], [4- 11- 17–23], [4- 11- 19–23], [4- 12- 18–23], [4- 12- 20–23]	14	[4, 5, 15, 23], [4, 6, 16, 23], [4, 9, 17, 23], [4, 10, 18, 23], [4, 11, 19, 23], [4, 12, 20, 23]
(4,24)	[4- 5- 13–24] ,[4- 5- 19–24], [4- 6- 14–24], [4- 6- 20–24], [4- 9- 17–24], [4- 9- 19–24], [4- 10- 18–24], [4- 10- 20–24], [4- 11- 13–24], [4- 11- 17–24], [4- 11- 19–24], [4- 12- 14–24], [4- 12- 18–24], [4- 12- 20–24]	14	[4, 5, 13, 24], [4, 6, 14, 24], [4, 9, 17, 24], [4, 10, 18, 24], [4, 11, 19, 24], [4, 12, 20, 24]

4. Performance Analysis Of The Proposed Design

The fault-tolerance capability of the proposed 6DP-MIN is high among all the MINs available in the literature for 8x8 networks. It can tolerate upto five link or switching elements failures for every S-D node pair.

4.1 Reliability Analysis

This section evaluates the reliability of various MINs and the proposed 6DP-MIN. There are multiple methods [3] used in literature to calculate reliability like the Decomposition method, Reliability Block Diagram, Monte carlo simulation, Reliability bounds, etc.

The frequently considered reliabilities are: 2 terminal, broadcast, network reliability [31].

- Two-terminal reliability or terminal reliability (TR) is the most commonly used reliability. It is defined as the probability of having at least one operational path between a specified source and a destination node.
- All terminal reliability or network reliability is defined as the probability of an operational path for every node pair.
- Broadcast reliability is defined as the probability of existing the path between a given source and all destinations.

Some general assumptions are used for evaluating reliability; these assumptions are:

i. All switching elements can have only two states: working or failed; no other intermediate state exists.
ii. All switching elements are statically independent and have identical reliability.
iii. All switching elements of initial and final stages are perfectly reliable.

For reliability evaluation, we are using two steps process, which involves (i) finding pathsets for specified node pairs, and (ii) disjointing the found pathsets using a MVI algorithm.

For two-terminal reliability, we find the paths for different source to destination node pairs shown in Table 3. From the table, we can see that it provides total 14 paths or 12 redundant paths. Twelve paths are present when *jth* switch of the source stage is connected to the *(j + 2)th* switch of the destination stage as represented in Fig. 7 otherwise it provides 14 redundant paths. If the switch number appears four or greater than 4 then 4 is subtracted from the number, which will provide the correct number of destination switches. Now using these redundant paths, terminal reliability expression in the compact form of the sum of disjoint products (SDP) have been evaluated for the proposed 6DP-MIN using an improved multi-variable inversion (MVI) algorithm [32] which are given by the following mathematical expression, where *r* is the reliability of each switching elements:

$$R_{2TR} = 12r^4 - 12r^5 - 42r^6 + 84r^7 - 4r^8 - 108r^9 + 87r^{10} + 12r^{11} - 48r^{12} + 24r^{13} - 4r^{14} for 12 paths$$

$$R_{2TR} = 14r^4 - 20r^5 - 43r^6 + 144r^7 - 144r^8 + 32r^9 + 45r^{10} - 32r^{11} + 2r^{12} + 4r^{13} - r^{14} for 14 paths$$

For broadcast and network reliability first total number of broadcast paths (specified source to all destination nodes) and all terminal paths (all source to all destination nodes) have been evaluated, which are 84 and 684 in number, respectively. Using these path sets, reliability values for different switch reliability has been calculated and given in Table 5.

Table 5
All three types of reliability for 6DP-MIN at different values of switch reliability.

Switch reliability	2 terminal Reliability (2 TR)		Broadcast reliability (BR)	Network Reliability(NR)
	14 terminal paths	12 Terminal paths	84 Broadcast paths	684 Network Paths
0.9	0.809996217	0.809995928	0.590480998	0.430447428
0.95	0.902499938	0.902499936	0.773780764	0.663419976
0.96	0.921599984	0.921599983	0.815372651	0.721389451
0.98	0.960400	0.9604	0.903920796	0.85076302
0.99	0.9801	0.9801	0.95099005	0.922744694

4.2 Cost Analysis

The most important thing that is considered in MIN design is its cost. The cost of a MIN can be calculated by using switching elements complexity. Switching elements complexity simply involved number of gates/crossover point used, for example a switch of size 2x2 has

4 unit of hardware cost and a switch of size 2x6 having 12 units hardware cost. Therefore, we can say that a switch of size having mxn has a hardware cost of mn units. For mux and de-mux we roughly assume that mx1 mux or 1xm de-mux has a cost of m units [32].

Following equation can be used to calculate the cost of MIN:

$(numberofMuxXcostofaMux) + (numberofDemuxXcostofaDemux) + (totalnumberofswitchesXCostofaSwitch)$

Here, we are considering switches of different sizes there for cost of (total number of switches X cost of a switch) calculated separately for each stage. Now cost for smaller network which are having less number of paths and low fault tolerant capacity having less cost but the MINs having large number of paths and having high fault tolerant capability having more cost. Therefore for cost comparison we are using a new concept "cost per unit" which is calculated as given below

$$costperunit = \frac{Totalcostofthenetwork}{totalnumberofpathsforeach(S-D)nodepair}$$

Total hardware Cost of the proposed 6DP-MIN is evaluated as follows:

Numbers of 2 x 6 switching elements = 4; giving cost = *2x6x4 = 48*

Numbers of 3 x 3 switching elements = 16; cost of these switching elements = *3x3x16 = 144*

Numbers of 6 x 2 switching elements = 4;cost of these switching elements = 6 x 2 x 4 = 48

Total hardware cost of 6 disjoint Path MIN for N = 8 is 48 + 144 + 48 = 230 units.

Total number of paths for each source to destination node pair is shown in Table 3. From the table, if we calculate cost per unit for 14 and 12 paths will be given as:

$$costperunit = \frac{230}{14} = 16.43 for 14 paths$$

$$= \frac{230}{12} = 19.17 for 12 paths$$

Table 6
comparison of proposed 6DP-MIN with others existing MINs.

Sr. No.	Types of network	total number of paths	Disjoint paths	Switch Reliability r is 0.9			Total Cost	Cost per unit
				terminal Reliability	Broadcast Reliability	Network Reliability		
1	SEGINs	3	2	0.7873	0.5635	0.3999	80	26.66
2	SEGLNIN	4	2	0.7997	0.5798	0.4167	100	25
		5	2	0.8004			100	20
3	3-DGIN	4	3	0.8057	0.3765	0.2623	176	44
4	3 disjoint path network	7	3	0.8082	0.58733	0.42644	120	17.14
		6	3	0.80818			120	20
5	4DGIN-1,4DGIN-2	5	4	0.8092	0.5889	0.4269	160	32
		6	4	0.8094			160	26.67
		7	4	0.8095			160	22.86
6	4DGIN-3	6	4	0.8094	0.5889	0.4283	160	26.66
7	**6DP-MIN (Proposed)**	14	6	0.80999	0.59048	0.43044	230	16.43
		12	6	0.80999			230	19.17

From the Table 6, we can say that proposed 6DP-MIN having more number of redundant and disjoint paths with respect to less cost per unit and better reliability from the compared MINs.

5. Conclusion

In this paper, a new design layout of fault-tolerant MIN is proposed. It provides six disjointpaths between any S-D node pairs. In this design, faulty switches of ntermediate stagesare tolerated by using the various redundant paths available in the network. The present study also compared the reliability evaluation of some existing MIN architectures, and the reliability of the proposed six disjoint paths with other MINs. Hence, it is a better option for multiprocessor interconnectionnetworks. In Table 6, a comparative view of the proposed six disjoint paths multistage interconnection network has been given. This design provides a large number of redundant paths, which are 14 and 12 in numbers for different source to destination node pairs. Due to 6 disjoint paths, this network can tolerate upto five link failures.Two terminal reliability expressions for 14 and 12 paths are evaluated, given in table 4. Broadcast and network reliability also calculated of this proposed design.

Declarations

Acknowledgement

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Table 4

Table 4 is not available with this version

Figures

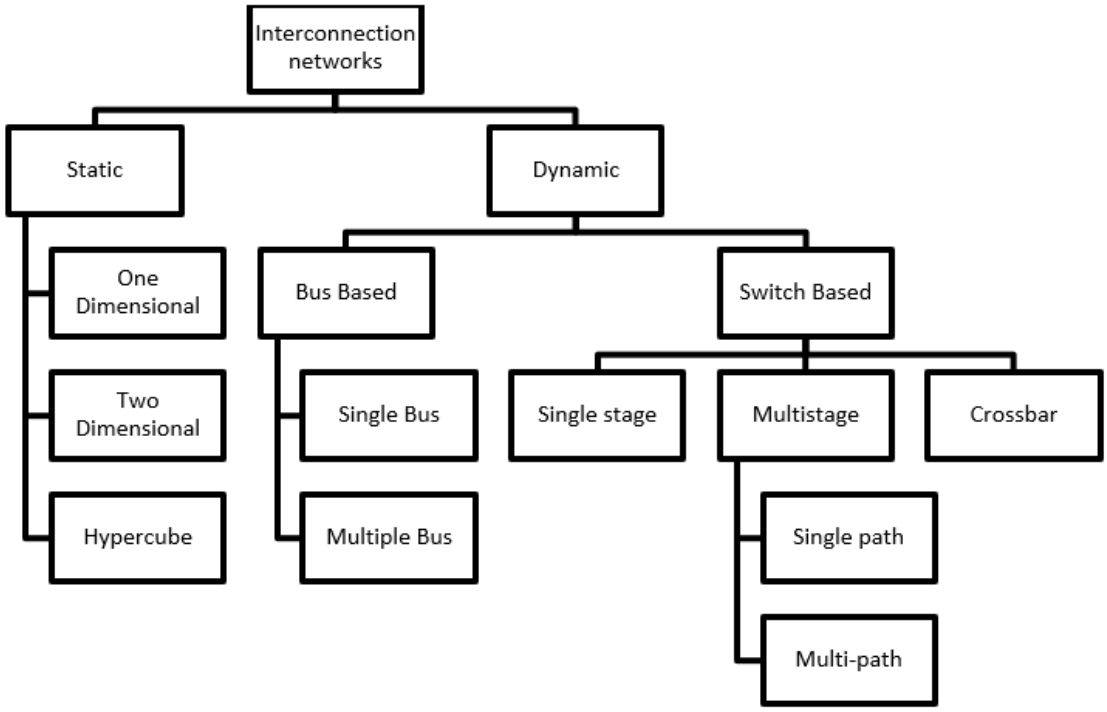

Figure 1

Classification for interconnection networks based on topology [2].

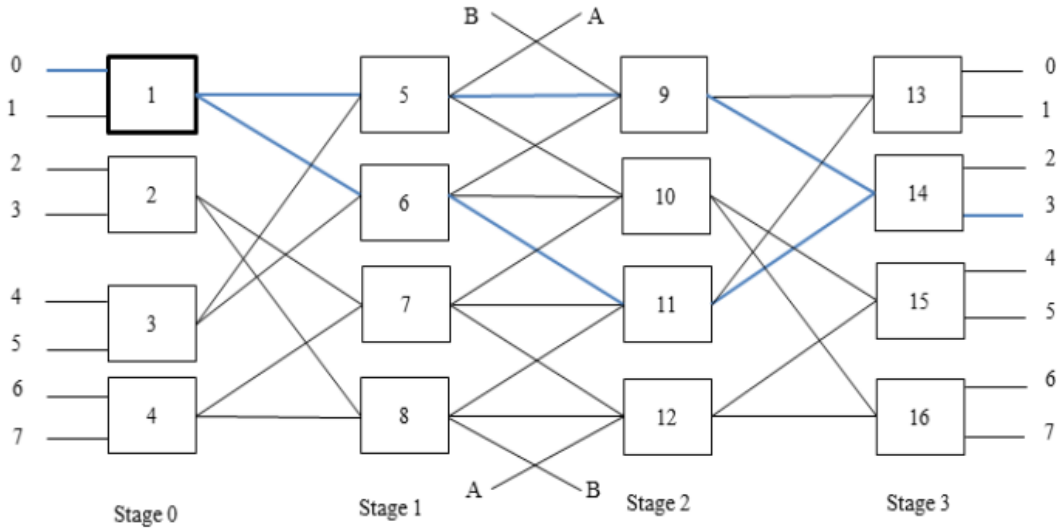

Figure 2

A topological view of SEGIN.

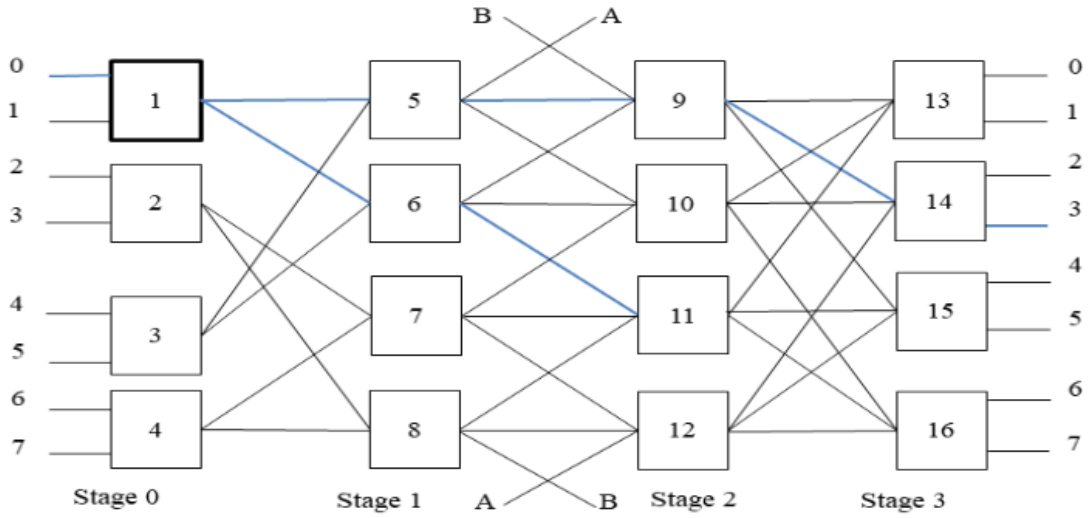

Figure 3

A topological view of SEGLNIN

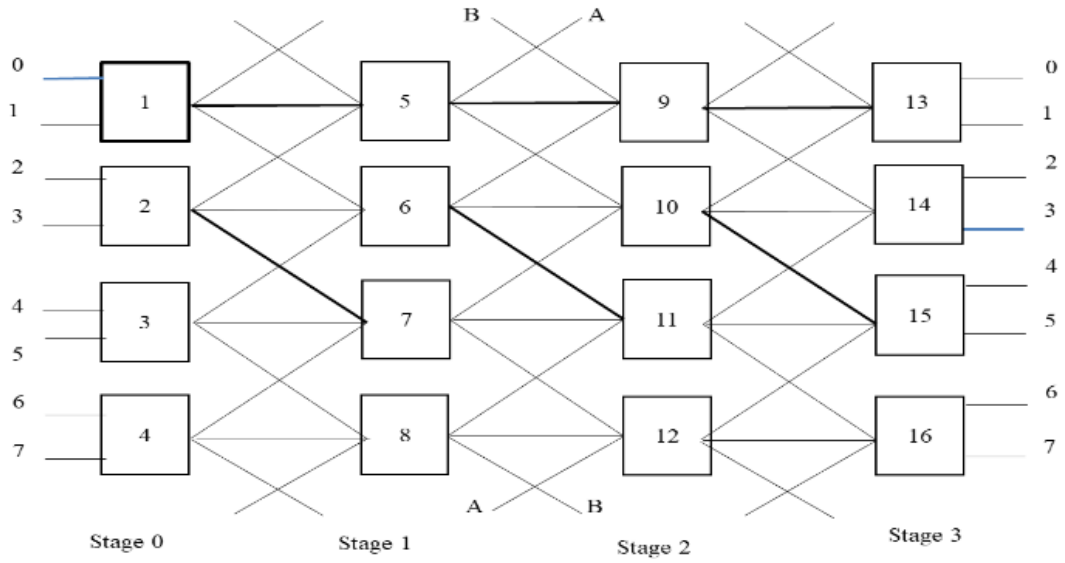

Figure 4

A connection pattern of 8x8 size three disjoint path multistage interconnection network [23].

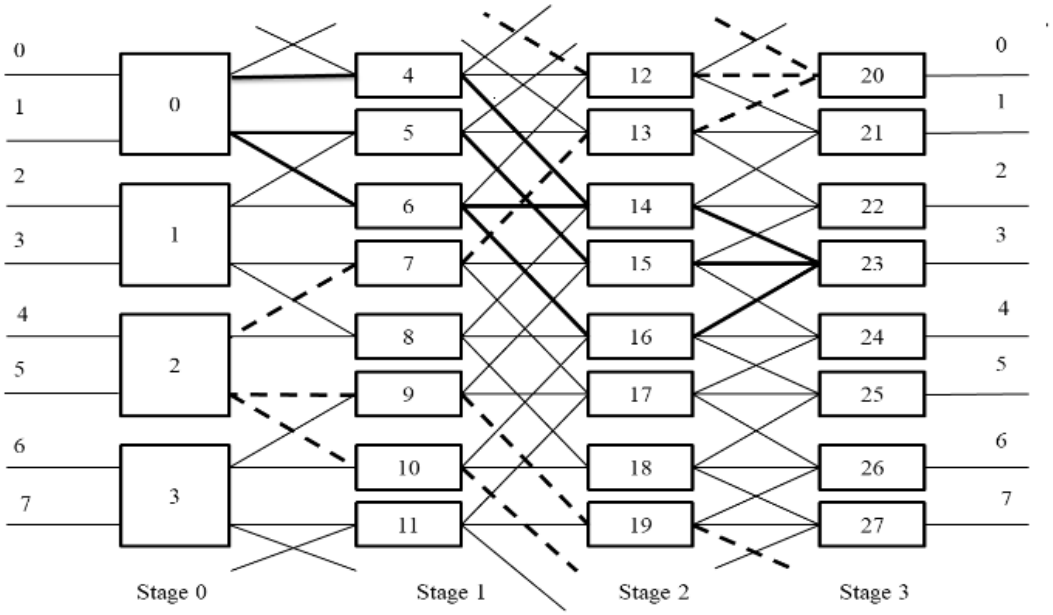

Figure 5

connection pattern of 3 DGIN [24].

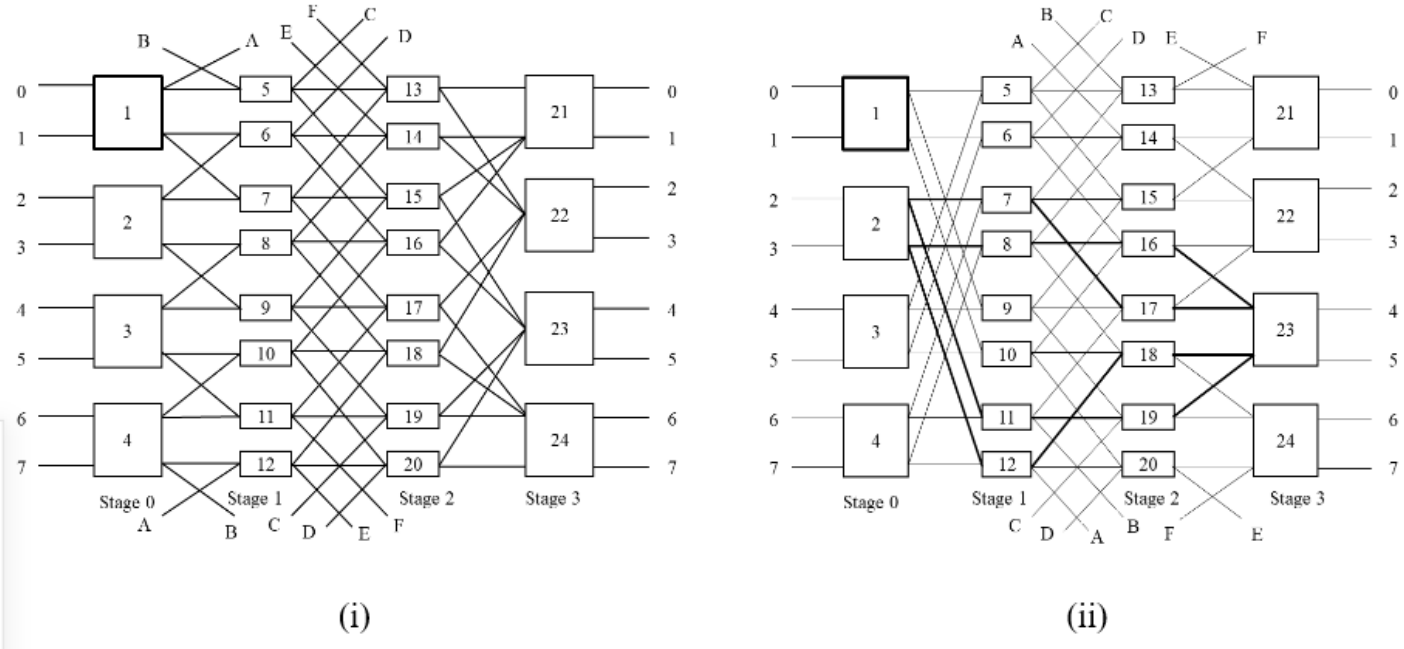

Figure 6

A connection pattern layout (i) 4 DGIN-1 (ii) 4DGIN-3.

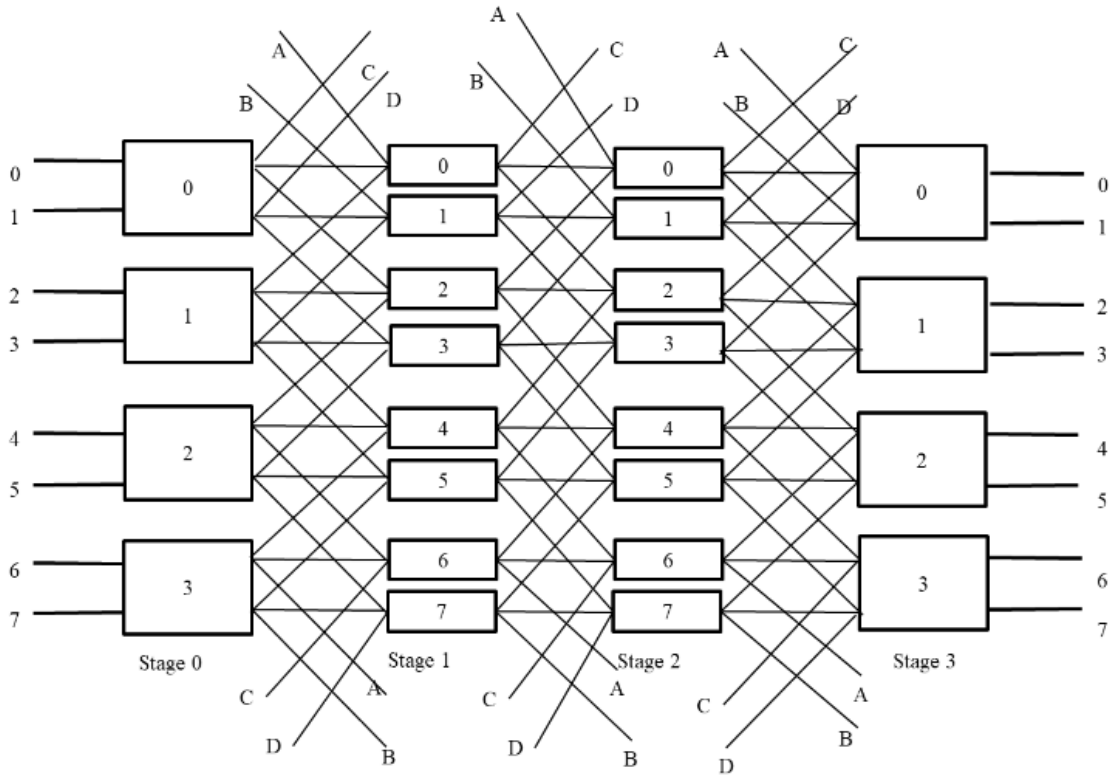

Figure 7

Connection pattern diagram of the 6DP-MIN.

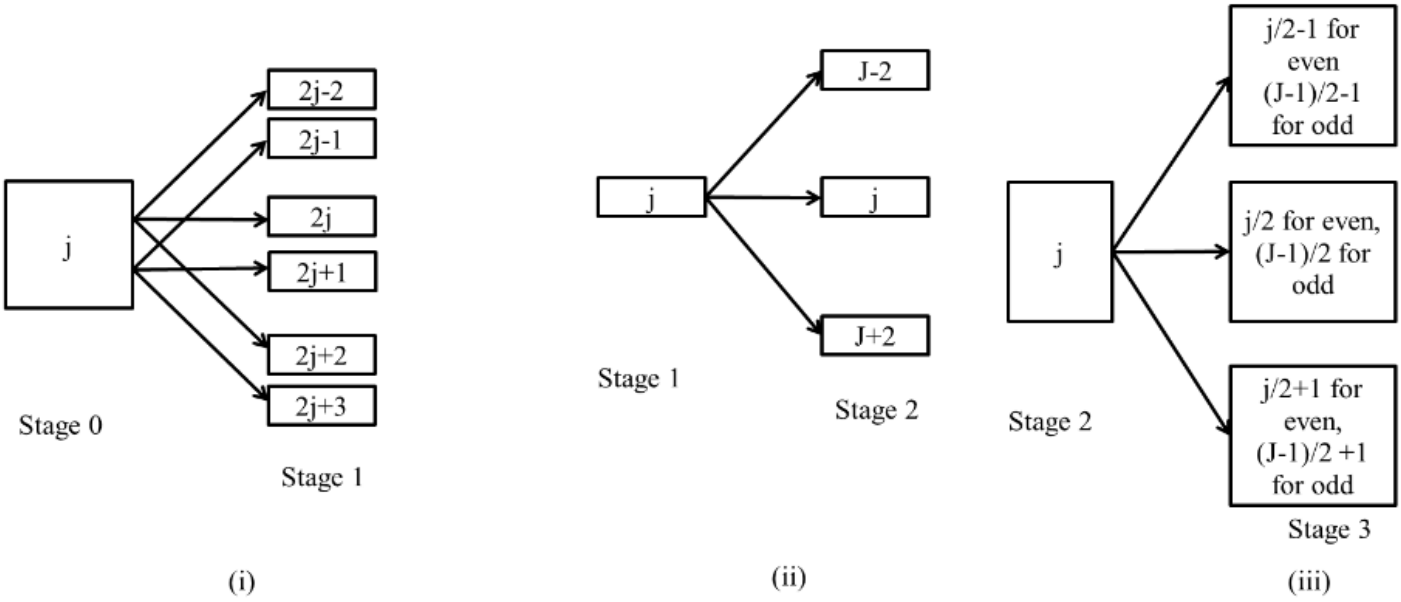

Figure 8

Connection pattern algorithm of 6 disjoint path multistage interconnection network (i) between stage 0 and stage 1 (ii) between stage 1 and stage 2 (iii) between stage 2 and stage 3.