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On High-Speed Digital-to-Analog Converters and Semi-Digital FIR Filters

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To my family

Abstract

High-speed and high-resolution digital-to-analog converters (DACs) are vital components in all telecommunication systems. Radio-frequency digital-to-analog converter (RFDAC) provides high-speed and high-resolution conversion from digital domain to an analog signal. RFDACs can be employed in direct-conversion radio transmitter architectures. The idea of RFDAC is to utilize an oscillatory-pulse-amplitude modulation instead of the conventional zero-order hold pulse amplitude modulation, which results in DAC output spectrum to have high-energy high-frequency lobe, other than the Nyquist main lobe. The frequency of the oscillatory pulse can be chosen, with respect to the sample frequency, such that the aliasing images of the signal at integer multiples of the sample frequency are landed in the high-energy high-frequency lobes of the DAC frequency response. Therefore the high-frequency images of the signal can be used as the output of the DAC, i.e., no need to the mixing stage for frequency up-conversion after the DAC in the radio transmitter. The mixing stage however is not eliminated but it is rather moved into the DAC elements and therefore the local oscillator (LO) signal with high frequency should be delivered to each individual DAC element.

In direct-conversion architecture of IQ modulators which utilize the RFDAC technique, however, there is a problem of finite image rejection. The origin of this problem is the different polarity of the spectral response of the oscillatory-pulse-amplitude modulation in I and Q branches. The conditions where this problem can be alleviated in IQ modulator employing RFDACs is also discussed in this work.

$\Sigma\Delta$ modulators are used preceding the DAC in the transmitter chain to reduce the digital signal's number of bits, still maintain the same resolution. By utilizing the $\Sigma\Delta$ modulator now the total number of DAC elements has decreased and therefore the delivery of the high-frequency LO signal to each DAC element is practical. One of the costs of employing $\Sigma\Delta$ modulator, however, is a higher quantization noise power at the output of the DAC. The quantization noise is ideally spectrally shaped to out-of-band frequencies by the $\Sigma\Delta$ modulator. The shaped noise which usually has comparatively high power must be filtered out to fulfill the radio transmission spectral mask requirement.

Semi-digital FIR filter can be used in the context of digital-to-analog conversion, cascaded with $\Sigma\Delta$ modulator to filter the out-of-band noise by the modulator. In the same time it converts the signal from digital domain to an analog quantity. In general case, we can have a multi-bit, semi-digital FIR filter where each tap of the filter is realized with a sub-DAC of M bits. The delay elements are also realized with M-bit shift registers. If the output of the modulator is given by a single bit, the semi-digital FIR filter taps are simply controlled by a single switch assuming a current-steering architecture DAC. One of the major advantages is that the static linearity of the DAC is optimum. Since there are only two output levels available in the DAC, the static transfer function, regardless of the mismatch errors, is always given by a straight line.

In this work, the design of SDFIR filter is done through an optimization procedure where the $\Sigma\Delta$ noise transfer function is also taken into account. Different constraints are defined for different applications in formulation of the SDFIR optimization problem. For a given radio transmitter application the objective function can be defined as, e.g., the hardware cost for SDFIR implementation while the constraint can be set to fulfill the radio transmitter spectral emission mask.

Populärvetenskaplig sammanfattning

Snabba och högupplösande digitala-till-analog-omvandlare (DAC) är vitala komponenter i telekommunikationssystem. Så kallade RFDAC:ar, dvs digital-till-analog-omvandlare som arbetar i radiofrekvenser möjliggör snabb och högupplöst konvertering direkt från den digitala domänen till den analoga. RFDAC:ar kan användas i radiosändare som använder sig av direktomvandling. Tanken med RFDAC:ar är att utnyttja en oscillerande pulsamplitudmodulering stället för konventionell pulsamplitudmodulering. Detta resulterar i att DAC:ens utsignalspektrum kommer ha högre signalenergier i högre frekvensband, dvs inte inom det så kallade Nyquistbandet. Frekvensen hos den oscillerande pulsen kan väljas beroende på sampelfrekvensen så att vikningskomponenter hamnar i multiplar av sampelfrekvensen. Det innebär att, med hjälp av filtrering, man kan använda de högre frekvenskomponenterna snarare än de lägre. Det behövs ingen extra blandare för att multiplicera upp signalfrekvensen runt en bärfrekvens. Själva blandningen sker istället inne i digital-till-analog-omvandlaren.

I direktomvandlande IQ-modulatorer som använder RFDAC:ar kan det uppstå problem med undertryckning av vikta kopmponenter. Orsaken till detta problemet är att det är olika polaritet på pulsamplitudmodulationen i de olika grenarna. Hur dessa problem kan bemötas beskrivs i detta arbete.

$\Sigma\Delta$ modulatorer används sändarkedjan för att minska antal bitar i den digitala signalen. Fortfarande bibehålls dock samma effektiva upplösning. Genom att använda $\Sigma\Delta$ minskar nu det totala antalet analoga byggstenar i omvandlaren vilket gör det enklare att kunna fördela högfrekventa signaler med högre kvalitet. En kostnad som måste tas i beaktande är att en sigma-delta producerar högt kvantiseringsbrus utanför signalbandet. Det måste filtreras bort för att kunna uppfylla kraven på utsänd effekt i sidoband.

Semi-digital FIR-filter kan användas i samband med digital-till-analog omvandling då de serieskopplas med $\Sigma\Delta$ modulatorn. Detta kommer filtrera ut det extra bruset medan det samtidigt representerar den digitala signalen med en analog motsvarighet. I det allmänna fallet kan ett semi-digitalt FIR-filter bestå av ett antal grenar i vilka det sitter mindre digital-till-analogomvandlare med lägre upplösning. Om grenarna innehåller 1-bitsomvandlare så kommer följdaktigligen de små omvandlarna helt enkelt bestå av en brytare som leder ström av viss kvantitet till utgång eller icke. En av de största fördelarna är att linjäriteten hos omvandlaren blir ideal. Då det bara finns två möjliga signalsnivåer kommer överföringsfunktionen alltid kunna beskrivas av en rät linje, dvs helt linjär.

I detta arbete presenterar vi hur SDFIR-filtret kan konstrueras genom att ett rigoröst optimeringsförfarande där brusöverföringsfunktionen hos sigma-delta modulatorn också beaktas. Olika krav och målfunktioner har använts. För en given tillämpning kan man till exempel optimera hårdvarukostnaden och samtidigt kräva att utsänd effekt hålls inom tolerabla, specificerade nivåer.

Acknowledgments

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I have had the extraordinary luck in life to have been blessed with a family that always supports me. I would like to thank my parents for their never-ending love and support. Also my sisters, Soheila and Leila, for their kindness and energetic chats.

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M. Reza Sadeghifar
December 17, 2014,
Stockholm Sweden

Preface

Thesis outline

This thesis consists of two parts; Part-I, background and Part-II, publications. In Part-I a short background is given on different radio transmitter architectures and digital-to-analog converters (DAC) used in them. Part-II which forms the publications part, is comprised of five papers in the field of high-speed digital-to-analog converters and semi-digital FIR filters.

The outline of Part-I of the thesis is as follows. Chapter 1, is a review on different radio transmitter architectures while Chapter 2, gives an introduction on high-speed DACs for telecommunication. In this chapter the basics of high speed DACs and the fundamental limitations on achievable performance is described and different techniques to achieve high-speed digital-to-analog conversion is briefly explained.

In chapter 3, radio-frequency digital-to-analog converters (RFDAC) is studied in details. The RFDAC is employed in direct-digital-to-RF modulators for wireless radio transmitters. The intrinsic problem of the finite image rejection in these architectures is traced in details and conceptually illustrated. Moreover an overview of the proposed architecture in direct-digital-to-RF converters employing low-resolution oscillatory signal is also presented in this chapter.

Semi-digital FIR filter design is studied in chapter 4, where a background on different blocks in SDFIRs is reviewed. The optimization procedure for designing SDFIR is presented including the definition of different constraint used in the SDFIR design. Finally, in Chapter 5, conclusions are given and possible future work is discussed.

Publications

This thesis is comprised of four peer-reviewed papers (Papers B-E) and one non-peer-reviewed paper (paper A) as follows.

Paper A: **M. Reza Sadeghifar**, J Jacob Wikner, "A Survey of RF DACs," in *Proc. Swedish System On Chip Conf. (SSoCC)*, Sweden, 2010.

Paper B: **M. Reza Sadeghifar**, J Jacob Wikner, "A Higher Nyquist-Range DAC Employing Sinusoidal Interpolation," in *Proc. NORCHIP Conf.*, Tampere, Finland, Nov. 2010.

Paper C: **M. Reza Sadeghifar**, J Jacob Wikner, "Modeling and Analysis of Aliasing Image Spurs Problem in Digital-RF-Converter-Based IQ Modulators ," in *Proc. Int. Symp. Circuits Syst. (ISCAS)*, Beijing, China, May 2013.

Paper D: **M. Reza Sadeghifar**, Nadeem Afzal, J Jacob Wikner, "A Digital-RF Converter Architecture for IQ Modulator with Discrete-Time Low Resolution Quadrature LO," in *Proc. IEEE Int. Conf. Electronics, Circuits and Syst. (ICECS)*, Abu Dhabi, UAE, Dec. 2013.

Paper E: **M. Reza Sadeghifar**, J Jacob Wikner, Oscar Gustafsson, "Linear Programming Design of Semi-Digital FIR Filter and $\Sigma\Delta$ Modulator for VDSL2 Transmitter," in *Proc. Int. Symp. Circuits Syst. (ISCAS)*, Melbourne, Australia, May 2014.

The following papers contain work done by the author but are not included in the thesis either because it has not been the main focus of this thesis or is under review process or is covered in author's other publications.

1. Nadeem Afzal, **M. Reza Sadeghifar**, J Jacob Wikner, "A Study on Power Consumption of Modified Noise-Shaper Architectures for Sigma-Delta DACs," in *Proc. European Conf. Circuit Theory Design (ECCTD)*, Linköping, Sweden, Aug., 2011.

2. **M. Reza Sadeghifar**, J Jacob Wikner, and Oscar Gustafsson "Optimization of Semi-Digital FIR Filter and $\Sigma\Delta$ Modulator for VDSL2 Specification," in *Proc. Swedish System On Chip Conf. (SSoCC)*, Vadstena, Sweden, May, 2014.

3. **M. Reza Sadeghifar**, Oscar Gustafsson, J Jacob Wikner, "Optimizing Semi-digital FIR filters Using Analog Metrics," *IEEE Trans. Circuits Syst. I - Regular Papers*, under review.

Contents

Part I

Background

Chapter 1

Introduction

Increasing demand on the capacity of the current and next generation cellular radio has driven the integrated circuits for wireless communication in recent years. The trend towards more integration, lower power and smaller size has called for newer transceivers architectures. With the scaling of the CMOS technology towards smaller nodes, smaller size transistors and thus more integration than has become feasible. The digital integrated circuits has gained from the smaller size and hence lower capacitance and higher frequency of operation while the analog and RF circuits suffers from the lower intrinsic device gain and the reduction of the available voltage swing.

Consequently there has been a trend to migrate the analog and RF building blocks in transceivers' architecture into digital counterparts, to comply with scaling of CMOS technology and hence benefit in terms of speed, power and size. The objective has been to push the digital-analog interface towards the antenna and the ultimate "ambition" is to put the antenna directly after the DAC or ADC in transceivers.

The idea of direct-digital-to-RF modulator to be utilized in the multistandard and flexible transmitters is following this trend. There has been many different works in recent years that have tried to address the challenges and fulfill the requirements of different wireless communication standards [1–9].

In this chapter, a short overview of conventional architectures utilized in radio transmitters is given, and then briefly the direct-digital-to-RF modulator transmitters is introduced.

1.1 Transmitter Architectures

In the transmitter part of the radio, different architectures has been evolved during the course of time. In this chapter some of the architectures will be

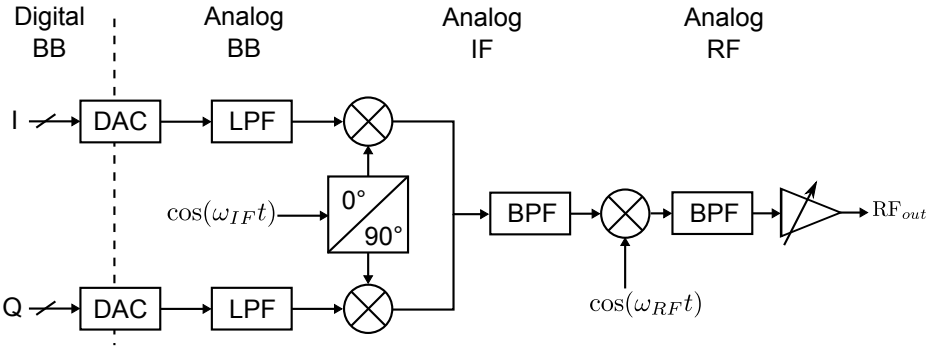

Figure 1.1: Superheterodyne transmitter

reviewed with their advantages and disadvantages for today's radio communication applications is discussed briefly.

1.1.1 Superheterodyne Transmitter

In superheterodyne transmitter, the frequency upconversion from baseband (BB) is performed in two steps, first into intermediate frequency (IF) and then to the desired radio frequency (RF). A simplified superheterodyne transmitter is shown in Fig. 1.1. Digital I and Q baseband signals are converted to analog signal through a digital-to-analog converter which typically is Nyquist-rate converter. The analog baseband low pass filters remove the aliasing images. The quadrature modulation is performed at IF and in the second step, the signal is upconverted to RF by the RF mixer stage. This architecture has the advantage of IQ modulation at IF frequencies which results in better matching between I and Q branches. However, there are some disadvantages to this architecture such as the complexity of having two VCOs, additional RF band pass filtering after the second frequency modulation and complex frequency planning.

1.1.2 Direct-Conversion Transmitter

The upconversion to the desired RF carrier can be performed directly from the baseband spectrum by the direct-conversion transmitter. In this architecture quadrature IQ modulator with RF frequency translates the baseband analog signal to RF carrier as shown in Fig. 1.2. The baseband analog signal is the filtered output of the DAC.

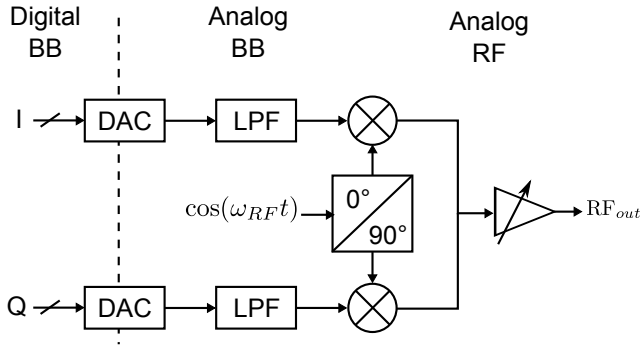

Figure 1.2: Direct-conversion transmitter

The RF signal is then amplified to the desired power level to be sent to the power amplifier (PA) and transmitter antenna.

1.1.3 Direct-Digital-to-RF Modulator Transmitter

In a direct digital-to-RF modulator transmitter, the digital-to-analog conversion and frequency mixing is performed in one block as shown in Fig. 1.3. This was first reported as an oscillatory pulse amplitude modulation (PAM) employed in the DAC in [1] and was coined as RFDAC.

Multimode Transmitter Using Direct-Digital-to-RF Modulator [2]

Multistandard challenges for wireless communication devices has called for innovative solutions that are independent from the system architecture. In [2], a multistandard transmitter implemented in 0.13 μm is reported. Due to 10-bit resolution of the direct-digital-to-RF modulator (DDRM) employed in that work, it could satisfy different standards spectrum mask requirements such as EDGE, WCDMA, and WLAN. However in this DDRM, the oscillatory PAM is not used and instead the digital signal and square wave local oscillator (LO) signal has controlled the two cascaded switches.

The drawback with this architecture is that the high frequency LO signal has to be delivered to all the unit elements of the DAC, which in this case is 1024 units, makes difficult to maintain good matching and avoid skew problems. Moreover the LO buffers used in that work to drive the large capacitance due to gate capacitance and wiring, is reported to consume about 12mA on each I and

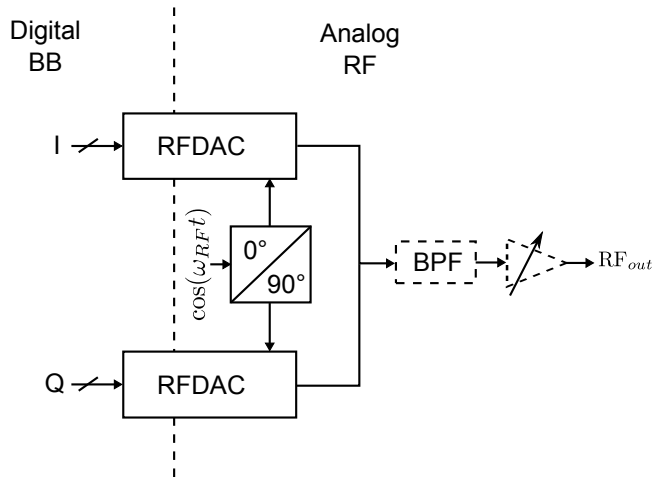

Figure 1.3: Direct-digital-to-RF modulator transmitter

Q branches. This translates to high power consumption in overall transmitter. This problem can be addressed by either using a fewer number of unit elements by employing $\Sigma\Delta$ modulator before RFDAC to reduce the number of bits [10], or using discrete-oscillatory signal [11].

$\Sigma\Delta$ *Direct-Digital-to-RF Modulator [10]*

As mentioned, one approach to decrease the number of unit elements in the DDRM is to employ $\Sigma\Delta$ modulator. $\Sigma\Delta$ modulator is usually used to reduce the number of bits, while maintaining the same level of signal to noise ratio. This is achieved by spectral shaping of the quantization noise to the out of interest band. In wireless communication applications, however this high power out-of-band noise needs to be filtered before sending over the channel in order to meet the spectral mask requirement.

In [10], a $\Sigma\Delta$ Direct-digital-to-RF modulator transmitter is presented. It employs a 3-bit output $\Sigma\Delta$ modulator and therefore a huge reduction on the number of unit elements of the DDRM (only 8 comparing to 1024 in the previous case). The penalty however is the need for a high-Q filter at the output of the DDRM. In that work a fourth order passive LC RF filter is utilized.

DDRM and Semidigial FIR filter [3]

To cope with the filter requirement in a $\Sigma\Delta$ DDRM, a semi-digital FIR filter combined with DDRM is employed in [3]. In a conventional semi-digital FIR filter the digital-to-analog conversion is embedded in a FIR filter topology such that the frequency response of the DAC is identical to the that FIR filter used. In [3], the DAC unit elements are replaced by a DDRM unit elements, targeting all together.

The drawback however is that in a semi-digital FIR filter the order of the filter should be high enough to get an adequate filtering response. Further, the bit resolution of the FIR coefficients should be in a range that filtering characteristics are maintained and thus the number of unit elements are increased again to before the $\Sigma\Delta$. In [3], to avoid this, a simple 6th order filter with identical taps is utilized which gave the impression of not being sufficient for wireless communication applications.

Chapter 2

Digital-to-Analog Converters for Telecommunications

Digital-to-analog converters (DACs), are utilized in different applications such as communication, data acquisition, or test and measurement applications [12, 13]. High-speed and high-resolution data converters are vital components in all telecommunication systems. Normally, the higher speed we can use for sampling, the lower requirements are put on analog components, such as analog filters [12]. Of course, a larger digital complexity is then required, but that is mostly scaled with process dimensions and becomes less of a concern. In this chapter, we present a discussion on some different design methodologies for high-speed digital-to-analog converters suitable for wideband applications with demanding requirements on linearity.

Most wide-spread telecommunication standards today such as GSM, LTE, WCDMA, WLAN, etc. require a typical range of 60 or 70 dB of linearity [14]. However for the next generation radio telecommunication systems very high linearity is required [15]. On the other hand, software-defined radio (SDR), needs the flexibility of the transceiver as well as the reconfigurable sampling as their key components. In SDR the system is required to be tuned over a fairly large frequency range such that it is flexible and can adopt to several different standards. Hence a high speed DAC with high linearity performance, gives the possibility to implement a reconfigurable multi-standard transmitter.

The first, and perhaps obvious, approach to convert from a digital to an analog representation at high speed is to increase the clock frequency of the DAC. This approach is however tied with an important question: do we need to also increase the signal bandwidth? For example, there is a substantial difference in design strategy if we want to obtain a 10-MHz signal bandwidth centered at some 500 MHz or if we want to obtain a 500-MHz signal bandwidth at a sample frequency of some 1 GHz, thus converting the entire Nyquist band.

This is of course a system-dependent issue, which could be related to for example software-defined radio or flexible front-ends [16].

2.1 Frequency Response of Digital-to-Analog Converter

Assume the input and output notations of a k-bit DAC as shown in 2.1. The

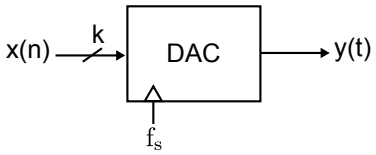

Figure 2.1: Block diagram of a k-bit DAC

output of the DAC, $y(t)$, is a analog signal, that can be expressed as a function of the input signal, $x(n)$, using the pulse amplitude modulation (PAM),

$$y(t) = \sum_{\forall n} x(n) \cdot p(t - nT), \tag{2.1}$$

where $p(t)$ is the pulse waveform and T is the sampling interval, $T = 1/f_s$. It is in theory possible to perfectly reconstruct $y(t)$ from $x(n)$ (for now ignoring the effect of truncation error due to limited word length) by selecting $p(t)$ as a mathematical function "$sinc(t)$" defined as $\frac{\sin(t)}{t}$ [17]. In frequency domain the digital signal which is repeated every 2π as a so called the aliasing images, undergoes an ideal brick-wall filter, resulted from the "sinc(t)", and the analog output signal is only the baseband signal without the aliasing images [17].

However, in reality this is impractical since the "sinc" function is double sided in time domain and thus cannot be realized by causal systems. Normally we select a rectangular pulse, $p(t) = u(t) - u(t - \tau)$, with a duration of τ. This forms a zero-order hold function, and typically, the duration, τ, equals the sampling period, but could be a fraction of that time if return-to-zero schemes are applied. In Fig. 2.2, the amplitude characteristics for some different return-to-zero schemes is plotted. It is normalized such that the frequency is $T = 1/f = 1$. The O factor describes the width of the active-high part of the PAM pulse compared to the sample period, i.e., we have

$$p(t) = \begin{cases} 1 & 0 \leq t \leq T/O, \\ 0 & \text{otherwise.} \end{cases}$$

From the equation above and the figure, we can see that the gain also decreases with the O factor, and normally if we apply a return-to-zero scheme, we also

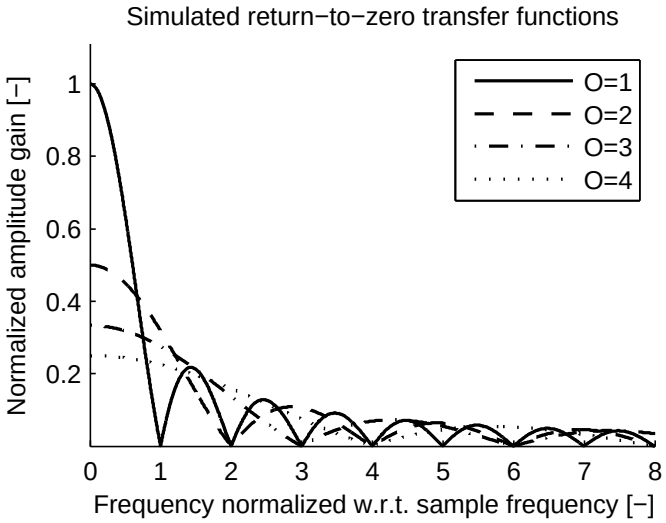

Figure 2.2: Frequency characteristics for different return-to-zero schemes

need to amplify the output of the DAC accordingly to restore the amplitude level. The advantage however - in our case - is that we get a widening of the spectrum and we will pass through high-frequency components (i.e. images of baseband spectrum), such that we can use other Nyquist ranges than that at frequencies below half the sample frequency.

2.2 Current-Steering Digital-to-Analog Converters

Current-steering digital-to-analog converter architecture is the primary choice for the high speed applications such as telecommunication DACs. It has the benefit of not necessarily requiring an output buffer for high performance. The current-mode operation copes with the slew-rate problem of which other DAC architectures suffer. It directs almost all of its current to the output, which means high efficiency [15, 18]. The block diagram of a binary weighted current-steering DAC is shown in 2.3. Each bit of the input digital word controls the appropriate current to the output. I_u represents the least significant bit current, Z_L the impedance load, and I_p and I_p are the positive and negative output current respectively. V_{out} is the differential output voltage. As illustrated in Fig. 2.4, there is normally a relationship between resolution and frequency in digital-to-analog converters [19–23]: with higher frequencies, the linearity decreases [20, 24].

However the drawback is the limited unit current source output impedance, which makes the total output impedance of the DAC input-code-dependent [20, 24, 25]. This gives rise to the non-linearity of the DAC and therefore limited

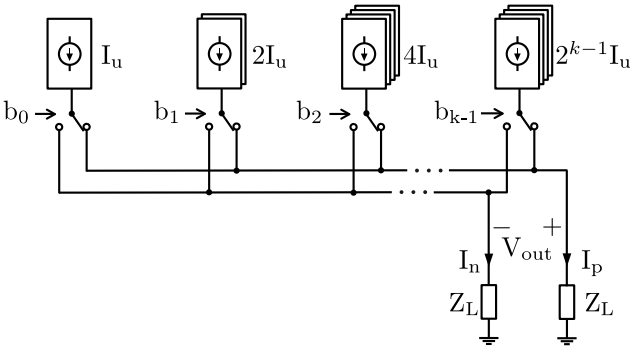

Figure 2.3: Block diagram of a binary weighted current-steering DAC in differential mode

Figure 2.4: Trade-off between frequency and resolution

spurious-free dynamic range (SFDR). In the current-steering DAC, the current sources will have a limited output impedance. For a linear system, this would not cause us any major issues, it would just result in a gain error in the output. There would only be a loss of signal power due to the unmatched impedance levels. However, as the output impedance varies with signal level, it affects the linearity significantly. The output voltage is dependent on the code as

$$V_{out}(X) = i_{out}(X) \cdot \frac{Z_L}{1 + Z_L/Z_S(X)}, \tag{2.2}$$

where Z_L is the load impedance and Z_S is the output impedance of the DAC which is in the unbuffered current-steering DAC also a function of input code, X [20]. Each current source will have a unit output impedance, Z_0, and if the corresponding weight is 2^n, the effective output impedance will be $Z_{unit}/2^n$. We can generalize this and say that if the code X is applied to the DAC there will be X current sources connected to the output and hence the effective output

impedance will be $Z_s = Z_{unit}/X$. This means that the output voltage can be written as:

$$V_{out} = \frac{i_{unit} \cdot X \cdot Z_L}{1 + \frac{Z_L}{Z_{unit}} \cdot X} = \frac{\Delta V \cdot X}{1 + X/\rho} \tag{2.3}$$

where we have set $\Delta V = i_{unit} \cdot Z_L$ as our least significant bit (LSB) voltage step at the output of the DAC and $\rho = Z_{unit}/Z_L$ is the ratio between output and input impedance of a unit source. The equation above is nonlinear with respect to the input code X and distortion will be introduced: the harmonic distortion (HD) will depend on the impedance ratio and the amplitude. The peak amplitude, X_0, is given by the number of bits in the DAC as $X_0 \approx 2^N$. The full-scale output current is $i_{unit} \cdot X_0$, and quite often we have levels around $i_{unit} \cdot X_0 \cdot Z_L \approx 1$ V. The ρ value is quite likely large, but for a higher number of bits, the X_0 grows larger too. The problem is also that the ρ decreases steadily with higher frequency. It can be shown [20] that the third order distortion for a differential DAC can be approximated as

$$HD_3 = 40 \cdot \log_{10} \rho - 12 \cdot (N - 2). \tag{2.4}$$

So, for an output impedance of 100 MΩ, the harmonic distortion becomes some 45 dB for a 14-bit DAC. For a 12-bit DAC it becomes 57 dB. If the output impedance is some 100 MΩ at 10 kHz and the load is 50 Ω, we get $HD_3 \approx 110$ dB. Assuming a slope of 20 dB per decade, we will at 1 MHz have 1 MΩ output impedance, resulting in $HD_3 \approx 70$ dB, etc. Major challenges are therefore to increase output impedance of the converter and/or to lower its load impedance.

2.3 Examples on High-Speed DAC Techniques

In this section a few techniques for high-speed digital-to-analog converters namely interpolating DACs, ΣΔ DACs, time-interleaved DACs and RFDACs will be briefly reviewed.

2.3.1 Interpolating Digital-to-Analog Converters

The digital interpolating DAC is indeed a normal, Nyquist-rate DAC combined with a digital interpolator. The ratio between the sample frequency (f_s), and the signal bandwidth (f_b), is normally identified as the oversampling ratio OSR = $f_s/2f_b$. In a Nyquist-rate converter, the oversampling ratio is unity, i.e., OSR = 1. The signal-to-noise ratio will be enhanced linearly with oversampling ratio. It can be shown, [20], that the in-band signal-to-noise ratio (SNR), or signal-to-quantization noise ratio (SQNR) is approximately

$$\text{SQNR} \approx 6.02N + 1.76 + 10\log_{10}(\text{OSR}), \tag{2.5}$$

where N is the number of bits of. The equation holds when we can guarantee all poles of the modulator to be placed in zero.

In the case of analog interpolation we try instead to mimic the desired analog output waveforms by for example microstepping methods as in e.g. [26, 27] or by using return-to-zero schemes which effectively introduce similar kind of zero-padding as the digital interpolation does, but with maintained requirements on the analog filters.

The return-to-zero scheme, i.e., using a PAM waveform which is unity for $0 < t < T/2$ rather than $0 < t < T$, as effectively gives you zero padding and a form of interpolation. The inverse clock signal can be used to "easily" create the zero padding. Notice, that the PAM waveform is still defined such that it has the same sample frequency as the brick-wall one. Advantages with the return-to-zero scheme is that we reduce both analog settling memory effects, as well as memory effects inside the digital logic, thus improving linearity and noise.

2.3.2 ΣΔ Digital-to-Analog Converters

ΣΔ modulators are attractive in many ways: they truncate the word length of the digital input word to the DAC and the error introduced by this operation is spectrally shaped to out-of-band frequencies [28, 29]. A simplified picture of a ΣΔ modulator is found in Fig. 2.5 where the word length is reduced from N bits down to M where M is usually much smaller than N. By filtering out this quantization noise which is outside the signal band we land at the original resolution within the band [30, 31].

ΣΔ DACs are also attractive since all operations are (unlike for ADCs) done in the digital domain. However, it is also highly nonlinear and has high gain in the feedback loop making it hard to analyze and stabilize. ΣΔ DACs

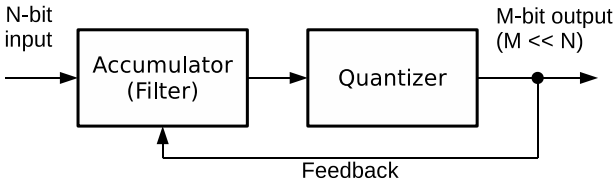

Figure 2.5: Simplistic view of a ΣΔ modulator

require a fairly high oversampling ratio between the sample frequency and signal bandwidth such that the added quantization noise can be moved far enough out-of-band and then filtered out with low complexity filters. If we for a moment neglect the complexity of the analog filter, the reduction in number of analog components using a ΣΔ modulator is enormous. For example, if we have a 16-bit converter, we need $2^{16} \sim 65000$ components in a Nyquist-rate converter. By allowing ourselves a certain amount of oversampling we can now trade frequency against analog complexity. For example by allowing an oversampling of 16 times and apply a modulator with a third-order transfer function, we can reduce

the number of components to approximately $2^6 \sim 64$, i.e. 1000 times less components. With less analog complexity the design becomes simpler, more regular and accurate, even though the analog accuracy requirements are the same in terms of linearity and in-band noise. With a lower number of analog components we can design for high-speed and apply dynamic element matching (DEM) techniques [32–35]. These techniques use randomization to cancel out signal-dependent components and transforming this energy into noise. It should be mentioned that for example digital pre-distortion (DPD) required to linearize the PA will need a bandwidth a couple of times wider than the signal band for proper cancellation of harmonics. To not destroy the properties of the DPD we cannot narrow down our bandwidth through the DAC too much. Researchers at MIT have however developed wideband digital $\Sigma\Delta$ modulators for high-speed applications with global feedback paths and still reached for example 200 MHz bandwidth at 5.25 GHz [10].

2.3.3 Time-Interleaved Digital-to-Analog Converters

Another way to increase the overall frequency is to use time-interleaved converters [36–38], as outlined in Fig. 2.6 which consist of several (three in the figure)

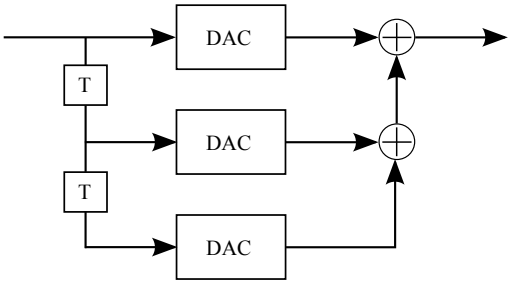

Figure 2.6: Example of three time-interleaved DACs

DACs connected in parallel by summation of the outputs. The DACs operate at time shifted clocks, but same frequency. By carefully generating the time shifts with high accuracy PLL and DLL, we could for example let all the DACs operate at say 1 GHz, but with a 120-degree phase shift between each other, thus outputting data at 3 GHz in total. The overall signal transfer function will be weighted by the following z-transform:

$$H(z) = 1 + z^{-1} + z^{-2} = \frac{z^2 + z + 1}{z^2}. \tag{2.6}$$

where a pair of complex zeros are introduced in the frequency domain. Thereby the spectrum will be attenuated accordingly and certain frequency bands become distorted. However, if we are able to control the positions of these zeros, and/or keep our signal out of those bands, we still quite likely have a competitive solution to reach high-speed conversion.

2.3.4 Radio-Frequency Digital-to-Analog Converter

As the name suggests, the radio-frequency digital-to-analog converters (RF-DAC) is a high frequency DAC of which the synthesized output signal is at radio frequency (RF). This technique was proposed in [1], for high-speed and high-resolution data conversion. It uses different type of pulse waveform in the DAC to generate the higher frequency lob in the frequency response of the DAC and hence utilizes the signal images at those high frequency lobes as the DAC output instead of Nyquist image. In Fig. 2.7, a traditional pulse amplitude modulation in conventional Nyquist DAC, return-to-zero interpolating DAC, and return-to-zero "ping-pong" DAC is shown. In Fig. 2.8, the oscillatory DAC

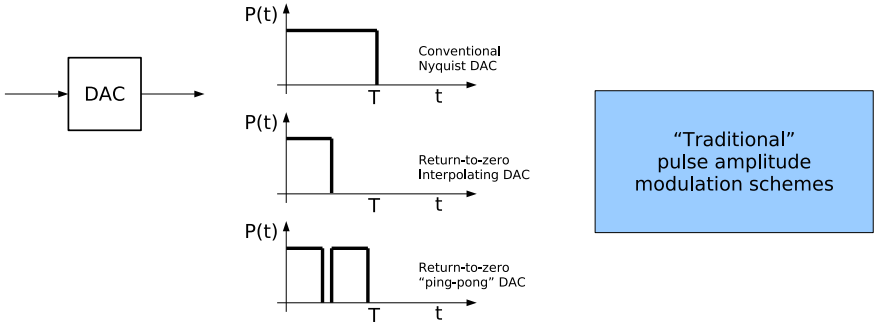

Figure 2.7: "Traditional" DAC output waveforms

output proposed in [1], with sinc pulses at twice the sample rate, three time the sample rate and at twice the sample rate bipolar, in shown respectively.

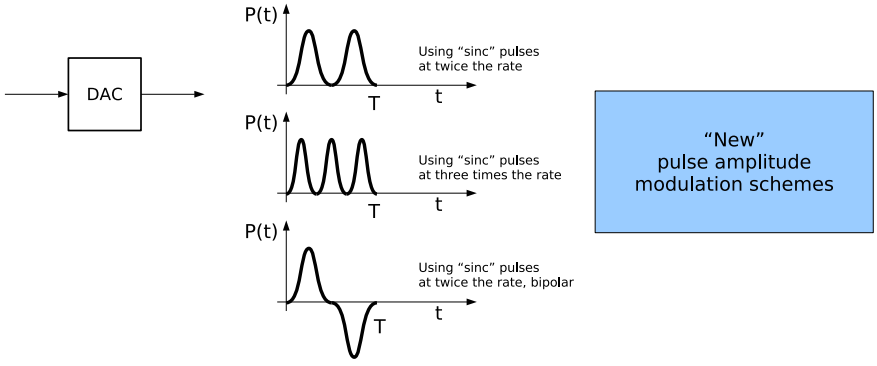

Figure 2.8: "New" DAC output waveforms

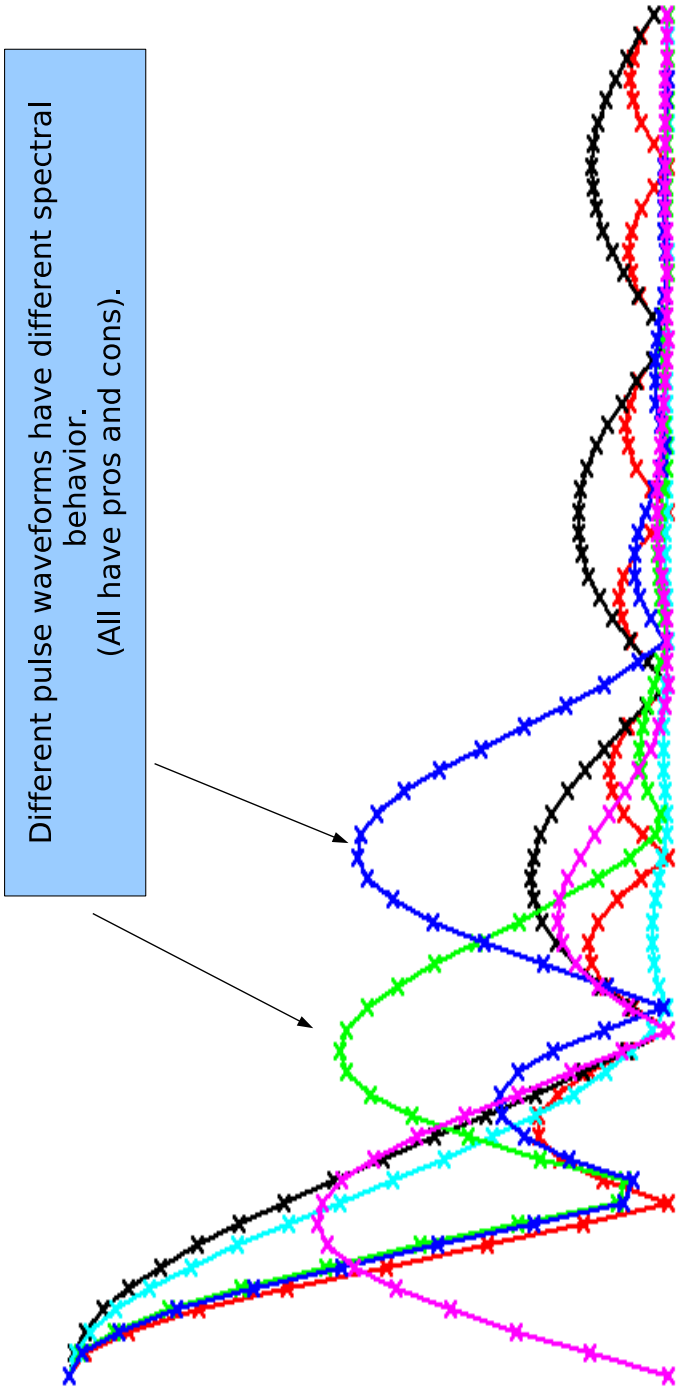

Figure 2.9: Different pulse waveforms

Different pulse waveforms have different spectral behavior as it is illustrated in Fig. 2.9. Each of these DAC output spectrums has their own pros and cons. However it is observed here that by selecting the pulse rate and the sample rate in a proper ratio we can allocate the lobes over the signal images (which are at integer multiples of the sample frequency) and hence utilize the higher frequency images as the output of the DAC.

The radio-frequency digital-to-analog converter techniques and different architectures as well as the proposed architectures will be be investigated more in detail in chapter 3.

Chapter 3

Radio-Frequency Digital-to-Analog Converters

3.1 Background

In direct-conversion architecture transmitters, the digital signal from a digital signal processor (DSP) is converted to an analog signal through a digital-to-analog converter and then low-pass filtered to remove the unwanted aliasing images. Then with the aid of mixers, the signal will be converted directly to the RF carrier signal.

The idea with the radio-frequency digital to analog converter (RF DAC) is to combine the mixer with the DAC in a clever way i.e. by reducing the number of analog components. We illustrate this in Fig. 3.1 where parts of the baseband, the DAC, filters, mixers and optionally the final bandpass filter can be merged. One result of this operation is that the digital sampling speed, as well as the requirements on linearity and frequency selectivity increase quite dramatically.

3.1.1 DAC and Mixer

The most intuitive approach is to combine the DAC directly with a mixer. This will constitute a traditional way of modulating and transmitting. The ambition should be to push the DAC closer to the antenna by preferably increasing its sampling frequency as much as possible. We also want to push the mixer closer to the DAC such that we can remove the resistive load at the output of the DAC. The left-most part of Fig. 3.2 shows an example of a DAC element merged with a passive mixer (passive in the sense that there is no gain associated with it). For this purpose we integrate the mixer close to the DAC and without the resistive load. The current-to-voltage-to-current conversion - which introduces distortion - is avoided. The load impedance is also reduced by sinking the DAC output currents in the low-impedance drains of the mixer transistors. In the right-most part of Fig. 3.2 we find an active implementation of the mixer DAC.

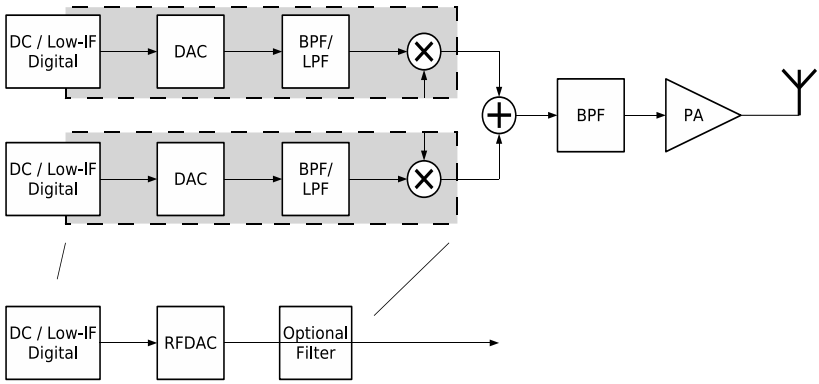

Figure 3.1: Illustrating the boundaries of the RF DAC

In this case we have actually illustrated this with a single unit element of the DAC. Then, several of these units must be connected in parallel to achieve the overall functionality of the DAC. The static output current is given by

$$i_{out}(t) = X(n) \cdot i_{unit}, \tag{3.1}$$

and to be more accurate we need to include the pulse-amplitude modulation (PAM) waveform in the expression and we get

$$i_{out}(t) = \sum_{\forall n} i_{out}(n) \cdot p(t - nT) = \sum_{\forall n} i_{unit} \cdot X(n) \cdot p(t - nT), \tag{3.2}$$

where, for example, $X(n) = X_0 \cdot \sin(\omega_1 Tn)$, could contain the signal information and $p(t)$ could be the brick-wall function or a return-to-zero. Now, assume that i_{unit} instead is a time-dependent oscillating signal as

$$i_{unit}(t) = i_{unit,0} \cdot q(t), \tag{3.3}$$

where $q(t)$ is an additional pulse-amplitude modulation signal at a frequency which is a multiple of the sample period, T, i.e., $q(t) = q(t + kT)$. (Selecting a multiple of the sample period, minimizes the glitches.) We can now write the output current as

$$i_{out}(t) = \sum_{\forall n} i_{unit,0} \cdot X(n) \cdot q(t) \cdot p(t - nT), \tag{3.4}$$

or

$$i_{out}(t) = i_{unit,0} \cdot q(t) \cdot \sum_{\forall n} X(n) \cdot p(t - nT). \tag{3.5}$$

If $q(t)$ now is given by the local oscillator (LO) signal, $\sin(\omega_0 Tn)$, we see that the mixed products at $\omega_0 \pm \omega_1$ are produced such that we can center the signal information at higher frequencies.

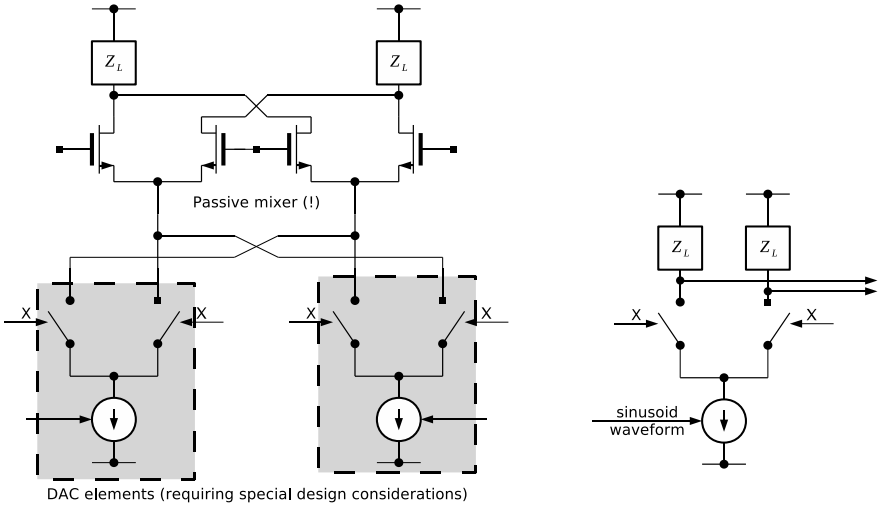

Figure 3.2: Two examples of unit DAC element integrated with mixers, one with passive mixer on output (left) and one with active mixer on input (right).

In a general case, if we assume $x_r(t)$ as the reconstructed signal, we have

$$x_r(t) = \sum_{\forall n} X(n) \cdot p(t - nT), \tag{3.6}$$

Ideally, $p(t)$ should be a sinc function, i.e., $\sin(t)/t$, such that a brick-wall filtering is obtained which band-limits the signal to Nyquist range. However, in conventional Nyquist-rate DACs (using a zero-order hold technique) $p(t)$ is typically a rectangular-shaped pulse that results in a sinc weighted frequency characteristics.

In the approach used in [1], an oscillatory pulse is embedded in the PAM pulse, $p(t)$. The signal spectrum of their proposed pulse waveform in the frequency domain turns out to be very interesting. Assume that we have a PAM waveform as

$$p(t) = \begin{cases} 1 + \cos(\omega_0 t) & |t| \leq T/2 \\ 0 & |t| > T/2, \end{cases} \tag{3.7}$$

where we currently allow the function to also take negative time values. Here, ω_0 is a certain angular frequency, typically associated with multiples of the sample frequency and T is the time duration of the pulse, which typically is given by $T = 1/f_s = 2\pi/\omega_s$, where f_s is the sample frequency and ω_s is the sample angular frequency. The corresponding Fourier transform of the PAM waveform in (3.7) can be written as

$$P(j\omega) = T\frac{\sin\frac{\omega}{2f_s}}{\frac{\omega}{2f_s}} + \frac{T}{2}\frac{\sin\frac{\omega-\omega_0}{2f_s}}{\frac{\omega-\omega_0}{2f_s}} + \frac{T}{2}\frac{\sin\frac{\omega+\omega_0}{2f_s}}{\frac{\omega+\omega_0}{2f_s}}. \tag{3.8}$$

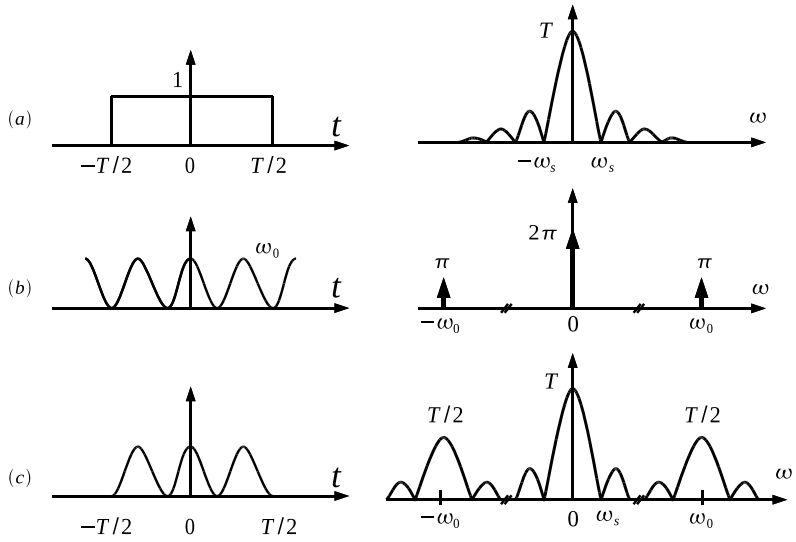

Figure 3.3: Frequency characteristics of a (a) brick-wall, (b) sinusoid, and effect of (c) combined brick-wall and sinusoid waveforms.

Figure 3.3 shows how different pulse waveforms affect the output spectrum. In Fig. 3.3(a), we find the effect of the traditional, practical brick-wall pulse. The spectrum is sinc-weighted and attenuated images are found over the frequency domain.

In Fig. 3.3(b), we illustrate the relationship between time domain and frequency domain for a sinusoid and in (c) the combined waveform is shown, as also described by (3.7) and (3.8), respectively. The output spectrum of the signal, say $X(j\omega)$ will be multiplied by the $P(j\omega)$ from (3.8) and hence the higher Nyquist range (at ω_0) can be utilized instead of the original Nyquist band.

As can be seen, there is a loss of signal power, but in terms of in-band signal-to-noise ratio (SNR), there is no loss, as the output quantization noise of the DAC is attenuated as well. The component will however be more sensitive to circuit noise and other external factors.

3.2 Finite-Image-Rejection Problem

Direct-digital-to-RF converters of IQ modulators have an intrinsic finite-image-rejection characteristic [39], that will be theoretically discussed in this section. This discussion is part of the Paper D in this thesis. A conventional I/Q modulator is shown in Fig. 3.4. In this transmitter in-phase (I) and quadrature-phase(Q) digital signals are converted to analog signals through a conventional digital-to-analog converter and after low-pass filtering to remove unwanted remaining of images, they are mixed with orthogonal LO signals to be shifted

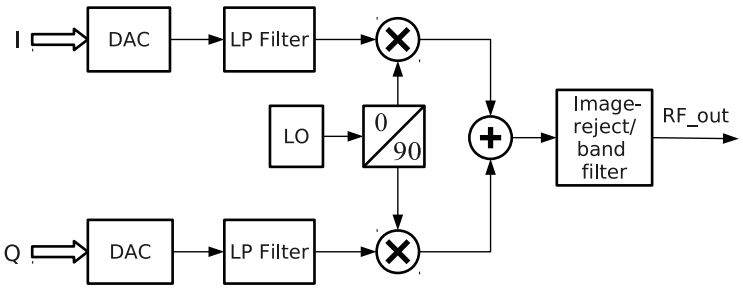

Figure 3.4: Conventional I/Q modulator.

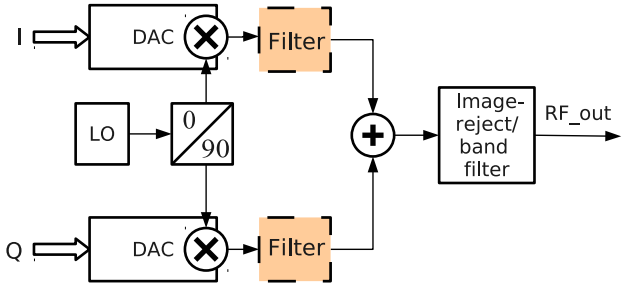

Figure 3.5: Digital-RF modulator.

to higher frequencies. The summation of the signals at this point removes the unwanted sideband and we achieve a single sideband (SSB) signal to pass to the antenna. Apart from the filtering problem of spurs emission, the DRFC has an intrinsic characteristic regarding the rejection of the sideband or clock alias image of the IQ modulation. This problem was not present in the conventional IQ modulators since the unwanted images are removed utilizing low-pass filters after the DAC (reconstruction filters) and hence it removed the effect of *sinc* function ($sinc(\theta)$ defined as $sin(\theta)/\theta$) roll-off associated with the DAC response. Finite image rejection can degrade the performance in terms of error vector magnitude (EVM) in a digital modulation scheme. In this paper we are going to conceptually study the origin of the finite image rejection and possible techniques to overcome the problem.

Digital-to-analog conversion can be modeled mathematically by pulse-amplitude modulation (PAM) as

$$y(t) = \sum_{m=-\infty}^{+\infty} x[m]p(t - mT), \tag{3.9}$$

where x[m] and y(t) denote the digital input and analog output respectively and

$p(t)$ is the modulation pulse. In frequency domain this equation, using Fourier transform, is written as

$$Y(j\omega) = X(e^{j\omega T})P(j\omega). \tag{3.10}$$

To achieve an ideal conversion the pulse $p(t)$ must be a *sinc* function. This however is not practically possible due to the non-causality of the *sinc* pulse. The conventional choice of $p(t)$ has been a rectangular pulse. In this way the spectrum of the digital signal, repeated every sample frequency ω_S is weighted with a *sinc* function (the spectrum of rectangular pulse, $P(j\omega)$) which has its zeros at integer multiples of ω_S. To remove unwanted, to some extend attenuated images by *sinc* roll-off, low-pass analog reconstruction filters should be used as also shown in Fig. 3.4.

3.2.1 Oscillatory PAM

Suggestions of other $p(t)$ pulses has led to the introduction of oscillating waveforms. A sinusoidal pulse can be used as $p(t)$ in order to produce a high-frequency lobe in $P(j\omega)$, which can be located over the higher frequency images of the analog signal [1].

Utilizing the RFDAC idea of [1], together with a $\Sigma\Delta$ modulator, an I/Q modulator is proposed in [10]. The I and Q digital signals are modulated with $p_i(t)$ and $p_q(t)$ respectively. The resulting modulated signal can be formulated as

$$x_{RF}(t) = \sum_{m=-\infty}^{+\infty} i[m]p_i(t - mT) + q[m]p_q(t - mT). \tag{3.11}$$

Taking Fourier transform from both sides we get

$$X_{RF}(j\omega) = \sum_{m=-\infty}^{+\infty} i[m]P_i(j\omega)e^{-j\omega mT} + \sum_{m=-\infty}^{+\infty} q[m]P_q(j\omega)e^{-j\omega mT}. \tag{3.12}$$

Finally the RF quadrature modulated signal can be noted as

$$X_{RF}(j\omega) = I(e^{j\omega T})P_i(j\omega) + Q(e^{j\omega T})P_q(j\omega). \tag{3.13}$$

Figure 3.6 illustrates the $p_i(t)$ and $p_q(t)$ signals. $p_i(t)$ is a windowed sinusoidal signal that can be theoretically decomposed into a pure sinusoid and a rectangular function and consequently the frequency spectrum of this pulse, i.e., $P(j\omega)$ is the convolution of a *sinc* with Dirac delta functions. As shown in Fig. 3.6 this results in spectrum that has higher frequency lobes at positive and negative sides. One may argue that the average value of this pulses are non-zero

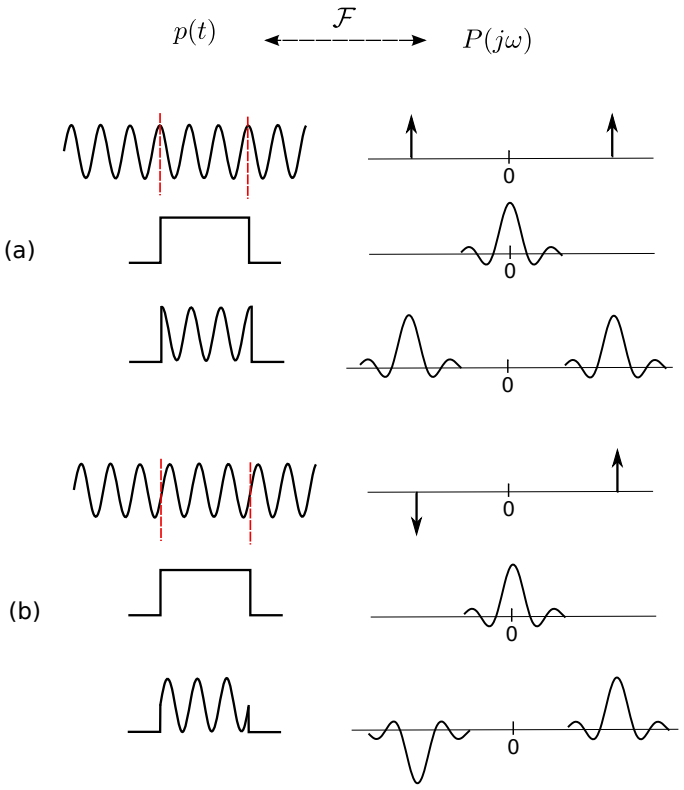

Figure 3.6: Windowed PAM of I and Q.

and hence you should also get another lobe centered at zero frequency. That is actually true but since this effect appears on both I and Q signals in the same way it will not affect image rejection issue which is the main focus of this paper. To clarify the image problem in details, a color coded illustration is depicted in Fig. 3.7. The tail of the *sinc* function, of $P(j\omega)$, at negative frequencies is continued to the positive frequencies and affect the I and Q signals. For instance, the I signal at ω_{LO}, is shaped not only by the main lobe of the *sinc* function (shown in black) but also with the tail of the other *sinc* function, shown in red in Fig. 3.7.

For the sake of simplicity the I signal influenced by the main lobe and the one influenced by the tail of the "sinc", is decomposed into two versions of the I signal as shown in Fig. 3.8. Now there are main replicas of the signals and attenuated versions. The phase of the attenuated versions of the I and Q signals are not maintained orthogonal anymore and once they are added together, do not cancel the mirrored images.

Figure 3.9 shows the I and Q signals in one diagram. As can be observed, the replicas of the main signals and its images cancel out completely. But this

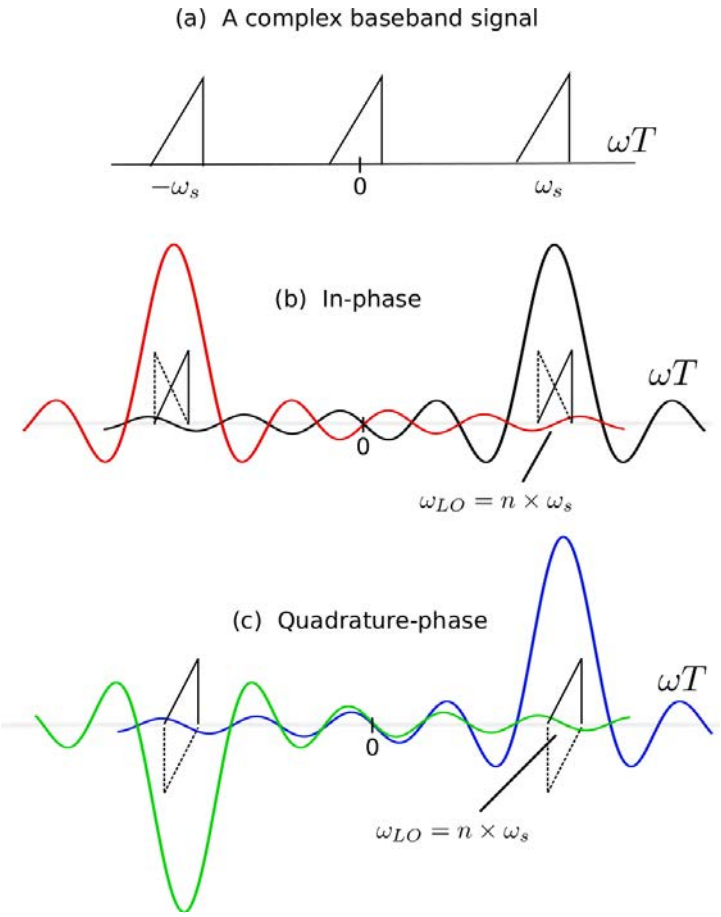

Figure 3.7: Decomposing a SSB complex signal into I and Q signals together with PAM spectrum of the I and Q, LO.

is not the case with the attenuated (and flipped) versions of the signals. They do not cancel each other but add together and acts as the sideband image of the main signal, on both negative and positive frequencies. The image rejection is defined as the power ratio between wanted signal and unwanted sideband signal (IRR). The image rejection is increased if the oscillatory pulse $p_i(t)$ signal frequency ω_{LO} is selected larger. However there are other issues from requirement specification to implementation constraints that prevents arbitrary selection of the output signal's frequency.

The finite image rejection issue is a strong function of the PAM pulse selection. If the $p(t)$ pulse is selected such that its respective frequency spectrum has a better filtering behavior then the effect of the image interference will be more faded. Moreover a filtering characteristic of the PAM will also be bene-

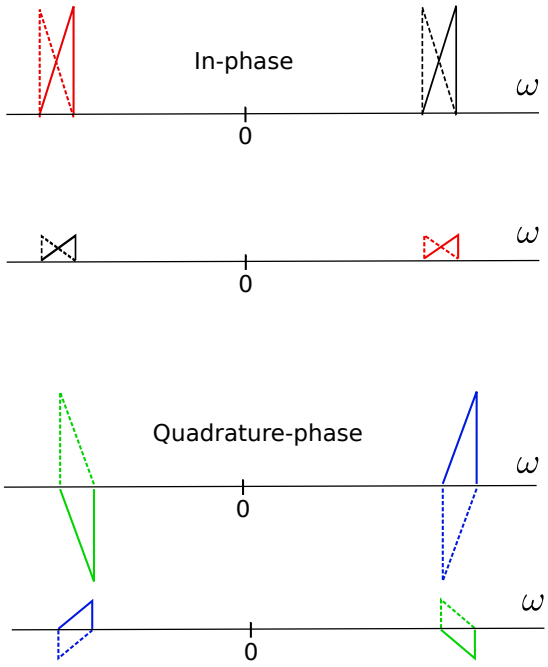

Figure 3.8: Outcome of the DRFCs; the signals affected by the I and Q PAMs plotted in separate axes.

ficial when there is a $\Sigma\Delta$ modulator preceding the digital-RF converter since large magnitude spurs needs to be suppressed to be able to meet respective spectral emission masks of the application. A discrete-time oscillatory signal $p(t)$ is suggested in [40]. Due to digital nature of producing such a pulse, it can be optimized to have the best filtering characteristic at its spectrum.

Different types of mismatch can be addressed in digital-RF converters. Timing errors in digital input transitions, amplitude and phase mismatch between quadrature LO signals, cell to cell mismatches of the converter, all results in imbalance between the I and Q arms. The alignment of digital data transition and oscillatory signal here is very important and misalignment will give rise to image power.

3.2.2 Conceptual Illustration

Assume that we have a complex baseband signal that is symbolically shown in Fig. 3.7a. In digital domain the complex signal is mapped to a digital modulation scheme, splitting the real and imaginary part of this complex signal (that constitutes the I and Q). This is conceptually illustrated in Fig. 3.7b-c. Each branch of I and Q then is modulated with a digital-RF converter and according to Eq. 5, the I and Q digital signals are shaped according to the $P_i(j\omega)$ and

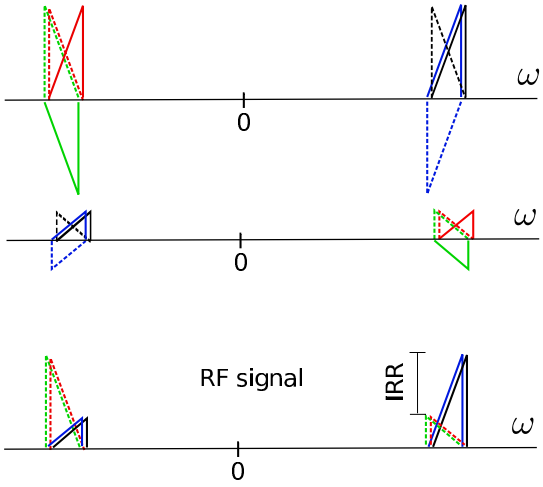

Figure 3.9: Conceptual illustration of the IQ modulator output signal, when I and Q are added, and the finite image rejection.

$P_q(j\omega)$ spectrum and then summed finally together at the output.

3.2.3 Alleviate the Image Spur Problem with Digital IF Mixing

The finite image rejection issue is raised from asymmetric shape of the *sinc* functions tail (from negative frequencies) around the RF center frequency. This is clearly illustrated in Fig. 3.7. As can be observed, the signal is experiencing the *sinc* function in opposite phases on each side of the RF center frequency. By using quadrature digital mixing, before applying the signal to DRFC, we can center I and Q signals at intermediate frequency (IF) of $f_s/4$ [10]. Hence the I and Q signals undergo the same amount of attenuation with identical phase and therefore the I and Q addition can effectively remove the side band image. However, the main lobe of the *sinc* function still affects the signals unevenly if the signals are not at *sinc*'s center frequency. This effect is however easily correctable with conventional anti-*sinc* pre-emphasis filters. Another advantage of using digital-IF mixing is to avoid the clock feedthrough which is located at the RF center frequency. Digital-IF mixing to $f_s/4$ is a digital multiplier-free quadrature modulation that utilizes a multiplexer to implement multiplication by 1, -1 and 0 [41–44]. This technique is very hardware and power efficient.

3.3 RFDAC with Sinusoidal Interpolation

A pseudo-analog interpolation technique to design DACs is proposed in [26]. In this technique, a linear interpolation function is realized such that a linear transition is obtained between two consecutive samples, rather than applying the

brick-wall pulse. For example, the continuous-time waveform between samples $x(nT-T)$ and $x(nT)$ can be written as

$$x_r(t) = x(n-1) + (x(n) - x(n-1)) \cdot \frac{t-(n-1)T}{T}, \tag{3.14}$$

for $(n-1)T < t \leq nT$ in this particular case. To obtain this linear interpolation, a kind of microstepping in [26] is used. At a frequency L times higher than the sample frequency, the analog output is updated with a slight increase in amplitude to eventually reach the appropriate level upon arrival of the next sample at the original sample frequency. The PAM pulse includes, in this case, a ramp and its spectrum is expected to be shaped as sinc^2. The attenuation of out-of-band images at higher frequencies would then be approximately doubled in terms of decibels thus motivating a lower complexity in the analog reconstruction filter [26]. However, it also impacts the usable frequency range, as the data needs to be restricted to a more narrow band, eventually resulting in a fairly low-bandwidth DAC implementation.

Figure 3.10 illustrates three different interpolation waveforms in the time domain. In (a) the linear interpolation waveform as proposed in [26] is shown illustrating the microstepping approach. In (b) we find the approach used in [1] with continuous-time waveforms. Fig. 3.10(c) illustrates our proposed approach as further described in Section 3. The proposed approach utilizes the microstepping technique as described in [26] and combines it with the generation of a sinusoid approach. Consequently, the hardware needed for analog oscillatory pulse generation such as voltage-controlled oscillators (VCO), power and area consuming buffers, etc. can be replaced by circuits that are more digital in nature.

3.3.1 RFDAC with Discrete-Time Sinusoidal Interpolation

RFDAC with discrete-time sinusoidal interpolation is the proposed technique in Paper B in this thesis. In addition to the microstepping technique to generate the interpolation waveform, we also quantize the amplitude levels as illustrated in Fig. 3.10(c). In practice, this means that we actually control the PAM waveform with yet another DAC, rather than using the analog VCO as required in [1]. Our figure of merit is to reduce the number of closed-loop analog components and instead offer a direct, digital data stream that can be weighted and combined in the analog domain. The data stream can be generated by a high-speed direct digital synthesis (DDS) phase accumulator [45]. This phase accumulator can potentially also be used in a combination with non-linearly weights in the current source to achieve high speed. As argued above, a DAC with digital generating circuits replaces the oscillatory waveform and essentially we can expect the overall DAC output to behave quite similarly to the continuous-time approach. In Fig. 3.11 we show the main ideas behind the approach in [1] and our proposed approach. In (a) the tail current source is controlled by an analog waveform, typically some kind of sinusoid centered around a DC point, whereas

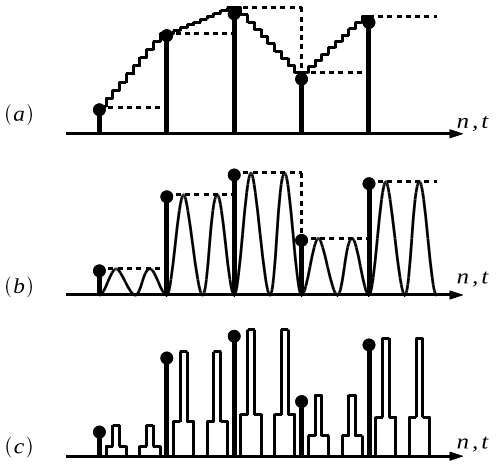

Figure 3.10: Illustration of time-domain behavior for (a) linear interpolation, (b) sinusoid mixing, (c) quantized microstepping of sinusoid waveform.

in (b) we have divided the tail current source into a multiple of sub-current sources that are controlled by digital data streams. The combined current of these sub-sources will generate the total tail current. For the case in Fig. 3.11(a) using a standard CMOS transistor, the tail current will be approximated by

$$I_T(t) = \alpha \cdot (v_{ac} \sin(\omega_0 t) + V_{DC} - V_T)^2 . \tag{3.15}$$

The current contains a DC component, one signal component at ω_0 and one at $2\omega_0$. For our proposed case, as in Fig. 3.11(b), the tail current would instead be given as

$$I_T\left(\frac{nT}{L}\right) = I_{T,0} \cdot \sum_{m=0}^{M-1} W_m \cdot y\left(\frac{nT}{L} + \frac{mT}{L}\right), \tag{3.16}$$

where W_m are the weight ratios of the different current sources and $I_{T,0}$ is a unit current source. The M control signals, y_m, are running at L times the sample frequency, such that the tail current is quantized with respect to both time and amplitude.

In both cases described above the output DAC current is composed by the difference between the two currents at the output of the switches, i.e., $I_D = I_P - I_N$. Further, the switches are controlled by the data signal and the total output current from the DAC - at time point nT - can be written as

$$I_D(nT) = I_T(t) \cdot X(nT) - I_T(t) \cdot \tilde{X}(nT), \tag{3.17}$$

where $X(nT)$ is the digital word and $\tilde{X}(nT)$ its inverse.

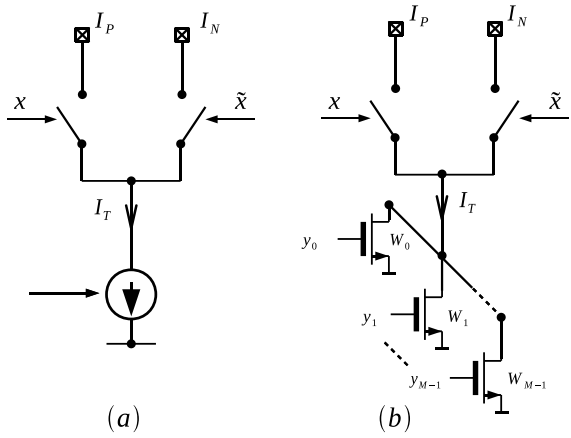

Figure 3.11: Simplified representation of two approaches to perform up-mixing in a current-steering DAC. (a) shows an analog method and (b) a mixed-signal method.

3.4 A Direct-Digital-to-RF Converter Employing Sinusoidal Interpolation and SDFIR

Utilizing a digital $\Sigma\Delta$ modulator in an oversampling D/A converter potentially enables us to achieve the same in-band performance compared to a Nyquist-rate DACs but with fewer DAC unit elements and hence we gain in terms of clocking, signal routing and unit element matching [46]. However, the out-of-band noise will be high and needs to be attenuated before entering the power amplifier in case of a wireless transmitter. This usually puts requirement on the off-chip filters or LC-tank resonator circuits at the output. In order to relax the requirements of these analog filters, we can utilize the SDFIR filter after the $\Sigma\Delta$ modulator which not only performs the actual D/A conversion but also can be structured so that it has a specific filter response suitable for the given application *sinc* function roll-off associated with conventional DACs. Examples of this technique are presented in [47–50]. Furthermore, the RFDAC concept can also be applied to this configuration to relocate the output analog signal to RF frequencies with the aid of mixers embedded in the SDFIR filter taps [3]. Figure 3.12 depicts the signal chain in one of the branches of I or Q of a digital-RF IQ transmitter. First, the input signal, which can be that of I or Q path, is interpolated and then $\Sigma\Delta$ is employed to reduce the number of bits and then the output is fed to a DAC with low number input bits. The digital data is converted into an analog signal and also mixed to higher frequencies with the applied LO signal. The band filter afterwards is required to select the corresponding band.

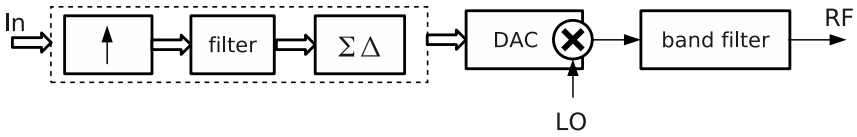

Figure 3.12: Digital to RF converter chain for each I and Q branch.

3.4.1 Discrete-Time LO

An alternative to a continuous-time oscillatory signal applied to the current source unit elements in the RFDAC would be to employ a sinusoid interpolation technique [40]. This can be seen as an additional auxiliary DAC, generating the tail current of the main DAC (unit element). By discretizing the LO signal we still get the higher-frequency lobe of the DAC spectrum in RFDAC concept. This enables us to use the digital images as signal bands rather than the first Nyquist image [1]. The oscillatory LO signal is distributed over all the unit element current sources to realize the mixing stage [3, 10]. This requires huge buffers to drive high swing, high frequency LO signals to the unit elements. In this technique, instead of distributing an analog oscillatory signal to all current sources a fixed-pattern mixing signal is generated by digital circuitry and is applied to the respective weighted sub-elements [40]. That means the continuous time signal is replaced by a low resolution discrete-time signal and still the performance does not degrade and we can save power consumption and area. Moreover, the transmitter will benefit from the technology scaling as it is more digital in nature. Figure 3.11 illustrates the discrete-time LO signal generation with weighted sub-elements, $w_1, w_2 ...., w_m$.

The fixed-pattern digital oscillatory signal generator block can eventually be replaced by a direct digital frequency synthesizer (DDFS) that outputs a set of bits to control a set of non-linearly weighted current sources. This set of non-linearly weighted sources will effectively create a oscillatory tail current in the unit elements of the DAC. Thus it enables us to tune the LO frequency for different wireless communication standards. This is however not discussed in detail in this paper. The proposed IQ transmitter architecture [11], employs the discrete-time LO signal as shown in Fig. 3.13. From a system perspective it can be realized that there are many possibilities to improve the performance by for example sharing filter weights, apply new techniques, since it is the co-design of the DAC, the mixer and the DDFS (to generate the discrete LO signals) altogether.

This proposed architecture is part of the Paper C in this thesis, however only the system functionality of this architecture is studied and approved. Nonetheless, parts of the digital circuitry (such as the DDFS) are operating at quite high-frequency. The LO frequency is generated from the DDFS and thus its clock frequency must be multiples of the LO frequency. This implies that the digital portion could consume quite high power and there could be quite some

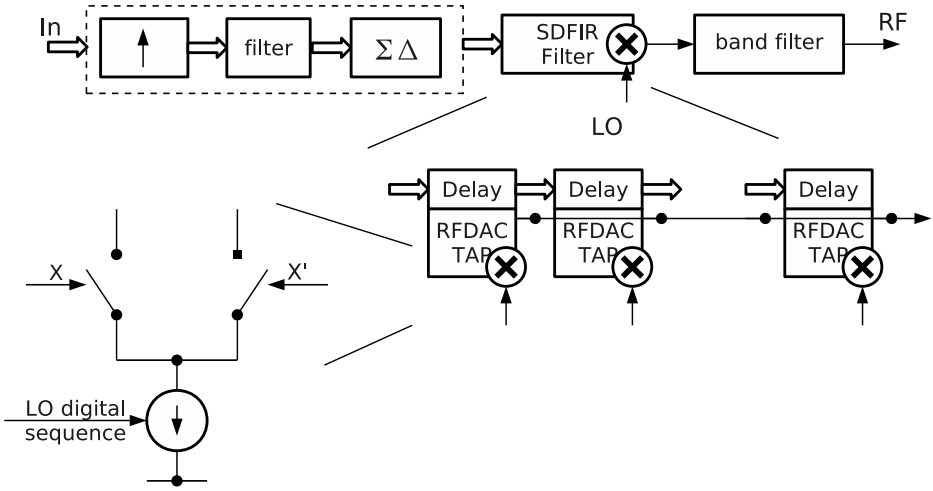

Figure 3.13: Digital-RF converter employing semi-digital FIR filter.

challenge to reach high speed given the CMOS process however since it is digital in nature it will benefit from technology scaling. Previously reported digital-RF converters, utilize a VCO to generate the oscillatory signal. This comes with a fairly high analog cost and offers less room for digitally-assisted innovative techniques. In the proposed approach, owing to the inherently digital nature of the oscillatory signal generation, there is a capacity to enhance the overall performance - both from technology scaling point-of-view and by applying special digital techniques. For instance, mitigating process variations and mismatch in the DAC unit element implementation. According to the RFDAC concept presented in [1], the oscillatory signal does not need to be a perfect sinusoid. There is a trade off where the imperfection in the oscillatory mixing signal ends up as higher-energy signal far-out-of-band images, which can easily be suppressed with a relaxed analog filter. The main concern, however, is the close out-of-band spectrum, which has to be attenuated as much as possible. There are different approaches for this problem, suggested in the publications: employing a bandpass ladder filter with LC resonators [2, 10, 51] or utilizing the embedded SDFIR reconstruction filter [3]. In the former approach, any deviation of the LC values from their nominal values results in a shift of the filter center frequency and a large amplitude loss within the RF band. In the latter approach, however, typically a large number of filter taps is needed to obtain a filter response that satisfies spectral emission mask specification of the targeted communication standard. A large number of taps is specially problematic in an RFDAC concept where a high frequency LO signal should be distributed to a large amount of unit elements. Although in the proposed architecture we use a SDFIR filter approach, the huge LO buffers problem is circumvented since we only need to bring digital controls to the edge of the unit element

switches. Therefore, the SDFIR filter can have a more number of taps to obtain the required response for the spectral emission than in [3]. The micro-stepping oscillatory signal generated as LO is exploited in the SDFIR filter. Another potential for improvement in this architecture is that the filter coefficients can be propagated towards and be combined with the digital oscillatory signal generator weights. Therefore there is room for co-optimization of the digital oscillatory signal generator and the SDFIR filter coefficients.

3.4.2 Semi-Digital FIR Filter Design

The semi-digital FIR filter is implemented with the aid of weighted subDACs in each taps. The weight of the each subDACs is equal to the SDFIR filter coefficient. In case of a one bit quantizer at the output of the $\Sigma\Delta$ modulator, each subDAC in the filter taps will become a current source weighted according to the SDFIR filter coefficients. Since we use a unit element current source, the filter coefficients needs to be integer number. Therefore the passband gain of the SDFIR filter should be larger than one to allow integer coefficients for the filter. Usually there are spectral emission mask for different transmitters to be fulfilled. In this paper, we have chosen wide-band CDMA standard to demonstrate the feasibility of the proposed IQ modulator. The maximum magnitude deviation of the filter response in the stopband can therefore be derived from the spectral emission mask requirement. The total number of unit elements in a general purpose DAC is proportional to the resolution of the DAC. In a SDFIR filter the resolution, i.e., signal-to-noise ratio (SNR), is independent of the total umber of unit elements. Therefore the total number of the unit elements should be minimized as objective function of the optimization problem. Moreover the $\Sigma\Delta$ modulator noise transfer function can also be included in the optimization problem. The SDFIR filter problem is formulated and solved with a quadratic solver. The resulting SDFIR filter is used in the next Section for the proposed IQ modulator. The objective in this optimization problem was to minimize the emitted noise in the stopband so that the requirement on the filter after the IQ modulator is relaxed. This is done by using the stopband energy as the objective function of the optimization problem while the passband ripples is set as the constraint.

Chapter 4

Semi-Digital FIR Filters

4.1 Introduction

sigma-delta ($\Sigma\Delta$) modulators are attractive in digital-to-analog converter (DAC) where the signal bandwidth is relatively small compared to the sample frequency. Using the digital $\Sigma\Delta$ modulator we can effectively lower the number of data bits in the DAC and use a less complex set of analog components [52]. In fact, by employing oversampling and digital $\Sigma\Delta$ noise shaping, higher effective resolution can be achieved from a nominally lower-resolution DAC. One of the costs, however, is a higher quantization noise which is ideally spectrally shaped to out-of-band frequencies by the modulator. In oversampling DACs the base-band data is up-sampled and digitally filtered, hence a lower sinc attenuation in the pass-band is achieved. Moreover the transition band between the main image and the sinc-weighted image is also increased, which in turn reduces the requirement on the following analog reconstruction filter [12]. The oversampling DAC can be replaced, as shown in Fig. 4.1, with an interpolating stage, digital $\Sigma\Delta$ modulator and a semi-digital finite-impulse response (FIR) filter [49]. In this configuration, the N-bit base-band data is up-sampled and filtered through the interpolation and then applied to the digital $\Sigma\Delta$ modulator. The output of the $\Sigma\Delta$ is an M-bit signal where M would typically be significantly smaller than N. The M-bit data is converted to analog through the semi-digital FIR (SDFIR) filter and the resulting analog signal is then filtered with analog reconstruction filter to remove the images at integer multiples of the sample frequency [53]. The output voltage, or current, will be fed forward to an analog output driver.

The type of DAC that we consider in this work typically finds its place in transmitters for telecommunication applications [12]. In wireless communication systems, to ensure that the transmitter out-of-channel emissions remain sufficiently small, a spectral emission mask is defined [54, 55]. To fulfill this requirement, in presence of spectrally shaped out-of-band noise, usually bulky

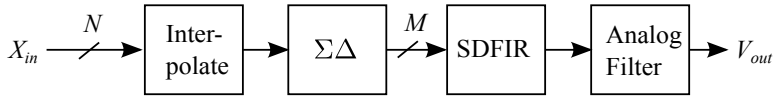

Figure 4.1: Block diagram of interpolation, ΣΔ modulator, DAC and filtering stages in a transmitter chain.

and expensive off-chip components (for instance, surface acoustic wave (SAW) filters) are required. These components increase the overall system cost and power consumption especially in multi-band application [56]. To mitigate some of this cost and complexity, the DAC can be structured in a semi-digital FIR filter configuration so that it utilizes the frequency selective filtering behavior of FIR filters [20, 49, 50, 57]. The semi-digital FIR filter architecture provides both analog filtering as well as digital-to-analog conversion. Although, in most telecommunication applications, the attenuation provided by a semi-digital FIR filter in the transmitter path does not totally resolve the out-of-band noise suppression problem, it relaxes the tight requirement on the expensive off-chip SAW filters or the succeeding analog filter. Semi-digital FIR filters, used as filters and data converters and implemented as switched-capacitor network or in current-mode (current-steering) architectures, have been previously reported previously [20, 49, 50, 57–59].

For instance, in [49], a semi-digital FIR filter is designed to target the elimination of the out-of-band noise caused by a preceding second-order ΣΔ modulator. The semi-digital FIR reconstruction filter is of order 128, followed by a single-pole low-pass filter. It achieves an out-of-band quantization noise energy suppression of 72 dB using a 6-bit accuracy in the filter coefficients.

In [50], a current-mode semi-digital FIR filter with 60 identical, non-zero tap coefficients has been reported with a total number of 180 current sources (three per tap). Due to the moving-average operation of this filter, the filter will have a sinc roll-off behavior which does not provide enough suppression, although it has other advantages with respect to implementation aspects as all taps are equally large.

In [60, 61], a switched-capacitor SDFIR is reported. The filter taps are selected by windowing an ideal "sinc" impulse response with a Kaiser window function. The filter coefficients have been quantized in two steps, first scaled with a gain of 64 and then a bivariate search was performed around the quantized coefficients with the aim of maximizing the stop-band attenuation.

In [48], a 45-tap, current-mode semi-digital FIR filter was reported for an IQ-transmitter DAC application. The DAC was implemented using 45 different taps where each coefficient was quantized to a 5-bit accuracy and a total number of 319 current sources was used. Optimizing the FIR filter considering hardware cost (word length and filter order) is also discussed in [12].

Another application where designing an efficient semi-digital FIR filter can be important is in radio-frequency DACs (RFDACs) with embedded semi-digital

FIR filter [3, 10]. An oscillating pulse is provided for each unit element of the DAC. Due to the added complexity, a reduced nominal number of bits in the DAC is desired. In turn, this would call for a word length reduction using a $\Sigma\Delta$ modulator cascaded with an SDFIR. A good filter characteristic achieved by the SDFIR could then relax the requirement on the band-pass reconstruction filter.

One of the challenges is how to select the filter taps, i.e., not only the filter order, but also the coefficient values. The most straight-forward approach is to use conventional methods for digital FIR filter design [62, 63] and apply it to the semi-digital FIR filter. This method has however some disadvantages. First of all, in this way the $\Sigma\Delta$ modulator transfer function is not taken into account for designing the SDFIR filter, hence it is most likely an over-design. Secondly, the SDFIR integer coefficients are achieved by rounding the floating-point FIR filter coefficients and therefore, with the rounding error, one must over-design the filter to meet the requirements [20]. The effect of filter coefficients quantization is analyzed in [64, 65] and it is shown that the quantization error limits the attenuation level in the stop-band.

In this paper, we formulate the optimization problem such that it considers the transfer characteristics throughout the transmit chain and includes the $\Sigma\Delta$ modulator and the DAC pulse-amplitude modulation. Moreover, the analog implementation parameters is also included in the optimization procedure. Through the optimization we can minimize the impact of typical analog imperfections (mismatch, noise, etc.) on the output signal. To systematically tackle the problem, we define different set of parameters and metrics to be used in optimization problem of the semi-digital FIR filter; the magnitude metrics, the energy metrics and the analog metrics (or hardware cost). In the optimization problem, each of these metrics can be selected as objective function or constraint.

4.2 Oversampling DAC

We often understand oversampling DACs (OSDACs) as DACs running at a higher sample frequency than the required Nyquist frequency. The ratio between the sample frequency (f_s), and the signal bandwidth (f_b), is normally identified as the oversampling ratio $\mathrm{OSR} = f_s/2f_b$. In a Nyquist-rate converter, the oversampling ratio is unity, i.e., $\mathrm{OSR} = 1$.

4.3 $\Sigma\Delta$ Modulator

The digital $\Sigma\Delta$ modulator has been commonly used in audio systems. In applications with much wider signal bands, such as ADSL and Bluetooth, there are implementations suggested [19, 20, 50, 57, 66]. For a given modulator order (L), and assuming a modulator that shapes noise to higher frequencies, i.e., a

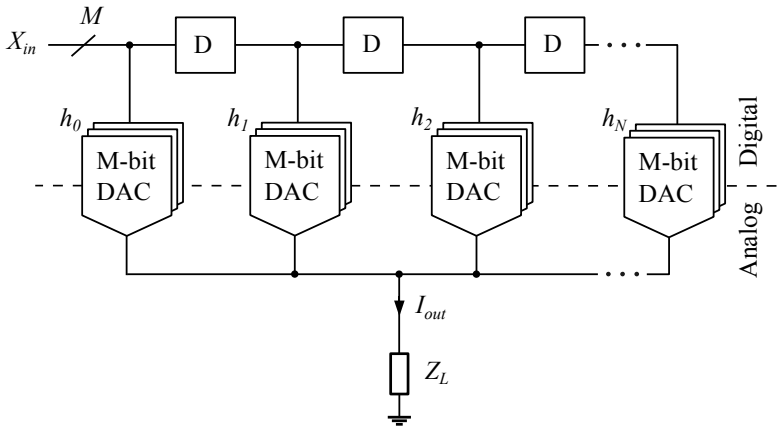

Figure 4.2: Multi-bit semi-digital FIR filter architecture.

low-pass modulator, the NTF is in the discrete-time frequency domain given by $\mathrm{NTF}(z) = \left(1 - z^{-1}\right)^L$. It can be shown, [20], that the in-band signal-to-noise ratio (SNR), or signal-to-quantization noise ratio (SQNR) is approximately

$$\begin{aligned} \mathrm{SQNR} &\approx 6.02M + 1.76 + (20L + 10)\log_{10}(\mathrm{OSR}) \\ &- 10\log_{10}\frac{\pi^{2L+1}}{2L+1}, \end{aligned} \tag{4.1}$$

where M is the number of output bits of the $\Sigma\Delta$ modulator. The equation holds when we can guarantee all poles of the modulator to be placed in zero. Another observation is that the achievable in-band SQNR cannot exceed the one provided at the input of the interpolation (given by N bits), which means that $\mathrm{SQNR} \leq 6.02N + 1.76$. If we consider the power spectral density of the shaped noise at higher frequencies, we find that the noise level can be determined as function of M, OSR, and L (and N, ultimately). This would then define the attenuation requirements of the filter.

4.4 Semi-Digital FIR Filter

The digital $\Sigma\Delta$ modulator introduces quantization noise with comparatively high power and it must be filtered out to avoid, e.g., leaking into other bands. This can either be done with the analog reconstruction filter or with a semi-digital FIR filter (practically both). Semi-digital FIR filters are a class of filters that can be used in the context of digital-to-analog conversion [49]. In the general case, we can have a multi-bit, semi-digital FIR filter where each tap of the filter is realized with a sub-DAC of say M bits. The delay elements are realized with $M-$bit shift registers. As illustrated by the current-steering example in

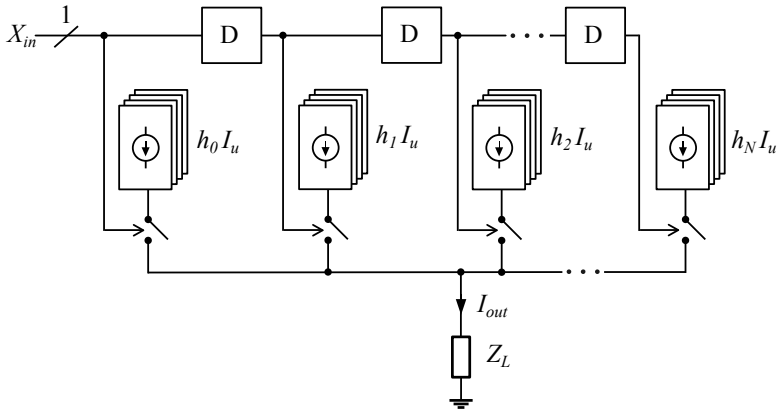

Figure 4.3: Single-bit semi-digital FIR filter architecture.

Fig. 4.2, the input data travels through the shift register and then goes to the M-bit sub-DACs, each weighted and scaled according to the corresponding SDFIR filter coefficient. The output current of each sub-DAC is steered to the output and terminated by the load impedance effectively generating an output voltage. If the output of the modulator is given by a single bit, the semi-digital FIR filter taps are simply controlled by a single switch assuming a current-steering architecture DAC [20, 48–50, 67–72]. One of the major advantages is that the static linearity of the DAC is optimum. Since there are only two output levels available in the DAC, the static transfer function, regardless of mismatch errors, is always given by a straight line. In another type of application, SDFIRs are employed in feedback path of high speed $\Sigma\Delta$ ADCs [73, 74].

Figure 4.3 shows a single-bit semi-digital FIR filter where the input is the bit stream from the modulator. Each sub-DAC in this case is implemented using an integer number (filter coefficient) of unit current sources. FIR filters are causal, linear and time-invariant systems that can be uniquely described by their impulse response. The transfer function of a semi-digital FIR filter is therefore given by

$$H(z) = \frac{Y(z)}{X(z)} = \sum_{n=0}^{N} h_n z^{-n}, \tag{4.2}$$

where $X(z)$ is the input in the $z-$domain, h_n denotes the filter coefficients, and the output $Y(z)$, would be directly proportional to the output current. In time domain, $y(nT) = I_{\text{out}}(nT)/I_u$, where I_u is the nominal current of a single unit current source. In differential mode current-steering DAC, negative coefficients can be implemented by swapping the switches directing the current from the taps to the output.

A conventional approach of SDFIR design to fulfill a specific requirement, is to use conventional FIR design algorithms to find the coefficients and then scale

and truncate them to obtain a set of integer numbers. Typically, this must be a higher than necessary filter order such that, after truncation, the filter response still fulfills the requirement [20], due to the error introduced by the effects of coefficient inaccuracy in FIR filters [75].

Instead, the semi-digital FIR filter can be designed with integer variables as FIR coefficients, which will be discussed in details.

4.5 Analog Reconstruction Filter

In non-ideally reconstructed systems, replicas of the signal spectrum is repeated at integer multiples of the sampling frequency. In DAC, due to pulse-amplitude modulation, the replicas at integer multiples of sample frequency are typically attenuated to some extent by the sinc function which has its zeros at integer multiples of the sample frequency. However, that much of attenuation is usually not enough and there is a need for an analog reconstruction filter after the DAC to remove the remainder of the signal aliases [20]. This holds for a semi-digital FIR filter too, since pulse-amplitude modulation is used and thus aliases exist. However, the analog filter requirement is relaxed considering that interpolation in the $\Sigma\Delta$ and the SDFIR filter is used and the transition band of the filter is increased due to up-sampling the signal.

4.6 VDSL2 Technology

Digital-to-analog converter (DAC) are used in analog front end of different telecommunication standards. In wired communication such as Digital Subscriber Line technologies (xDSL), high performance DAC and analog reconstruction filter are employed to fulfill the specification. Very high bit-rate digital subscriber line (VDSL) technology provides higher data transmission. The second generation system VDSL2, can provide data rate up to 100 Mbit/s using frequency bandwidth up to 30 MHz according to International Telecommunication Union (ITU) [55]. This technology is designed to allow delivery of triple play services over copper infrastructure. However, high bandwidth puts stringent requirement on the DAC linearity and signal-to-noise ratio (SNR) and also on the analog reconstruction filter. Typically a 14 bit DAC together with scrambling technique is used to achieve required SNR and linearity. The reconstruction analog filters of third or fourth order are used to fulfill the power spectral density (PSD) mask [76, 76–81].

Oversampled DAC and digital $\Sigma\Delta$ modulator are used to enhance the performance of the digital-to-analog conversion such as SNR and linearity and in the same time decrease the DAC complexity in terms of the number of bits. This means that the DAC can have the same resolution with fewer number of bits [29, 30].

The semi-digital finite impulse response (SDFIR) filter can be used to comply

with filtering requirement while the requirement on the analog filters is relaxed to a large extend [20, 47, 48, 60, 82]. This will be specially interesting when the output quantizer of the $\Sigma\Delta$ modulator is only one bit, which will result in one-bit DAC for each tap to implement. This will give us the inherently linear response for the digital-to-analog converter, a big credit for one-bit semi-digital FIR filter.

In Paper E of this thesis, we utilize integer optimization techniques to select the SDFIR taps in such a way that the PSD mask for the VDSL2 is fulfilled while minimizing the analog cost of the filter [83]. The technique used in this paper can be applied to any semi-digital FIR filters in different application such as in [3, 11].

Chapter 5

Conclusions and Future Work

5.1 Conclusions

Radio frequency digital-to-analog converters has been shown in recent years to be a promising technique with respect to the high speed and high resolution digital-to-analog conversion. In RFDAC technique the analog complexity moves to the digital domain, hence, higher level of integration is possible with the digital circuitry. Besides, the transceiver design benefits from the CMOS technology scaling. The discrete-time low-resolution technique proposed for the oscillatory pulse amplitude waveform results in the same performance as previously reported designs but with more digital circuits and hence rooms for improvements in lower cost and more integration.

Moreover, an optimization method for semi-digital FIR filter including the $\Sigma\Delta$ modulator response is presented and has shown to be promising in terms of hardware reduction of the conventional semi-digital FIR filters. The number of unit elements of the SDFIR is typically the limiting factor in this architectures, preventing the SDFIR filter solutions to be used widely in different applications. The optimization technique proposed here shows that we can reduce the complexity of the SDFIR filter in terms of total number of unit elements required to obtain enough attenuation by the filter, make it suitable to be used in different applications. The optimization method can save about 38% of the total number of unit elements with variable passband gain method, as presented in Paper E.

5.2 Future Work

The following ideas are identified as possibilities for future work:

- The implementation of the direct-digital-to-RF modulator employing the RFDAC technique discussed in this thesis, in silicon and demonstrating the feasibility of the physical implementation of the solution.

- Utilizing the direct digital synthesis to generate the oscillatory signals required for the RFDAC. In this way there is possibility to co-optimize the direct digital synthesizer and the RFDAC or semi-digital FIR filter.
- Optimizing the semi-digital FIR filter with respect to analog metrics in general case. Such that we also include the energy optimization metrics into account. Then three different metrics, magnitude metrics, energy metrics and analog metrics can be utilized in the optimization problem formulation depending on the application and the requirements.
- Physical implementation of the semi-digital FIR filter employed in the direct-digital-to-RF modulator utilizing the direct digital synthesis technique.

References

References

[1] S. Luschas, R. Schreier, and H.-S. Lee, "Radio Frequency Digital-to-Analog Converter," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1462–1467, Sept. 2004.

[2] P. Eloranta, P. Seppinen, S. Kallioinen, T. Saarela, and A. Parssinen, "A multimode transmitter in 0.13 um CMOS using direct-digital RF modulator," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2774–2784, Dec. 2007.

[3] S. M. Taleie, T. Copani, B. Bakkaloglu, and S. Kiaei, "A linear $\Sigma\Delta$ digital-IF to RF DAC transimtter with embedded mixer," *IEEE Trans. Microwave Theory Tech.*, vol. 56, no. 5, pp. 1059–1068, May 2008.

[4] M. Park, M. Perrott, and R. Staszewski, "A time-domain resolution improvement of an RF-DAC," vol. 57, no. 7, pp. 517–521, July 2010.

[5] ——, "An amplitude resolution improvement of an RF-DAC employing pulsewidth modulation," vol. 58, no. 11, pp. 2590–2603, Nov. 2011.

[6] V. K. Parikh, "All digital quadrature modulator for wideband wireless transmitters," Ph.D. dissertation, The University of Texas at Dallas, 2008.

[7] V. Parikh, P. Balsara, and O. Eliezer, "All digital-quadrature-modulator based wideband wireless transmitters," vol. 56, no. 11, pp. 2487–2497, Nov. 2009.

[8] G. Engel, S. Kuo, and S. Rose, "A 14b 3/6GHz current-steering RF DAC in 0.18 um CMOS with 66db AClr at 2.9GHz," in *Proc. IEEE Int. Solid-State Circuit Conf.*, Feb. 2012, pp. 458–460.

[9] G. Engel, D. Fague, and A. Toledano, "RF digital-to-analog converters enable direct synthesis of communications signals," *IEEE Commun. Mag.*, vol. 50, no. 10, pp. 108–116, Oct. 2012.

[10] A. Jerng and C. Sodini, "A wideband $\Sigma\Delta$ digital-RF modulator for high data rate transmitters," *IEEE J. Solid-State Circuits*, vol. 42, no. 8, pp. 1710–1722, Aug. 2007.

[11] M. Sadeghifar and J. Wikner, "A digital-RF converter architecture for IQ modulator with discrete-time low resolution quadrature LO," in *Proc. IEEE Int. Conf. Electron. Circuits Syst.*, Dec. 2013.

[12] M. Gustavsson, J. Wikner, and N. N. Tan, *CMOS data converters for communications*. Kluwer academic publishers, 2002.

[13] B. Razavi, *Principles of data conversion system design*. IEEE press New York, 1995, vol. 126.

[14] Q. Gu, *RF system design of transceivers for wireless communications*. Springer, 2005.

[15] G. Manganaro, *Advanced data converters*. Cambridge University Press, 2012.

[16] J. Mitola and G. Q. Maguire Jr, "Cognitive radio: making software radios more personal," *Personal Communications, IEEE*, vol. 6, no. 4, pp. 13–18, 1999.

[17] A. V. Oppenheim, A. S. Willsky, and I. T. Young, *Signals and Systems*. Prentice-Hall, 1983.

[18] I. Akita, T. Itakura, and K. Shiraishi, "Current-steering digital-to-analog converter with a high-PSRR current switch," vol. 58, no. 11, pp. 724–728, 2011.

[19] J. J. Wikner and N. Tan, "Modeling of CMOS digital-to-analog converters for telecommunication," *IEEE Trans. Circuits Syst. II*, vol. 46, no. 5, pp. 489–499, 1999.

[20] J. J. Wikner, "Studies on CMOS Digital-to-Analog Converters," Ph.D. dissertation, Linköping University, Sweden, 2001, Dissertation No: 667.

[21] A. van den Bosch, M. Steyaert, and W. Sansen, "SFDR-bandwidth limitations for high speed high resolution current steering CMOS D/A converters," in *Proc. IEEE Int. Conf. Electron. Circuits Syst.*, vol. 3, 1999, pp. 1193–1196 vol.3.

[22] S. Luschas and H.-S. Lee, "Output impedance requirements for DACs," in *Proc. IEEE Int. Conf. Electron. Circuits Syst.*, Sept. 1999, pp. 1193–6.

[23] A. van den Bosch, M. Borremans, M. Steyaert, and W. Sansen, "A 10-bit 1-GSample/s Nyquist current-steering CMOS D/A converter," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 315–324, Mar. 2001.

[24] N. Tan and J. J. Wikner, "A CMOS digital-to-analog converter chipset for telecommunication," *IEEE Circuits Devices Mag.*, vol. 13, no. 5, pp. 11–16, 1997.

[25] K. O. Andersson, "Modeling and implementation of Current-Steering Digital-to-Analog Converters," Ph.D. dissertation, Linköping University, Sweden, May 2005, Dissertation No: 944.

[26] Y. Zhou and J. Yuan, "An 8-bit 100-Mhz CMOS Linear Interpolation DAC," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1758–1761, Oct. 2003.

[27] ——, "A 10-bit 100-MHz CMOS Linear Interpolation DAC," in *Proc. Europ. Solid-State Circuits Conf.*, May 2002, pp. 471–474.

[28] J. Candy, G. Temes, I. of Electrical, E. Engineers, I. Circuits, and S. Society, *Oversampling Delta-Sigma Data Converters: Theory, Design, and Simulation*, ser. A selected reprint volume. Wiley, 1962.

[29] N. Afzal and J. Wikner, "Power efficient arrangement of oversampling ΣΔ DACs," in *Proc. Norchip*, Nov 2012.

[30] N. Afzal, M. Sadeghifar, and J. Wikner, "A study on power consumption of modified noise-shaper architectures for ΣΔ DACs," in *Proc. Europ. Conf. Circuit Theory Design*, Aug 2011, pp. 274–277.

[31] N. Afzal and J. Wikner, "Study of modified noise-shaper architectures for oversampled ΣΔ DACs," in *Proc. Norchip*, Nov. 2010.

[32] M. Vesterbacka, M. Rudberg, J. J. Wikner, and N. U. Andersson, "Dynamic element matching in D/A converters with restricted scrambling," in *Proc. IEEE Int. Conf. Electron. Circuits Syst.*, 2000, pp. 36–39.

[33] K. O. Andersson, N. U. Andersson, and J. J. Wikner, "A differential DAC architecture with variable common-mode level," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2002, pp. 113–6.

[34] K. Andersson, N. U. Andersson, and J. Wikner, "Spectral shaping of DAC nonlinearity errors through modulation of expected errors," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2001, pp. 417–420.

[35] N. U. Andersson and J. Wikner, "A strategy for implementing dynamic element matching in current-steering DACs," in *Proc. IEEE Southwest Symp. Mixed-Signal Design.*, Feb. 2000, pp. 51–6.

[36] J. Pham and A. Carusone, "A time-interleaved ΔΣ-DAC architecture clocked at the nyquist rate," *IEEE Trans. Circuits Syst. II - Express Briefs*, vol. 55, no. 9, pp. 858–862, 2008.

[37] S. Noli, A. P. Perez, E. Bonizzoni, and F. Maloberti, "ΔΣ time interleaved current steering DAC with dynamic elements matching," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2009, pp. 407–10.

[38] S. Balasubramanian, G. Creech, J. Wilson, S. M. Yoder, J. J. McCue, M. Verhelst, and W. Khalil, "Systematic analysis of interleaved digital-to-analog converters," vol. 58, no. 12, pp. 882–886, 2011.

[39] M. Sadeghifar and J. Wikner, "Modeling and analysis of aliasing image spurs problem in digital-RF-converter-based IQ modulators," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2013, pp. 578–581.

[40] ——, "A higher Nyquist-range DAC employing sinusoidal interpolation," in *Proc. Norchip*, Nov. 2010, pp. 1–4.

[41] J. Vankka, J. Ketola, J. Sommarek, O. Vaananen, M. Kosunen, and K. Halonen, "A GSM/EDGE/WCDMA modulator with on-chip D/A converter for base stations," *IEEE Trans. Circuits Syst. II*, vol. 49, no. 10, pp. 645–655, Oct. 2002.

[42] J. Vankka, J. Sommarek, J. Ketola, I. Teikari, and K. Halonen, "A digital quadrature modulator with on-chip D/A converter," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1635–1642, Oct. 2003.

[43] J. Sommarek, J. Vankka, J. Ketola, J. Lindeberg, and K. Halonen, "A digital modulator with bandpass delta-sigma modulator," in *Proc. Europ. Solid-State Circuits Conf.*, Sept. 2004, pp. 159–162.

[44] J. Sommarek, J. Vankka, J. Ketola, I. Teikari, and K. Halonen, "A digital quadrature modulator with on-chip D/A converter," in *Proc. Europ. Solid-State Circuits Conf.*, Sept. 2003, pp. 85–88.

[45] A. Majid and A. W. Malik, "Design and implementation of a direct digital frequency synthesizer using sum of weighted bit products," Master's thesis, Linköping University, Sweden, 2009.

[46] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*. Wiley-IEEE Press, 2004.

[47] D. Su and B. Wooley, "A CMOS oversampling D/A converter with a current-mode semidigital reconstruction filter," *IEEE J. Solid-State Circuits*, vol. 28, no. 12, pp. 1224–1233, Dec. 1993.

[48] A. Lin, D. Su, R. Hester, and B. Wooley, "A CMOS oversampled DAC with multi-bit semi-digital filtering and boosted subcarrier SNR for ADSL central office modems," *IEEE J. Solid-State Circuits*, vol. 41, no. 4, pp. 868–875, Apr. 2006.

[49] D. Su and B. Wooley, "A CMOS oversampling D/A converter with a current-mode semi-digital reconstruction filter," in *Proc. IEEE Int. Solid-State Circuit Conf.*, Feb. 1993, pp. 230–231.

[50] D. Barkin, A. Lin, D. Su, and B. Wooley, "A CMOS oversampling bandpass cascaded D/A converter with digital FIR and current-mode semi-digital filtering," *IEEE J. Solid-State Circuits*, vol. 39, no. 4, pp. 585–593, 2004.

[51] P. Eloranta and P. Seppinen, "Direct-digital RF modulator IC in 0.13μm CMOS for wide-band multi-radio applications," in *Proc. IEEE Int. Solid-State Circuit Conf.*, Feb. 2005, pp. 532–4.

[52] S. R. Norsworthy, R. Schreier, and G. C. Temes, *Delta-Sigma Data Converters: Theory, Design, and Simulation*. IEEE press New York, 1996, vol. 97.

[53] B. Wooley, "Cascaded noise-shaping modulators for oversampled data conversion," in *Proc. IEEE Custom Integrated Circuits Conf.*, Sept. 2003, pp. 113–114.

[54] "UE radio transmission and reception (FDD)," Third-Generation Partnership Project 3GPP, Technical Specification 25.101, Sept. 2012. [Online]. Available: http://www.3gpp.org/ftp/Specs/html-info/25101.htm

[55] "Very high speed digital subscriber line transceivers 2 (VDSL2)," International Telecommunication Union (ITU-T), Technical Specification G.993.2, Dec. 2011. [Online]. Available: http://www.itu.int/rec/T-REC-G.993.2-201112-I/en

[56] C. Eder, G. Fischerauer, P. Hagn, and G. Riha, "SAW filters for 3G systems: a quantum leap in size and passive integration is ahead," in *2001 IEEE Ultrasonics Symposium. Proceedings*, 2001.

[57] X. Wang and R. Spencer, "A low-power 170-MHz discrete-time analog FIR filter," *IEEE J. Solid-State Circuits*, vol. 33, no. 3, pp. 417 –426, March 1998.

[58] P. Hurst and J. Brown, "Finite impulse response switched-capacitor filters for the delta-sigma modulator D/A interface," *IEEE Trans. Circuits Syst.*, vol. 38, no. 11, pp. 1391–1397, Nov. 1991.

[59] T. S. Doorn, E. Tuijl, D. Schinkel, A.-J. Annema, M. Berkhout, and B. Nauta, "An audio FIR-DAC in a BCD process for high power class-D amplifiers," in *Proc. Europ. Solid-State Circuits Conf.*, 2005.

[60] P. Francese, P. Ferrat, and Q. Huang, "A 13-b 1.1-MHz oversampled DAC with semidigital reconstruction filtering," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2098–2106, Dec. 2004.

[61] ——, "A 13b 1.1 MHz oversampled DAC with semidigital reconstruction filtering," in *Proc. IEEE Int. Solid-State Circuit Conf.*, Feb. 2004, pp. 370–533 Vol.1.

[62] L. Rabiner, "Linear program design of finite impulse response (FIR) digital filters," *IEEE Trans. Audio Electroacoust.*, vol. 20, no. 4, pp. 280–288, 1972.

[63] Y. C. Lim, S. Parker, and A. Constantinides, "Finite word length FIR filter design using integer programming over a discrete coefficient space," *IEEE Trans. Acoust., Speech, Signal Processing*, vol. 30, no. 4, pp. 661–664, 1982.

[64] D. Chan and L. Rabiner, "Analysis of quantization errors in the direct form for finite impulse response digital filters," *IEEE Trans. Audio Electroacoust.*, vol. 21, no. 4, pp. 354–366, 1973.

[65] B. Liu, "Effect of finite word length on the accuracy of digital filters–a review," *Circuit Theory, IEEE Transactions on*, vol. 18, no. 6, pp. 670–677, 1971.

[66] J. Wikner, Y. Gao, and N. Tan, "D/A conversion interface for DMT-ADSL applications," *IEEE Circuits Devices Mag.*, vol. 14, no. 6, pp. 7–13, 1998.

[67] V. Srinivasan, G. Rosen, and P. Hasler, "Low-power realization of FIR filters using current-mode analog design techniques," in *Proc. Asilomar Conf. Signals Syst. Comput.*, vol. 2, Nov. 2004, pp. 2223–2227 Vol.2.

[68] M. A. T. Sanduleanu, A. J. M. Van Tuijl, R. Wassenaar, and H. Wallinga, "A 16-bit D/A interface with sinc approximated semidigital reconstruction filter and reduced number of coefficients," in *Proc. Europ. Solid-State Circuits Conf.*, 1998, pp. 180–183.

[69] H. Qiuting and G. Moschytz, "Analog FIR filters with an oversampled ΣΔ modulator," *IEEE Trans. Circuits Syst. II - Express Briefs*, vol. 39, no. 9, pp. 658–663, Sept. 1992.

[70] J.-W. Kim, B.-M. Min, J.-S. Yoo, and S.-W. Kim, "An area-efficient sigma-delta DAC with a current-mode semi-digital iFIR reconstruction filter," in *Proc. IEEE Int. Symp. Circuits Syst.*, vol. 1, May 1998, pp. 344–347 vol.1.

[71] Q. Huang, "Mixed analog/digital, FIR/IIR realization of a linear-phase lowpass filter," *IEEE J. Solid-State Circuits*, vol. 31, no. 9, pp. 1347–50, 1996.

[72] A. Flament, A. Frappe, A. Kaiser, B. Stefanelli, A. Cathelin, and H. Ezzeddine, "A 1.2 GHz semi-digital reconfigurable FIR bandpass filter with passive power combiner," in *Proc. Europ. Solid-State Circuits Conf.*, 2008, pp. 418–421.

[73] H. Pakniat and M. Yavari, "A ΣΔ FIR-DAC for Multi-bit ΣΔ Modulators," *IEEE Trans. Circuits Syst. I*, vol. 60, no. 9, pp. 2321–2332, 2013.

[74] O. Oliaei, "Continuous-time sigma-delta modulator incorporating semi-digital FIR filters," in *Proc. IEEE Int. Symp. Circuits Syst.*, vol. 1, 2003.

[75] A. Petraglia and S. Mitra, "Effects of coefficient inaccuracy in switched-capacitor transversal filters," *IEEE Trans. Circuits Syst.*, vol. 38, no. 9, pp. 977–983, Sept. 1991.

[76] H. Weinberger, A. Wiesbauer, C. Fleischhacker, and J. Hauptmann, "A 800 mW, full-rate ADSL-RT analog frontend IC with integrated line driver," in *Proc. IEEE Int. Solid-State Circuit Conf.*, 2001, pp. 115–118.

[77] G. Cesura, A. Bosi, F. Rezzi, R. Castello, J. Chan, S. Wong, C. F. Yung, O. Carnu, and T. Cho, "A VDSL2 CPE AFE in 0.15 um CMOS with integrated line driver," in *Proc. IEEE Int. Solid-State Circuit Conf.*, 2009, pp. 108–109,109a.

[78] S. Oswal, F. Mujica, S. Prasad, R. Srinivasa, B. Sharma, A. Raychoudhary, H. Khasnis, A. Sharma, R. Sriram, B. Vijayvardhan, R. Menon, R. Gireesh, N. Ahuja, M. Gambhir, and M. Sadafale, "A 0.13 um CMOS four-channel ADSL2+ analog front-end for CO applications with 75mW per channel," in *Proc. IEEE Int. Solid-State Circuit Conf.*, 2004, pp. 404–535 Vol.1.

[79] H. Khasnis, R. Mundhada, N. Saxena, R. Srinivasa, S. Cholkar, S. Prasad, R. Jonnavithula, V. Baireddy, M. Sadafale, R. Hariharan, J. Tangudu, P. Indu, V. Mishra, M. Ali, M. Locke, K. Kratochwil, and G. Somayaji, "An adsl2 and vdsl2 cpe system-on-chip with integrated voice over ip capabilities for residential gateway applications," in *Signals, Systems and Electronics, 2007. ISSSE '07. International Symposium on*, 2007, pp. 235–237.

[80] R. Hogervorst, B. Tourette, N. Monier, O. Metayer, E. Afifi, J.-C. Delefosse, and J.-Y. Michel, "A 3 V CMOS quad-spectrum ADSL CPE analog front-end with 5 V integrated line driver," in *Proc. IEEE Int. Solid-State Circuit Conf.*, 2004, pp. 406–535 Vol.1.

[81] B. Schafferer and R. Adams, "A 3v CMOS 400mW 14b 1.4GS/s DAC for multi-carrier applications," in *Proc. IEEE Int. Solid-State Circuit Conf.*, Feb. 2004, pp. 69–70.

[82] Y. Gao, J. Wikner, and H. Tenhunen, "Design and analysis of an oversampling D/A converter in DMT-ADSL systems," *Analog Integrated Circuits Signal Process.*, vol. 32, no. 3, pp. 201–210, 2002.

[83] M. Sadeghifar, J. Wikner, and O. Gustafsson, "Linear programming design of semi-digital FIR filter and $\Sigma\Delta$ modulator for VDSL2 transmitter," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2014.

Part II

Publications

Publications

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