On-Line Dead-Time Compensation Technique for Open-Loop PWM-VSI Drives

Alfredo R. Muñoz, Member, IEEE, and Thomas A. Lipo, Fellow, IEEE

Abstract—A new on-line dead-time compensation technique for low-cost open-loop pulsewidth modulation voltage-source inverter (PWM-VSI) drives is presented. Because of the growing numbers of open-loop drives operating in the low-speed region, the synthesis of accurate output voltages has become an important issue where low-cost implementation plays an important role. The so-called average dead-time compensation techniques rely on two basic parameters to compensate for this effect: the magnitude of the volt seconds lost during each PWM cycle and the direction of the current. In a low-cost implementation, it is impractical to attempt an on-line measurement of the volt-seconds error introduced in each cycle-instead an off-line measurement is favored. On the other hand, the detection of the current direction must be done on line. This becomes increasingly difficult at lower frequencies and around the zero crossings, leading to erroneous compensation and voltage distortion. This paper presents a simple and cost-effective solution to this problem by using an instantaneous back calculation of the phase angle of the current. Given the closed-loop characteristic of the back calculation, the zero crossing of the current is accurately obtained, thus allowing for a better dead-time compensation. Experimental results validating the proposed method are presented.

Index Terms—AC drives, blanking time, current measurement, induction motors, volt-second compensation, volts per hertz.

I. INTRODUCTION

NE OF THE main problems encountered in open-loop pulsewidth modulation voltage-source inverter (PWM-VSI) drives is the nonlinear voltage gain caused by the nonideal characteristics of the power inverter. The most important nonlinearity is introduced by the necessary blanking time to avoid the so-called shootthrough of the dc link. To guarantee that both switches in an inverter leg never conduct simultaneously a small time delay is added to the gate signal of the turning-on device. This delay, added to the device's finite turn-on and turn-off times, introduces a load dependent magnitude and phase error in the output voltage [1]–[4]. Since the delay occurs in every PWM carrier cycle the magnitude of the error grows in inverse proportion to the output fundamental frequency, introducing a serious waveform distortion and fundamental voltage drop [7], [14]. The voltage distortion increases with switching frequency introducing harmonic components that, if not compensated, may cause instabilities as well as additional losses in the machine being driven [6], [8], [9]. Another source of output voltage distortion is the finite voltage drop across the switches during the on state [2], [5].

Manuscript received February 3, 1998; revised September 14, 1998. Recommended by Associate Editor, O. Ojo.

The authors are with the Department of Electrical and Computer Engineering, University of Wisconsin, Madison, WI 53706-1691 USA.

Publisher Item Identifier S 0885-8993(99)05562-3.

The dead-time problem has already been investigated by the industry [8], [9], and various solutions have been tried [2], [4]–[5], [7]–[10]. In most cases, the compensation techniques are based on an average value theory, the lost volt seconds are averaged over an entire cycle and added vectorially to the commanded voltage. More recently, a pulse based compensation method has been proposed by Leggate *et al.* [8], where the compensation is realized for each PWM pulse. This yields a more accurate compensation, but since it requires double sampling per carrier period, it increases the overhead on the processor.

Regardless of the method used, all dead-time compensation techniques are based on the polarity of the current, hence, current detection becomes an important issue. This is particularly true around the zero crossings where an accurate current measurement is needed to correctly compensate for the dead time [2], [8]. According to the average value theory, to compensate for the dead-time, the reference voltage is changed by adding or subtracting the required instantaneous average volt seconds. Although in principle this is simple, the dead time also depends on the magnitude and phase of the current as well as the type of switch used. Several authors have dealt with this problem by using startup measurement and calibration procedures. However, this type of compensation becomes mistuned as the operating conditions change due to loading and temperature.

In this paper, a new low-cost on-line dead-time compensation technique based on a back calculation of the current phase angle is presented. The method can be easily implemented as part of open-loop PWM-VSI drives requiring no additional hardware and only a few extra lines of software code. The proposed technique has been tested in the lab as part of a constant V/f motor drive giving excellent results. The implementation of the proposed compensation technique requires only one current sensor and a low-sampling frequency, making it very attractive for low-cost applications.

II. VOLT-SECOND COMPENSATION

In general the term "dead-time compensation," while widely used, often misleads since the actual dead time, which is intentionally introduced to avoid the so-called shootthrough, is only one of the elements accounting for the error in the output voltage. For this reason, it is referred to here as volt-second compensation. The volt-second compensation algorithm developed herein is based on the well known instantaneous average voltage method. Although this technique is not the most accurate method available, it is simple to understand and gives good results for steady-state operation. The basic principle is to compensate for the average loss or gain of voltage per carrier period. To understand the principle of operation it suffices to look at the voltages in one of the inverter legs over one carrier period. Fig. 1 shows idealized waveforms of the PWM carrier signal and reference voltages. It also shows idealized gate signals, V_{g+} and V_{g-} , ideal output voltage V_{AN}^* , actual pole voltage V_{AN} without dead-time compensation, and actual pole voltage compensated for dead time V_{ANc} for positive current. It is assumed that the switch exhibits finite turn-on and turn-off delay times t_{on} and t_{off} , respectively, and the blanking time is t_d . It is not difficult to show that for positive current the actual average pole voltage over one PWM carrier period, as a function of the commanded voltage V^* , is

$$\overline{V}_{AN} \approx V_{\rm dc} \left[\frac{1}{2} + \frac{V^*}{V_{\rm dc}} \right] - \Delta V \tag{1-a}$$

and for negative current is

$$\overline{V}_{AN} \approx V_{\rm dc} \left[\frac{1}{2} + \frac{V^*}{V_{\rm dc}} \right] + \Delta V \tag{1-b}$$

where ΔV represents the error due to the nonideal switching. The voltage error ΔV is found by computing the actual average voltage and subtracting off the ideal output voltage V_{AN}^* . Its value is easily found by calculating the area under the curve V_{AN} over one carrier period, and this yields

$$\Delta V = \frac{t_d + t_{\rm on} + t_{\rm off}}{T_c} \left[V_{\rm dc} - V_{\rm sat} + V_d \right] + \frac{V_{\rm sat} - V_d}{V_{\rm dc}} V^* + \frac{V_{\rm sat} + V_d}{2}$$
(2)

where V_{sat} is the on-state voltage drop across the switch and V_d is the forward voltage drop of the diode. V_{dc} is the dc-link voltage and T_c is the PWM carrier period. The first term in (2) is proportional to the switching frequency ($f_c = 1/T_c$) and accounts for most of the voltage error. Since the difference $V_{\text{sat}} - V_d$ is small and V_{dc} is much greater than V^* , the second term in (2) can be neglected, hence, the error can be approximated to

$$\Delta V \approx \frac{t_d + t_{\rm on} - t_{\rm off}}{T_c} \left[V_{\rm dc} - V_{\rm sat} + V_d \right] + \frac{V_{\rm sat} + V_d}{2}.$$
(3)

Although the sum $(V_{\text{sat}} + V_d)$ is relatively small, it still accounts for several volts for insulated gate bipolar transistor (IGBT)-based inverters, and it cannot be neglected.

As shown in Fig. 1, the volt-second error can be interpreted as the difference in areas between the commanded voltage V_{AN}^* and the actual voltage V_{AN} . The (+) and (-) signs in the bottom trace indicate that in part of the cycle there is a gain of instantaneous average voltage and in part of it there is a loss of volt seconds. During the turn-off process, the pole voltage transition is delayed t_{off} seconds, hence increasing the average voltage (shown by the + sign). On the other hand, the turn-on process is first delayed by the blanking time t_d , hence, reducing the average voltage (shown by the first - sign). In addition, because of the turn-on delay the pole

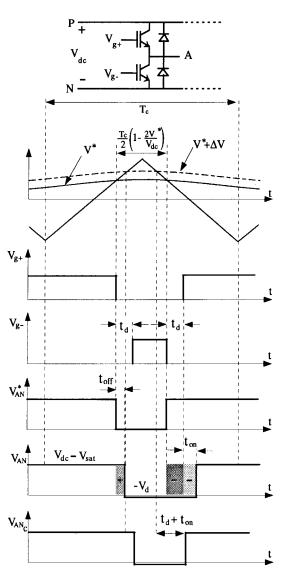


Fig. 1. PWM voltage waveforms for positive current. From the top: reference voltages and carrier signal, gate voltage top device, gate voltage bottom device, commanded pole voltage before compensation, actual pole voltage before compensation, and actual pole voltage after compensation.

voltage does not go high until after $t_{\rm on}$, thus giving rise to an additional reduction in the average voltage (shown by the second - sign). The net effect over one carrier cycle is a loss of average voltage given by ΔV . If a negative current polarity is considered, a similar analysis shows that there is a net gain of average voltage ΔV . In principle, the delay times $t_{\rm on}$ and $t_{\rm off}$ as well as the on-state voltage across the IGBT and the diode, are constant and independent of the load current. It is well known, however, that these quantities vary with temperature and current level making the voltage error ΔV load dependent. As a first approximation, this dependency can be taken into account by modeling both the diode and the switch as having a constant voltage drop plus a voltage drop proportional to the load current [2], [5]. It is also possible to use more accurate models to describe the switch (including the variation of the turn on and turn off delays), but this makes the system very expensive and unsuitable for low-cost constant V/f drives.

Experimental data illustrating the relative importance of the magnitude ΔV and its dependence on the load current is

TABLE I VOLTAGE ERROR DUE TO NONIDEAL SWITCHING

Current (A) (rms)	$V_{AN}(V)$ (rms)	ΔV (V) (rms)
0	25.0	0
0.5	10.7	14.3
1.16	10.4	14.6
1.87	10.0	15.0
2.30	9.7	15.3
9.40	9.1	15.9

presented in Table I. In all cases, the commanded voltage is set to 25 V and the switching frequency is fixed at 8 kHz. The switch is a standard 50-A IGBT module and the blanking time t_d was set to 2.5 μ s. The forward voltage drop across the diode varied between 0.73–0.97 V for currents between 0.5–3 A. Table I shows that, in this particular case, the deadtime effect (including the turn-on and turn-off delays) accounts for about 14.3 V with an additional variation of about 1.6 V for currents between 0 and 9.4 A. Here, it is important to point out that the amount of volt seconds lost (gained) per fundamental cycle does not depend on the magnitude of the commanded voltage. Hence, its impact will be much more severe for lowoutput fundamental voltages, as is the case in constant volts per hertz drives operating at low speeds [12].

Average compensation algorithms are based on commanding a voltage modified by ΔV such that, after passing through the inverter, the instantaneous average output voltage is equal to the ideal commanded voltage V^* . This is accomplished by modifying the actual commanded voltage to be $V^* + \Delta V$ when the current is positive and $V^* - \Delta V$ when the current is negative. The implementation of the method requires a good estimate of the required correction voltage ΔV as well as an accurate knowledge of the polarity of the current [1].

A. Magnitude Correction

The magnitude of ΔV , as given in (3), involves several terms that depend on the device used and the load current. In general, it is very expensive and not practical to measure each one of the terms in (3). Instead, they are normally obtained through off-line experimental measurements [5]. The main difficulty is changes in device's on-state voltages with load current and frequency [13]. An exact compensation would require either a precise model of each switch or direct voltage measurements. Since both techniques are expensive a much simpler approach is used. The method consists in using (3) to compute ΔV for nominal values (this will be referred to as ΔV_o) and then apply a small correction factor ΔV_c for different load currents. The final magnitude of the compensation used in the algorithm is $\Delta V = (\Delta V_o + \Delta V_c)$, which is schematically shown in Fig. 4.

The correction factor ΔV_c is stored in a table that uses the current magnitude as input yielding ΔV_c at the output. The table can be built using actual experimental data, based on manufacturer specifications or using a mathematical model for the switch and diode. The complete table is built in RAM as a lookup table. An alternate method to the lookup table is to use an approximate model of the diode and IGBT to describe the

voltage drop as a function of the load current. The tradeoff is an increased amount of code versus a lookup table. In addition, a lookup table can be easily modified to account for changes in devices. The detection of the current direction on the other hand, must be done on line. The main problem in this case occurs around the zero crossings where it is very difficult to achieve a reliable measurement due to the PWM noise and the clamping of the current [9], [15].

B. Current Polarity Determination

As mentioned in the Introduction, average dead-time compensation techniques rely on direct current measurements to determine the sign of the compensation needed. Because of PWM noise and current clamping around the zero crossing, accurate measurement of the current polarity is very challenging [9], [15]. In the past, several solutions have been proposed, however, they require either a high-bandwidth current sensor [2], [11] or are computation intensive making them not suitable for low-cost applications [7]–[9].

The main objective here is to be able to obtain reliable current polarity information using a low-cost implementation. In general, only the polarity of the current is needed for compensation, however because of the change in the switching times with load changes, the magnitude of the current is also required. To overcome this difficulty a transformation similar to a d-q synchronous frame transformation is used. Assuming a sinusoidal current in phase a and multiplying it by $\cos \omega t$ and $\sin \omega t$ yields

$$i_q = I_{\rm pk} \cos(\omega t - \phi) \cos(\omega t)$$
$$= \frac{I_{\rm pk}}{2} \left[\cos(2\omega t - \phi) + \cos(\phi) \right] \tag{4}$$

and

$$i_{d} = I_{\rm pk} \cos(\omega t - \phi) \sin(\omega t)$$
$$= \frac{I_{\rm pk}}{2} \left[\sin(2\omega t - \phi) + \sin(\phi) \right]$$
(5)

where $I_{\rm pk}$ is the peak value of the phase-a current and ϕ is the phase angle with respect to the voltage. Notice that the time functions $\cos \omega t$ and $\sin \omega t$ are required to generate the commanded voltages in a constant V/f implementation [12], therefore, its use in (4) and (5) does not represent an extra cost.

The d- and q-axis current components contain, ideally, both a double-frequency term and the wanted dc component. To eliminate the double-frequency term, a notch-type filter, tuned at twice the excitation frequency, is used. This filter corresponds to a second-order Butterworth design whose implementation requires only four additions and five multiplications. The tuning is accomplished by simply modifying the coefficients of the equation describing the filter. The generation of new coefficients for different tuning frequencies requires two additional multiplications. It is important to point out that if two of the phase currents are available for measurement purposes a standard dq transformation can be used. In this case, (4) and (5) would be substituted by

$$\begin{aligned} I_q &= i_a \cos \omega t - \frac{1}{\sqrt{3}} \left(i_a + 2i_c \right) \sin \omega t \\ &= I_{\rm pk} \cos(\phi) \end{aligned} \tag{6}$$

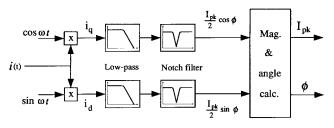


Fig. 2. Current measurement and decomposition into magnitude and phase angle.

and

$$i_q = i_a \sin \omega t + \frac{1}{\sqrt{3}} (i_a + 2i_c) \cos \omega t$$
$$= I_{\rm pk} \sin(\phi) \tag{7}$$

where i_a and i_c are the instantaneous currents in phase a and c, respectively. Since the double frequency is eliminated by the transformation itself the notch filter is no longer needed. This implementation however, requires two current sensors instead of only one as proposed here, making it a more expensive solution [15].

To eliminate the high-frequency components, a low-pass filter is added. The low-pass filter is easily designed since it is only required to eliminate the high-frequency contents introduced by the PWM frequency. In principle, its bandwidth would be limited only by the PWM frequency, however, to avoid fast changes in the angle measurement a cutoff frequency of twice the excitation frequency is used. The filter is implemented using a first-order transfer function requiring only two multiplications and one addition. Although the use of filters represents some extra overhead for the processor, the method is much less computational intensive, requires less memory and virtually no data bookkeeping than using other techniques such as fast Fourier transform (FFT) or time domain analysis. The time delay and phase shift introduced by the filters is very small, less than 1° at 1 Hz and 5° at 60 Hz. Since the dead-time compensation is not critical at higher frequencies (i.e., larger output voltages), the larger phase error at 60 Hz does not represent a problem.

After eliminating the ac components from (4) and (5) a simple trigonometric relation yields both the magnitude and the phase angle of the current. Once the phase angle is known, the instant of zero crossing can be determined simply by counting from the instant of the zero crossing of the reference voltage. Given the very small delay between the commanded voltage and the inverter output, it is possible to use the commanded voltage, rather than the actual voltage, as the reference for the phase angle measurement. A block diagram of the magnitude and phase angle measurements is shown in Fig. 2. Experimental results for a fundamental frequency of 3 Hz are presented in Fig. 3. In this figure, it is shown that even during the startup transient the algorithm converges to the correct phase angle within one cycle. Using a tighter notch filter increases the speed of response but this also increases the complexity of the filter design. In any case, a response within one cycle is considered acceptable for open-loop constant V/f drives.

Once the magnitude and phase angle of the measured current are determined by this means, an ideal current waveform is

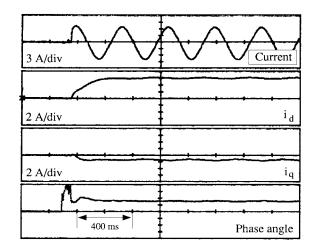


Fig. 3. Current magnitude and phase angle measurement. From top to bottom: measured current, d-axis component, q-axis component, and phase angle.

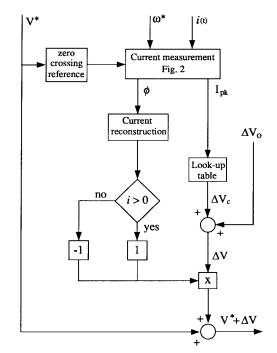


Fig. 4. Block diagram of the proposed dead-time compensation algorithm.

reconstructed. The reconstructed current is then used in the dead-time compensation algorithm, which proceeds as follows: if the reconstructed current is positive the magnitude ΔV [computed from (3) and corrected by ΔV_c] is added to the commanded voltage. Conversely, if the current is negative ΔV is subtracted from the commanded voltage. A block diagram showing the implementation is presented in Fig. 4. Since the reconstructed current is free from PWM noise the instant of zero crossing is easily determined.

III. INFLUENCE OF VOLTAGE ACCURACY ON V/f DRIVES

The importance of a correct synthesis of the output voltage in V/f drives goes beyond the harmonic distortion introduced by the dead time, but because of the loss of fundamental voltage, also affects the output torque and speed. In the past, Koga *et al.* showed that the dead-time effect results in an equivalent increased stator resistance affecting the stability of constant volts per hertz drives [14]. For this type of drive, it is known that the torque is proportional to the square of the fundamental voltage [12]. Assuming that the output voltage has an error ΔV with respect to the commanded value V^* then

$$T \propto (V^* + \Delta V)^2 \tag{8}$$

which can be approximated to

$$T \approx T_o \left(1 + \frac{2\Delta V}{V^*} \right) \tag{9}$$

where T_o is a proportionality constant given by the torque when there is no voltage error. The error in the torque due to an incorrect fundamental voltage is

$$\Delta T = T - T_o = \frac{2\Delta V}{V^*} T_o. \tag{10}$$

At high speeds, the commanded voltage V^* is large and the ratio $\Delta V/V^*$ becomes negligible, however, at low speeds V^* is small and even small errors in the voltage will yield large torque and speed errors. To better quantify the importance of (10) a set of dynamic simulations was carried out. To simplify the analysis ideal switches were assumed and the blanking time was set to zero. This implies a perfect dead-time compensation. The magnitude of the fundamental voltage was then changed by 1 V and the speed and torque were recorded. Figs. 5 and 6 show the steady-state torque and speed errors for three stator frequencies: 60, 6, and 3 Hz. As expected the errors are negligible for high-output voltages (60 Hz), but they become very large for small-output voltages (3 Hz). Hence, it is evident that to achieve good speed accuracy in a V/f drive it is essential to have an even better accuracy in the synthesized output voltage. For example, for the machine used in the experiment, to obtain a 0.3% speed accuracy it is necessary to synthesize the PWM output voltage to better than 0.4 V, which represents a 0.2% accuracy [12]. Accurate experimental verification of the influence of only the dead-time error on the torque-speed curve of the machine is quite difficult since it is impossible to separate accurately the individual effects that account for torque variations such as voltage and slip. In addition, at low frequencies a small change in the magnitude of the voltage may produce large changes in flux, hence affecting the torque production.

IV. EXPERIMENTAL RESULTS

The proposed compensation method has been implemented as part of a low-cost constant V/f drive using a 3-hp induction motor whose parameters are given in the Appendix. The phase current was measured using an open-loop-type current sensor with asynchronous sampling and the sampling time was set to 1 ms. Table II shows the voltage error after the compensation has been applied. The small error still present is due to inaccuracies in the computation of the magnitude of the correction voltage ΔV . The computation of the magnitude of the commanded voltages shown in this table, as a function of the frequency, goes beyond the scope of this paper and

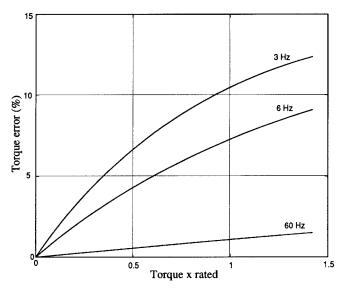


Fig. 5. Torque error due to 1-V peak error in output voltage. Simulation results.

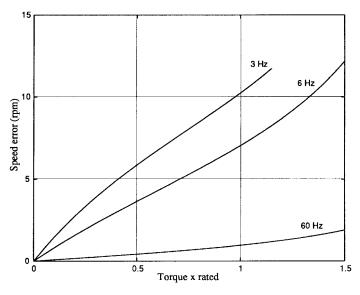


Fig. 6. Speed error due to 1-V peak error in output voltage. Simulation results.

the details can be found in [12]. For the sake of completeness, however, it can be noted that the commanded voltage does not corresponds to just the ratio V/f, but it needs to be boosted at low frequencies to compensate for the stator resistance voltage drop. In addition to this, the frequency also needs to be adjusted to compensate for the increased slip with load. The magnitude of the commanded voltage as a function of the frequency can be computed from

$$V_s = I_s r_s \cos \phi + \sqrt{\left(\frac{V_{so} f_e^*}{f_R}\right) - (I_s r_s \sin \phi)^2} \qquad (11)$$

where the notation corresponds to that used in [12].

Fig. 7 shows the phase current when the actual measured current or the reconstructed waveform is used in the deadtime compensation algorithm. In the first case, the clamping of the current around the zero crossing is quite clear. This result is similar to the one reported in [5], but the technique used here is simpler. The second waveform corresponds to

frequency (Hz)	I _{as} (A)	V*as (V)	V _{as} (V)	error ∆V (V)
1	5.1	5.6	5.4	0.2
2	5.4	7.8	7.6	0.2
3	5.3	10.2	9.8	0.4
5	5.9	14.2	13.9	0.3
10	6.0	25.0	24.7	0.3
20	5.8	46.5	46.4	0.1
30	5.5	68.1	68.0	0.1

 TABLE II

 OUTPUT VOLTAGE USING PROPOSED DEAD-TIME COMPENSATION

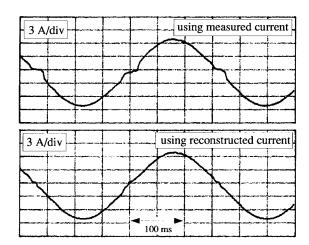


Fig. 7. Phase current. Top trace: using measured current to compensate for dead time; bottom trace: using reconstructed current for dead-time compensation. Fundamental frequency is 3 Hz.

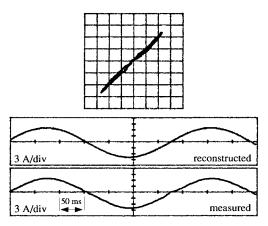


Fig. 8. Measured current at 3 Hz. Top trace: reconstructed current; bottom trace: measured current.

the case where the reconstructed current is used. Fig. 8 shows the measured and reconstructed currents along with a x-y plot indicating an almost perfect match. The improvement achieved by the proposed method is self-evident and the current shows almost no distortion. The very minor distortion still present in the current is due to errors in the computation of the correction voltage ΔV and, to some lesser extent, to the asynchronous sampling of the current. A more accurate calculation of ΔV , however, would bring only a marginal improvement and it would require a more complex model making the method less desirable for low-cost applications.

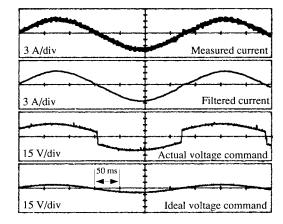


Fig. 9. Measured current at 3 Hz. From top to bottom: phase current, filtered phase current, actual commanded voltage, and ideal commanded voltage.

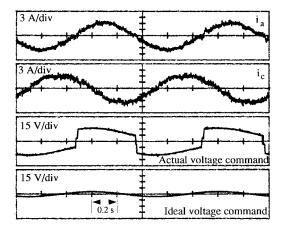


Fig. 10. Measured current at 1 Hz. From top to bottom: phase-a current, phase-c current, actual commanded voltage, and ideal voltage command.

The proposed dead-time compensation method has also been tested as part of a constant V/f drive for output frequencies between 1–60 Hz showing good performance [12]. The worst case scenario corresponds to no-load operation at low frequency where the dead-time effect is much more severe. Experimental results for no-load operation at 3 and 1 Hz are shown in Figs. 9 and 10. The phase-a current (raw and filtered) is shown in Fig. 9, also shown here are the actual commanded voltage (including the compensation ΔV) and the ideal commanded voltage. Results for 1-Hz operation are shown in Fig. 10. In both cases, the line currents show almost no distortion and the magnitude corresponds to rated no-load

current, thus indicating a correct compensation. No low-order harmonics were observed.

It should be noted that the relatively low-sampling frequency used for the current (1 ms) did not affect the steadystate operation at rated frequency. This is due to the instantaneous average characteristic of the phase angle measurement circuit and dead-time compensation strategy used. The dynamic response is limited by the bandwidth of the phase detection circuit. For frequencies above and about 40 Hz, the relative magnitude of the error introduced by the dead time becomes less important and its effect on the performance of the drive is greatly diminished.

V. CONCLUSIONS

The dead-time compensation method proposed in this paper provides a low-cost and efficient means to reduce current distortion in open-loop PWM-VSI drives. The output voltage error produced by the dead time and its influence on the torque output for constant V/f drives has been presented in some detail and a compensation method based on an average technique using a feed forward and a feedback loop has been implemented. The main problem, current detection around the zero crossings, has been solved by using an instantaneous back calculation of the current phase angle. The calculated phase angle is then used in the feed forward compensation loop and the current magnitude is used in the feedback loop. Given the closed-loop nature of this calculation, the zero crossing of the current is accurately obtained. Experimental results validating the proposed method are presented.

Appendix			
PARAMETERS OF THE MACHINE	USED	IN THE	STUDY

TABLE III		
INDUCTION	MACHINE	Data

3 Hp	$r_s = 0.89 \Omega$
230 V	$r_r = 0.73 \ \Omega$
9 A	$L_{s} = 0.065 H$
60 Hz	$L_{r} = 0.065 H$
1740 rpm	$L_{m} = 0.062 H$

REFERENCES

- Y. Murai, T. Watanabe, and H. Iwasaki, "Waveform distortion and correction circuit for PWM inverters with switching lag-times," *IEEE Trans. Ind. Applicat.*, vol. 23, pp. 881–886, Sept./Oct. 1987.
 F. Blaabjerg and J. K. Pedersen, "Ideal PWM-VSI inverter using only
- [2] F. Blaabjerg and J. K. Pedersen, "Ideal PWM-VSI inverter using only one current sensor in the dc-link," in *IEE 5th Power Electronics and Variable-Speed Drives Conf.*, 1994, pp. 458–464.
- [3] B. K. Bose, Ed., *Power Electronics and Variable Frequency Drives*. New York: IEEE Press, 1996.
- [4] R. Sepe and J. Lang, "Inverter nonlinearities and discrete-time vector current control," *IEEE Trans. Ind. Applicat.*, vol. 30, pp. 62–70, Jan./Feb. 1994.
- [5] J. W. Choi and S. K. Sul, "Inverter output voltage synthesis using novel dead time compensation," *IEEE Trans. Power Electron.*, vol. 11, pp. 221–227, Mar. 1996.

- [6] J. S. Lee, T. Takeshita, and N. Matsui, "Optimized stator-flux-oriented sensorless drives of IM in low-speed performance," in *IEEE IAS Annu. Meeting*, 1996, pp. 250–256.
- [7] J. W. Choi and S. K. Sul, "A new compensation strategy reducing voltage/current distortion in PWM VSI systems operating with low output voltages," *IEEE Trans. Ind. Applicat.*, vol. 31, pp. 1001–1008, Sept./Oct. 1995.
- [8] D. Leggate and R. Kerkman, "Pulse based time compensator for PWM voltage inverters," in *IEEE IECON Conf. Rec.*, 1995, pp. 474–481.
- [9] T. Sukegawa, K. Kamiyama, K. Mizuno, T. Matsui, and T. Okuyama, "Fully digital, vector-controlled PWM VSI fed ac drives with an inverter dead-time compensation strategy," *IEEE Trans. Ind. Applicat.*, vol. 27, pp. 552–559, May/June 1991.
- [10] H. Kubota and K. Matsuse, "The improvement of performance at low speed by offset compensation of stator voltage in sensorless vector controlled induction machines," in *IEEE IAS Annu. Meeting*, 1996, pp. 257–261.
- [11] T. C. Green and B. W. Williams, "Control of induction motor using phase current feedback derived from the dc link," in *Proc. EPE'89*, vol. III, pp. 1391–1396.
- [12] A. Muñoz-Garcia, T. A. Lipo, and D. W. Novotny, "A new induction motor V/f control method capable of high performance regulation at low speeds," *IEEE Trans. Ind. Applicat.*, vol. 34, pp. 813–821, July/Aug. 1998.
- [13] J. Kimball and P. T. Krein, "Real time optimization of dead time for motor control inverters," in *IEEE PESC*, St. Louis, MO, 1997, pp. 597–600.
- [14] K. Koga, R. Ueda, and T. Sonoda, "Stability problem in induction motor drive system," in *IEEE IAS Annu. Meeting*, 1988, pp. 129–136.
- [15] N. Mutoh, K. Sakai, N. Fujimoto, A. Ueda, H. Fujii, and K. Nandoh, "Generation method using a software technique for PWM signals with superaudible frequencies," in *IPEC-Tokyo Conf. Rec.*, 1990, pp. 833–840.



Alfredo R. Muñoz (M'88) was born in Valparaíso, Chile. He received the B.S. degree in electrical engineering in 1981 from the Technical University Santa Maria, Valparaíso, and the M.S. degree in electrical engineering in 1995 from the University of Wisconsin, Madison. He is currently working towards the Ph.D. degree at the University of Wisconsin.

From 1981 to 1986, he was with Schlumberger Overseas. In 1987, he became a full-time Lecturer at the Technical University Santa María, where he

is currently on leave and a Research Assistant at the University of Wisconsin. He has been involved in several research projects in the areas of variablefrequency drives and power electronics. He was a Fulbright Fellow from 1993 to 1995. His main research interests include electric machines, ac drives, and power electronics.



Thomas A. Lipo (M'64–SM'71–F'87) is a native of Milwaukee, WI.

From 1969 to 1979, he was an Electrical Engineer in the Power Electronics Laboratory, Corporate Research and Development, General Electric Company, Schenectady, NY. He became Professor of Electrical Engineering at Purdue University, West Lafayette, IN, in 1979, and in 1981 he joined the University of Wisconsin, Madison, in the same capacity, where he is presently the W. W. Grainger Professor for Power Electronics and Electrical Ma-

Dr. Lipo received the Outstanding Achievement Award from the IEEE Industry Applications Society, the William E. Newell Award from the IEEE Power Electronics Society, and the 1995 Nicola Tesla IEEE Field Award from the IEEE Power Engineering Society for his work. Over the past 30 years, he has served IEEE in numerous capacities including being President of the Industry Applications Society.