On Modeling and Testing of Lithography Related Open Faults in Nano-CMOS Circuits†

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Abstract

Scaling of transistor feature size over time has been facilitated by corresponding improvement in lithography technology. However, in recent times the wavelength of the optical light source used for photolithography has not scaled in the same rate as that of the minimum feature size of the transistor. In fact, starting with 180nm devices, the wavelength of optical source has remained the same (at 193nm) due to difficulties in finding a flicker-free, high energy, coherent light source with compatible improvement in lens material for focusing this light. Consequently, upcoming technology nodes (65nm, 45nm, 32nm and 22nm) will be using a light source with wavelength much greater than the feature size. This creates a peculiar problem where line width on manufactured devices is a function of relative spacing between adjacent lines. Despite numerous restriction on layout rules, interconnects may still suffer from constriction due to this peculiarity also known as forbidden pitch problem. A small manufacturing variation turns the constrictions to open faults. Gate leakage current is a significant concern for present and upcoming technology nodes. Due to gate leakage, an open fault is not truly an open circuit. Our simulation studies show that the leakage current steers the floating input of a gate to certain meta-stable states. This property actually makes it easier to detect open faults either through side channel excitation or by stuck-at tests. The major contributions of this paper are (i) lithographic simulation based identification of potential open fault sites, (ii) identification of meta-stable input states for these open inputs, (iii) length calculation for side channel signals for definitive detection of open faults. Together, they provide a complete CAD framework for testing lithography related open faults.

Keywords: Open Faults, Lithography, Forbidden Pitch, Logic Switching Threshold

1. Introduction

As the VLSI technology aggressively marches toward 45nm nodes and below, it is being greatly challenged not only by deep sub-micron design issues, but also by manufacturing and reliability issues. Current test strategies are mainly focused on random defects under the assumption that random particles based defects are the primary mechanisms for yield loss during manufacturing. But continuous scaling of devices has caused feature driven defects to play a major role in high volume manufacturing. It has been shown previously that systematic defects are on the rise compared to random defects for the current and future technology nodes [1]. In this paper, we focus on one of the sources of systematic defects, namely the sub-wavelength lithography related defects. Lithography has become a major concern at technology nodes 65nm and below [2].

Historically, continuation of transistor feature size scaling has been possible through concurrent improvement in lithographic resolution. The lithographic resolution was primarily improved by moving deeper into ultraviolet spectrum of light. However, the wavelength of the optical source used for lithography has not improved for nearly a decade Figure 1. This has lead to development of sub-wavelength lithography.

Line width variation is a subject of major concern as it affects the device performance in integrated circuits. *Forbidden pitch* is one form of line width variation, the occurrence of which was originally reported by Socha *et al.*[3] for the 130 nm technology node. Forbidden pitch refers to a regular line pitch (line width + line separation) where due to destructive interference of light, the line widths shrink dramatically. This issue is a major concern in the very deep sub micron (VDSM) technology nodes of 65nm and below. It was shown in [2], the occurrence of forbidden pitches in 65 and 45 nm nodes lead to breaks in interconnect lines. The open fault problem is compounded by use of Copper (^{29}Cu) as interconnect. Cu is deposited by an electroplating process called damascene and is more prone to open faults [5]. Thus lithography related line width reduction is a major source of concern for open faults.

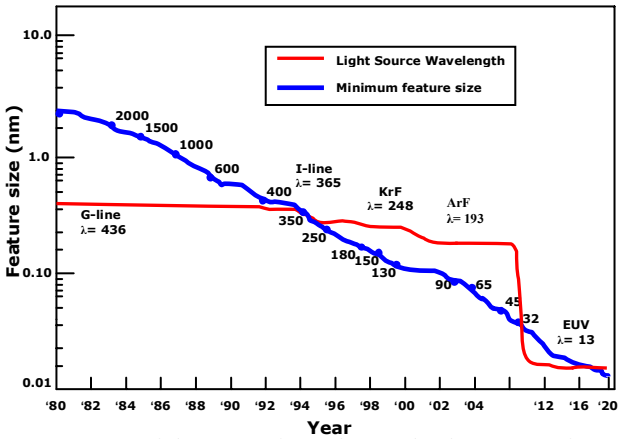

Figure 1 Light Source for various technology generations

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This paper deals with the extraction of such defect locations in a two-step process. In the first step a knowledge base of lithography related line width reduction/pullback is created by running aerial imaging simulation that simulates the lithography process. Such simulations are computationally expensive and can only be run on very small layouts. In the second phase, this library of knowledge is used to scan the physical design layout and faults.

Rest of the paper is organized as follows: In section 2 background and related work is presented. Section 3 describes the open fault extraction procedure and our experimental setup. In section 4, the detectability of open faults in presence of gate leakage is proven. We present experimental results in section 5 before conclusion from the results.

2. Background and Related Work

2.1 Background

As semiconductor manufacturing technology pushes towards the limit of optical lithography, the current state of art processes produce geometries or critical dimensions that are well below the optical wavelength (λ) where, critical dimension (CD) being the smallest width of a feature or the smallest space between two features [7]. For features that are spaced or sized smaller than the optical wavelength, effects due to diffraction, also known as optical proximity effects (OPE) come into play. Optical proximity effect is a well known phenomenon in the field of photolithography [3]. Specifically, these proximity effects occur when very closely spaced layout patterns are lithographically transferred to a photosensitive material (photoresist) on the wafer. This effect results from structural interaction of light waves of closely spaced main features with the neighboring features of a mask layout. This typically leads to undesirable variation in the critical dimension and also exposure latitude of the main feature. The magnitude of the proximity effect depends on the spacing between two features in a mask [8].

OPC and improved light sources have helped push technology for a couple of generations. However, they do not completely address the forbidden pitch phenomenon. There are pitch ranges at which, the exposure latitude of dense features is found to be worse than those of isolated features [4]. Such pitches are termed forbidden pitches and occur due to destructive interference of light waves of the main feature and the side features. The fields produced by the light waves of the side and main features decide whether the existence of side features will increase or degrade the exposure latitude of the main feature. The fields can be at the same phase and having constructive interference or at 180˚ out of phase and producing destructive interference. Forbidden pitch phenomenon is a limiting factor for the current manufacturing technology [6].

identify possible open fault locations for different metal layers based on the line width variation of a specific layer. This is the main thrust of this paper. However, identification of potential open-fault locations is not enough. We need the ability to detect these faults. We present an important result showing that gate leakage in nano-CMOS technologies facilitate detection of open

Optimal illumination and enhanced scatter bar techniques have been used effectively to suppress forbidden pitches in 130nm, 90nm and even in 65nm. However, our previous study shows that this is not adequate at 45nm and below because they lead to unacceptable reduction in line width.

The occurrence of forbidden pitches has been found to be more prominent as we go down to the 65nm and 45nm regime. At the 65nm node, the minimum line width (3λ) for Metal 1 layer is 97.5nm. In our simulation experiments, this width was tuned to get the best possible resolution at a pitch of 174nm. Using the same dose and exposure, forbidden pitches were detected at 354nm. At the 45nm node, the minimum line width (3λ) for Metal 1 is 67.5nm. Like in previous experiment, process was tuned to get the best possible resolution at this width with a pitch of 135nm. However, forbidden pitches were detected at 165nm for which the CD of the metal line goes to zero [2]. The plots in Figure 2Figure 3show the occurrence of forbidden pitches in 65nm and 45nm technology nodes.

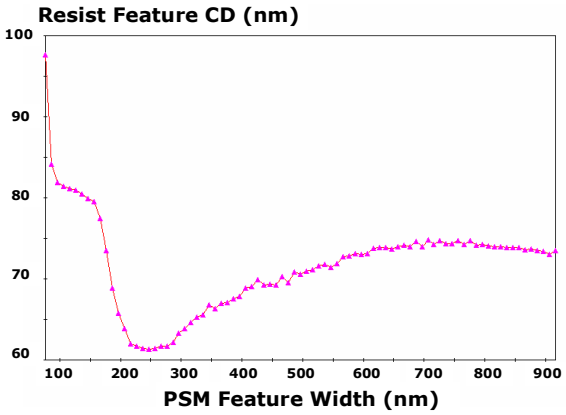

Figure 2 Forbidden Pitches for 65nm node

In these plots, the X-axis represent the pitch (width + separation) while the Y-axis shows the width of the line in image plane. In an unstructured layout, the forbidden pitch may occur due to discontinuity in adjacent lines which may lead to large reduction in line width. The use of copper as interconnects in the current fabrication technology compounds the line width reduction problem because it is prone to open faults [5].

Dense packing of layouts to reduce die area is cause for such regions to occur. Since we discovered a forbidden pitch at 2X the separation for 45nm technology, we

performed aerial imaging simulation on a mask with 3 times the regular gap. Such gaps are a common feature in current layouts being done for 90nm. Simulation shows that such gaps result in constriction of metal lines.

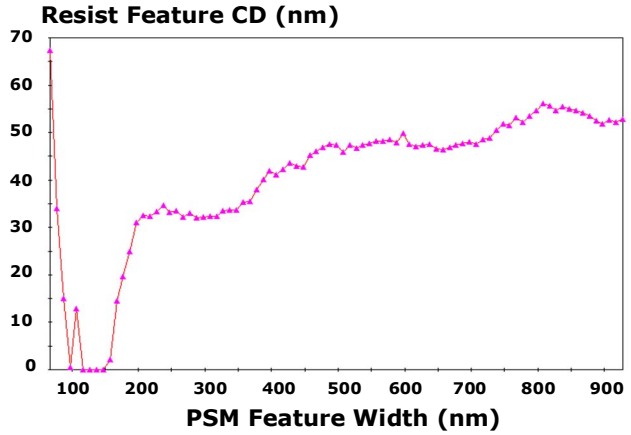

Figure 3 Forbidden Pitches for 45nm node

Such suspect features increase significantly in 45nm technology with a direct impact on yield. If such features are disallowed for lower metal layers, it forces the layout to be constrained to regular patterns in all lower metal layers.

2.2 Related Work

Classically physical defects are modeled in the gate-level representation as lines stuck at a specific logic value [9]. As the miniaturization and the density of devices on VLSI chips increases, open and bridging faults become more important and requires more refined fault models (such as transition fault model [9]) to improve the accuracy of the translation of physical defects into electrical faults. With the consistent progress of VLSI fabrication technology the problem of bridging faults became more prominent [10]. For the current generation VLSI circuits, the total number of break and bridging faults to be considered can easily become prohibitive if we restrict our fault modeling only in the gate level. This problem motivated the researchers to take the layout structure of the circuit into account while dealing with the fault modeling and testing of bridging faults [11][12]. Ferguson et al. [11] extracted physical defects from the circuit's layout and transformed them into transistor-level faults. Jacomet et al. [14] extended Ferguson's basic idea to propose a technology and structure dependent fault extraction process. The extracted faults were weighted according to their likelihood of occurrence. Konak et al proposed a charge based fault extraction and detection approach to circuit opens. Current testing and other parametric test techniques were suggested to detect bridging faults.

As minimum feature sizes continue to shrink, the wavelength of light used in modern lithography systems becomes considerably larger than the minimum line dimensions to be printed. The fabrication industry approaches to tackle this problem by adding more and more stringent design rules. Kahng *et al.* [15] reported a detailed taxonomic description of these design rules and predicted the trend for future physical design.

3. Open Fault Extraction

In this section we describe our defect extraction procedure and explain our experimental setup.

3.1 Methodology

Figure 4shows the overall framework of our methodology. The framework consists of four phases, *viz.* lithography simulation, defect characterization, layout fault extraction and logical fault translation. We now present a brief description of each of the four phases.

3.1.1 Lithography Simulation

In lithography simulation, metal layer masks are generated to find out the forbidden pitches. Experiments were performed by varying the pattern density for a small window of a mask layer to find out the change in critical dimension of those metal lines. The patterns were (i) regular (ii) based on actual layout found in 90nm process and (iii) random. The metal line widths and pitches were chosen to be consistent with current practice [15].

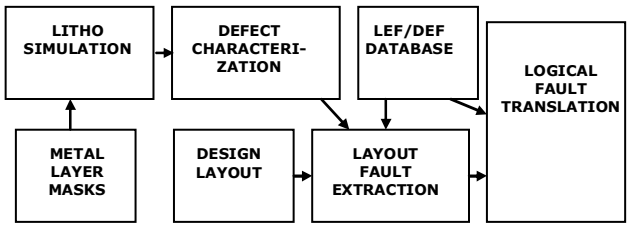

Figure 4 Extraction Methodology

An aerial imaging simulator was used to find the forbidden pitches for the 65nm and 45nm nodes. Experiments were performed on 97.5 and 67.5nm metal lines to create a model of the photoresist after being developed. The metal lines used were of minimum width (3λ) based on design rules.

A change in CD is noted as the pitch varies. At a particular pitch or at a range of pitches, the CD is found to reduce well below the allowable limit. These pitch ranges are called forbidden pitches. The same is done for different metal layers in the design, for which forbidden pitches have to be found. We limit the simulation to the first two metal layers as we do not find the phenomenon prominent in other upper metal layers.

3.1.2 Defect Characterization

Defect characterization involves the process of converting lithographic simulation data into models that can be used to find defect locations in layouts. A set of rules are defined for each metal layer taking pitch and simulation window. Forbidden pitches vary depending on the metal

layer and the simulation region over which the pitches were found.

For 65nm process technology, Metal 1 and Metal 2 layers had forbidden pitches at a specific pitch. The CD of these lines reduced to 30% of the actual tuned width. For the 45 nm process technology, the forbidden pitches were at a range of metal pitches for both Metal 1 and Metal 2 lines. Hence a defect type list with all the above conditions was made as a preprocessing step to facilitate the extraction process. One has to keep in mind that the list is device only for interconnect metal lines that connect between cells and not the metal/poly lines that are present within the cells. The primary reason for this is that cell layouts are from standard cell libraries and are pre-characterized for a design technology. Pitch rules cannot be applied to intra-cell lines.

3.1.3 Layout Defect Extraction

Defects characterized based on lithography simulation have been transformed into layout rules for polygons. A Design Rule Check (DRC) based approach is followed. This approach has been used to extract critical area in layouts [16] but has not been used to extract layout defects caused by manufacturing issues.

Using the DRC rules written for such defects, the geometric features of the layout that were parsed are checked for such conditions. The area of the layout over which these rules are checked depends on the simulation region over which the lithography simulation was conducted. If the condition is met, the error location is flagged and the coordinates are stored. The coordinates indicate the two lines that are at forbidden pitch. An example of such rule check is shown in Figure 5. The region marked by X is the forbidden pitch. The faulty nets on which constriction will happen are marked. We create a database of the LEF and DEF files at the beginning of our extraction procedure. Using the database, we can perform queries to i) obtain the locations of bounding boxes of cell in the design, ii) hierarchical net, cell and pin names and iii) design elements.

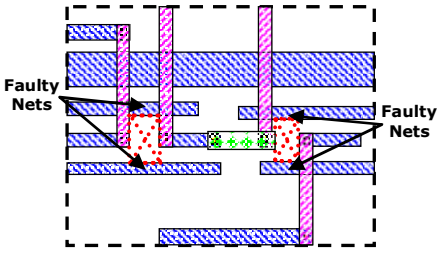

Figure 5 Open fault extraction

Once the error coordinates are obtained, database queries are done to find out what layout nets these fall under. Care must be taken that the complete hierarchical net names of the faulty nets are obtained. Connectivity information is also obtained for the net which will aid in obtaining the logic fault location.

3.1.4 Logical Fault Translation

The traditional approach in solving the problem of mapping layout level defects to logic faults has been solved using layout data (GDS2) and layout versus schematic information (LVS). A cross-mapping database is needed for processing the GDS2 and the LVS information. By using a physical design tool maintained by University of Michigan called Capo [17], we were able to the needed cross-referencing. Thus the physical faults are translated to logical faults.

3.2 Experimental Setup

We used a commercial imaging simulator called PROLITH™ for all our lithography simulation. The metal layer masks used for the simulation were binary masks (BIM). The masks were presumed to be Alternating Phase Shift Masks (Alt-PSM). A Quasar light source was used for this experiment. The wavelength of the light source was fixed at 193nm. The numerical aperture (NA) of the imaging system was 0.93. Forbidden pitch simulations were performed on metal pattern masks for different simulation regions to get an optimal window over which the circuit layouts will be scanned for defects.

We used Cadence Composer v5141USR3 and Cadence Silicon Ensemble 5.3 to generate circuit layouts. Cadence SKILL language was used to define design rules and obtain the defect coordinates for all our designs. A LEF/DEF parser of Capo, a placement tool from University of Michigan was used to perform layout net name mapping from the defect polygons [17].

4. Fault Testability

As discussed earlier, open faults may be induced by lithography related issues. The location of open faults is dependant on the actual layout.

However, identification of potential open-fault locations is not adequate. We need the capability to detect these faults. Earlier, it was shown that such faults may be detected by inducing transition in the adjacent nets and thereby injecting charge into the floating nets [18].

4.1 Meta-stability of Floating Nets

Gate leakage (oxide leakage) is a significant concern for sub-90nm technology nodes. An open net connected to input of a gate is not a truly floating net. To illustrate this point, consider an inverter with an open input. Suppose, the initial voltage of this open net was 0V, the output of the inverter will be at V_{DD}. This condition will lead to gate leakage current in the PFET which will raise the voltage of this open net. Similarly, if the input net started out at V_{DD}, NFET will have gate leakage to bring down the input voltage. In order to determine, whether the floating input reaches a stability value, we ran simulation with different initial conditions for an inverter at 45nm with different initial conditions using BPTM models. It was observed that the input floating net stabilized at either 0.1735V or

0.579V, while the corresponding output voltages were at 0.8V or 0V respectively. This led us to observe that a floating net has *bi-stable* input states. Same observation is repeated with other gate types.

4.2 Testing Bi-stable Floating Nets

Given that a floating input has two stable states, and the corresponding outputs are logical 0 or 1, there are two situations possible: (i) during test application, the floating input stays at a fixed state, i.e., it behaves as a stuck-at fault or (ii) it changes state. The latter can happen when there is charge flow from adjacent nets through capacitive X-talk. In this case a sufficient charge has to be applied to the net to change its value. One way to inject charge into floating nets is through capacitive coupling. The amount of the charge that can be injected by switching of a capacitively coupled net depends on the value of the coupling capacitance, which in turn depends on the coupling length. Another parameter that decides the switching capability is the *logic threshold voltage* of the gate.

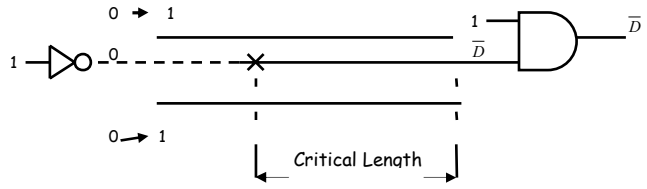

Figure 6 Critical length and side channel excitation technique

Critical coupling length is the length from the receiver over which the aggressor must be coupled to the victim floating net in order to induce a change in the output of the receiver (Figure 6).

We used spice simulations to find the amount of charge required to be induced (coupled) on to the victim by adjacent nets in order for the voltage on the victim net to rise/fall to logic threshold. These capacitance values in turn are used to find the *critical coupling length*. Since coupling capacitance per unit length varies from layer to layer, critical coupling length will vary as well. In Table 1, we show critical coupling lengths by layer when the receiver gate is an inverter. The lengths for other gate types are quite similar.

TABLE 1. Critical lengths for different metal layers

Metal Layer	Critical Length (microns)			
	65nm		45nm	
	Pull High	Pull Low	Pull High	Pull Low
M1	12.8	10	8	7
M2	15.2	13	11.5	10
M3	19	18	16.45	14
M4	20	18.5	16.5	14

The lengths were obtained from Synopsys Raphael tool which was used to perform 3D field simulation to compute coupling capacitances. TABLE 1 shows the critical lengths for metal layers up to M4 in 65 and 45nm nodes. The critical length is different for transition from each meta-stable state of the input. Having obtained critical length for different metal lines, side channel excitation technique based approach can be used to test such lithography induced faults. An open fault with less than critical coupling length cannot switch from one meta-stable state to another. In that case, it behaves as a stuck-at fault. Hence such faults are detected easily.

5. Results

We applied our open fault extraction methodology on ISCAS-85 benchmark circuits. TABLE 2 shows the number of defect locations occurring in each of these circuits due to the forbidden pitch issue at Metal layer 1. As can be seen from the result, the number of open fault sites increase from 65nm to 45nm technology nodes. We have also observed that the sites not only occur on interconnects between cells, but also within the standard cells. TABLE 3 shows the total defects that occur on Metal layer 2. As Metal 2 is not used for intra-cell routing, they are present only to connect different cells within the layout.

TABLE 2. Lithography aware open fault statistics for ISCAS-85 benchmark circuits (METAL I layer)

ISCAS 85 Circuit	Number of Defect Locations					
	65nm			45nm		
	Intra-cell	Inter-cells	Total	Test concern	Design concern	Total
c17	2	2	4	25	5	30
c432	34	6	40	370	27	197
c499	61	11	72	221	31	252
c880	8	8	16	177	73	250
c1355	60	10	70	241	84	325
c1908	15	15	30	265	91	356
c2670	25	23	48	336	45	381
c3540	34	26	60	361	134	495
c5315	91	65	156	315	231	546
c6288	62	22	84	344	272	616
c7552	126	41	167	698	153	851

TABLE 3. Lithography aware open fault statistics for ISCAS-85 benchmark circuits (METAL II layer)

ISCAS 85 Circuit	Number of Defect Locations	
	65nm	45nm
c17	0	3
c432	2	37
c499	2	72
c880	5	116
c1355	0	73
c1908	0	120
c2670	8	221
c3540	14	264
c5315	11	482
c6288	28	694
c7552	62	1073

In TABLE 4 we draw a comparison between our lithography aware open fault count and conventional stuck-at fault count for ISCAS-85 benchmark circuits. Different metal layers have different width and pitch. Consequently, lithography related problems affect them differently. Since, Metal layer 1 and 2 are usually the densest and by

implication more prone to open faults, we present a comparison between the numbers of possible open faults in these two layers with the total number of stuck-at faults. The point of this comparison is to show that lithography based technique narrows the fault list down and allows better targeting of test patterns. If it was the other way around, i.e., the total number of potential defects was very large then, there could be a potential issue of test data volume.

TABLE 4. Comparison between lithography aware open fault count and stuck-at fault count for ISCAS-85 benchmark circuits

ISCAS 85 Circuit	Lithography aware open fault count		Stuck-at fault count [19]
	65nm	45nm	
c432	42	200	524
c499	74	289	758
c880	21	322	942
c1355	70	441	1574
c1908	30	429	1879
c2670	56	602	2747
c3540	74	759	3428
c5315	167	1028	5350
c6288	112	1310	7744
c7552	229	1924	7550

Once the open fault sites are extracted, the side-channels are established by querying the physical netlist data base.

6. Conclusion

In this paper we made a case study for open faults induced by lithography related problems such as optical defocus. This has already been studied as a physical design problem. In this paper we examined the problem from a test aspect. We presented a methodology for extracting locations of such open faults. We showed that in general the number of such open faults is smaller than the number of stuck-at faults. We studied detection of such open faults and showed that due to presence of gate leakage, the floating inputs gravitate towards meta-stable voltage conditions. In this scenario a charge introduced by side channel excitation using capacitive cross-talk that can exceed switching threshold of the receiver can lead to detection. We also computed minimum length of side-channels required for such open fault detection using side-channel excitation method. ATPG for side channel excitation is well-established in literature.

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