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On-Orbit Flight Results from the Reconfigurable Cibola Flight Experiment Satellite (CFESat)

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Abstract—The Cibola Flight Experiment (CFE) is an experimental small satellite developed at the Los Alamos National Laboratory to demonstrate the feasibility of using FPGA-based reconfigurable computing for sensor processing in a space environment. The CFE satellite was launched on March 8, 2007 into a low-earth orbit and has operated extremely well since its deployment. The nine FPGAs used in the payload have been used for several high-throughput sensor processing applications and for single-event upset (SEU) monitoring and mitigation. This paper will describe the CFE system and summarize its operational results. In addition, this paper will describe several SEU detection circuits that were uploaded to the spacecraft and real-time SEU results obtained from these experiments.

1. INTRODUCTION

There is growing interest in using FPGAs within space systems due to low non-recurring engineering (NRE) costs, compressed life cycles and reduced costs (compared to ASICs), computational performance advantages, and reconfigurability. The ability to reconfigure the FPGA device after the spacecraft has launched allows the FPGA to be updated to accommodate evolving mission objectives, process data from multiple sensors, incorporate new scientific knowledge into the computational algorithms, or even to fix faults within the system. A variety of projects have demonstrated the benefits of using FPGAs in a spacecraft [1], [2], [3].

FPGA-based satellites include such projects as the Australian satellite FedSat, which uses FPGAs as part of its high performance computing payload [4]. The Mars rovers Discovery and Spirit each use FPGAs for motor control and landing pyrotechnics [1]. Further, most modern commercial and military satellite use anti-fuse FPGAs in a variety of applications [5].

While FPGAs offer a number of unique benefits for spacecraft electronics, they are susceptible to single event effects (SEE). FPGA devices contain a large number of internal memory cells that can be upset by high energy particles. They

also contain memory cells for user flip-flops, internal block memory, and for configuration memory (SRAM based FPGAs). Upsets within the configuration memory are especially challenging as these upsets may change the programming of the FPGA. Any system that incorporates FPGAs must provide a strategy for mitigating against these single-event upsets (SEU).

The Cibola Flight Experiment Satellite (CFESat), developed by Los Alamos National Laboratory, tests the suitability of FPGAs as an on-board reconfigurable processors in a spacecraft [2]. The Cibola Flight Experiment may receive any new FPGA configuration bitstreams from an uplink. The ability to “download” new configurations to the satellite payload allows the system to perform an unlimited number of processing functions. Further, this system incorporates a number of techniques to mitigate the effects of radiation induced upsets within the FPGAs.

This paper will describe the CFE system and initial results. The paper will begin by describing the system architecture and the techniques that were used to provide SEU mitigation. Next, the paper will briefly discuss the launch and operation of this satellite in its low-earth orbit (LEO) including radiation effects as well as thermal/power concerns. A number of SEU detection experiments were created for the system and uploaded to the orbiting spacecraft. Results from these experiments will be presented as well as lessons learned from the system.

2. CIBOLA FLIGHT EXPERIMENT (CFE)

The Cibola Flight Experiment is an aggressive small satellite project completed at Los Alamos National laboratory and funded by the Department of Energy to perform ionospheric and lightning studies. The satellite measures and detects impulsive events in a complex RF environment and groups events together for postprocessing. The real-time processing demands of this system are immense and cannot be performed using multi-processing with traditional processor architectures. A novel feature of the CFE architecture is the use of reconfigurable computing with FPGAs to perform the processing real-time. This section will summarize the CFE computing architecture with an emphasis on the reconfigurable

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computing aspect. The reference [2] contains a more in-depth description of the details summarized in this section.

System Architecture

The architecture of the processing payload of CFE is shown in Figure 1 and was designed specifically for high-throughput RF sensor processing. As seen in this figure, the CFE payload includes an R6000 microprocessor, spacecraft communications interface, a digitally controlled radio tuner, a two channel, 12-bit, 100 MHz analog to digital converter, three reconfigurable computing processors using Xilinx Virtex FPGAs, and non-volatile memory to store program and configuration data.

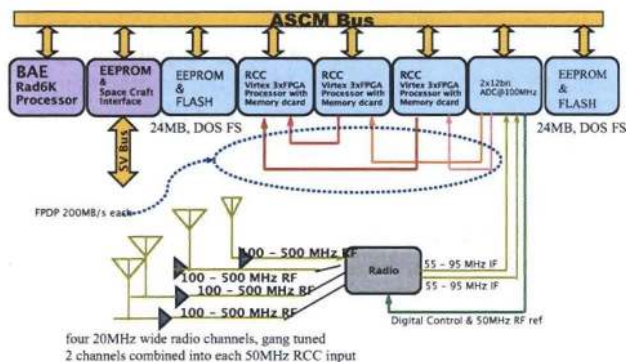


Figure 1. Payload Block Diagram

The RAD6000 30 MHz microprocessor, a radiation hardened R6000 processor supplied by BAE, controls all of the payload digital modules and manages payload communications with the vehicle. The processor includes 8 Mbytes of radiation-hardened SRAM and executes the VxWorks operating system. Although this processor and its associated SRAM are radiation-hardened, the processor architecture is almost two decades old and does not have the computational power necessary to perform the on-board sensor processing.

The payload uses both EEPROM and flash memory for non-volatile storage. Three banks of 1 Mbyte of EEPROM are available to store the operating system and binary user code objects for the microprocessor. Two banks of flash memory (24 Mbytes each) store Xilinx configuration bitstreams used to configure the Xilinx Virtex devices. More than 20 Virtex 1000 configurations, without the use of compression, can be stored in flash memory. Error control coding (ECC) is incorporated to mitigate SEUs that occur during read or write operations.

The analog front end includes four RF channels, each connected to a distinct log-periodic antenna, that can be 'gang' tuned by microprocessor command between 100 and 500 MHz. This configuration is designed to make high fidelity interferometric measurements. All four RF channels have an instantaneous bandwidth of 20 MHz. Two RF channels are combined into each of the 50 - 100 MHz IF ADC inputs; this provides input from all four antennas simultaneously to

the reconfigurable processors. The analog IF is sampled at 100 MHz with 12-bit resolution. The output of the payload ADCs is distributed across a network of point-to-point 200Mbyte/sec (32 bit x 50 MHz) TTL buses derived from the Front Panel Data Port (FPDP) specification. ADC data cascades through the three reconfigurable computers. Two reconfigurable computers each receive one channel of ADC data for preliminary processing, while the third RCC combines the two intermediate results into a final measurement.

Reconfigurable Computer (RCC) Architecture

One of the primary objectives of the Cibola Flight Experiment is to demonstrate the suitability of Xilinx Virtex FPGAs for space applications [6]. To this end, the CFE payload was built around three reconfigurable computer (RCC) modules used to perform processing duties for a variety of experiments (see Figure 2). Each RCC module uses three Xilinx Virtex XQVR1000 CG560 FPGAs as the data processors. The FPGAs are organized in a ring, and each has identical pinouts so they may share configuration files. This design detail reduces the amount of nonvolatile memory needed for FPGA configurations, the required uplink bandwidth, and provides for greater reliability through redundancy. In addition, complex designs only need to meet timing requirements once, reducing design time on the ground. The module has two high bandwidth TTL buses for moving data on and off the card. The nine FPGAs provide over 9 million system gates and over 1 Megabyte of block RAM memory.

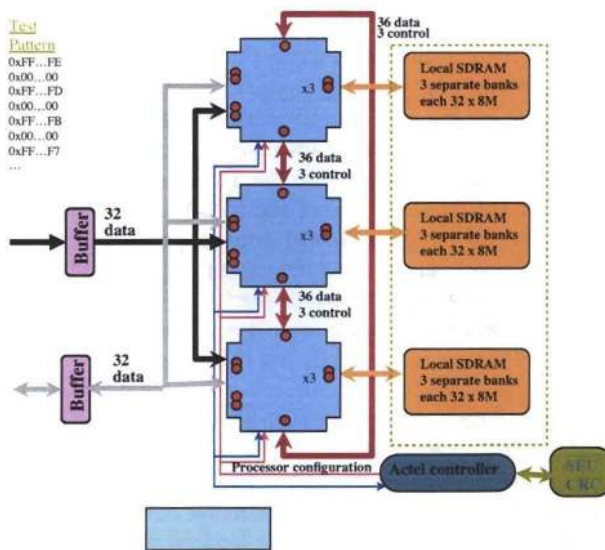


Figure 2. RCC Module Diagram

Each Virtex FPGA has 3 banks of independent memory; each bank is comprised of four Hyundai 64Mbit SDRAMs organized as 8 M x 32-bit wide for a total of 288 Mbytes per module. Each RCC module also has microprocessor access through an Actel RT54SX32S device that acts as a microprocessor interface and board controller. The Actel provides watchdog monitoring for the three Xilinx FPGAs as well as a configuration interface, which aids in CFE's SEU mitigation

scheme for the Xilinx FPGAs.

The use of Virtex FPGAs in this system may seem old and out of date when compared to FPGAs available today. However, the Virtex FPGA family was state of the art when the CFE system was first designed. Since all satellite systems go through an extensive design, qualification, and testing procedure, the components used on orbiting satellites typically lag far behind the components available commercially. Furthermore, the Xilinx Virtex FPGA was the first SRAM-based FPGA to go through extensive reliability qualification for radiation environments[7]. Many of the SEU mitigation techniques developed to support SRAM-based FPGAs were developed using this family.

SEU Mitigation

One of the most important issues that must be addressed when using SRAM-based FPGAs in a satellite is the occurrence of SEUs within the device. FPGA devices contain a large number of internal memory cells that can be upset by high energy protons, neutrons, and heavy ions. FPGAs contain memory cells for user flip-flops, internal block memory, and for configuration memory. Upsets within the configuration memory are especially challenging as these upsets may change the computational function of the FPGA. Any system that incorporates FPGAs must provide a strategy for mitigating against these SEUs.

The Cibola Flight Experiment investigated and developed techniques at the system level and application level for providing reliable operation of the SRAM-based FPGAs. First, the RCC boards used the QPro Virtex radiation hardened FPGAs [8]. These FPGAs use an epitaxial process that provides immunity against single event latch-up (SEL, a destructive failure) to an LET of 125 MeV. The .25 micron process provides for approximately 100 K Rad(Si) total ionizing dose (a cumulative and destructive radiation effect). These FPGAs are not, however, immune to SEUs within the user flip-flops, memories, and configuration data.

To detect and repair upsets within the configuration memory, the CFE system employs a form of configuration scrubbing [9]. Configuration scrubbing is accomplished at the system level with the use of an Actel, radiation tolerant fused-based FPGA. This device detects configuration SEUs by continuously reading the bitstream on each FPGA device through configuration readback. A cyclic-redundancy check (CRC) is calculated for each frame of a configuration (the finest granularity available for reconfiguration). The 'on-the-fly' CRC is compared against the codebook CRCs that are precomputed on the ground prior to uplinking the bitstream. When an upset is detected by a CRC mismatch, a microprocessor interrupt is generated. The microprocessor responds to the interrupt by fetching the frame data from FLASH and partially reconfiguring only the corrupted frame (156 bytes for the XQVR1000) and then performs a previously determined function such as resetting the system.

In addition to configuration scrubbing, a variety of application-specific mitigation techniques have been developed for CFE. Specific techniques that have been applied include half-latch removal [10] and triple modular redundancy (TMR) [11], [12]. Half-latch removal involves the removal of weak keeper circuits that cannot be repaired through scrubbing. TMR involves the triplication of circuit resources and the use of majority voters to isolate any single upset within the circuit. Scrubbing involves the continuous configuration of the FPGA to "clean" upsets that occur. Scrubbing prevents the accumulation of configuration upsets in order to significantly reduce the probability of getting a multi-bit upset. Together, these two techniques allow an FPGA to be used reliably in a variety of space environments.

3. CFE LAUNCH AND ORBIT RESULTS

CFE was launched into a circular low-earth orbit (560 km) on March 8, 2007 on a Lockheed Atlas-5 Medium rocket (STP1)¹. Ground station connectivity was established quickly after the launch, and successful communication with the satellite has been consistent over the 22 months of flight time.

Since its launch, CFE has received configuration data from the ground more than three dozen times, both regaining and increasing the portfolio of experiments within the reconfigurable payload. Over 18,000 experiments have been performed, where an experiment is the configuration of one or more Virtex devices and collection of data that is telemetered to the ground. This section will summarize the operation of the CFE in space including its power and thermal performance, SEU rates, and design applications.

In-Orbit Temperature Control and Power Consumption

A major design concern of CFE was the satellite's ability to adequately dissipate the heat generated by the FPGAs. It is well known that some high-density FPGA configurations may consume a large amount of power and thus generate a lot of heat. Further, the orbit environment includes wide temperature fluctuations that introduce stress on the mechanical assembly. Specifically, the FPGA to printed circuit board interface experiences [2]. extreme temperatures fluctuations as well as frequent cycling from low to high temperatures. The depth and frequency of these cycles reduce the reliability of both the die and the printed circuit board assembly. To help with heat dissipation, a system of heat pipes is used to limit the maximum temperature of the FPGAs. The heat pipes are passive and particularly well suited for this application. The heat pipe functions are similar to a diode. When the temperature at one end reaches the 'on' point, heat flows very efficiently by exploiting phase changes in a working fluid (in this case water). When the temperature drops below the set point, the heat pipe effectively turns off. This function helps limit both hot and cold temperature extremes experienced

¹The current location of the CFE satellite can be tracked by visiting the following URL: <http://www.n2yo.com/?s=30777>

by the assembly.

To mitigate against potential thermal problems, reconfiguration of the payload FPGAs is carefully monitored and scheduled in order to minimize both extremes in temperature and the number of cycles from hot to cold. Temperature sensors are included on all FPGA die to monitor the heat. Figure 3 displays the temperature history of one of the FPGAs to demonstrate the temperature fluctuations experienced by the reconfigurable computing boards. While the median temperature of the die are kept within a reasonable operating temperature (between 5°C and 25°C), the minimum and maximum measured temperatures involve a wide range between -10°C and 35°C. Through careful scheduling of applications on CFE, an acceptable temperature range can be maintained. Safety task monitoring will reset the system if temperature trip points are exceeded.

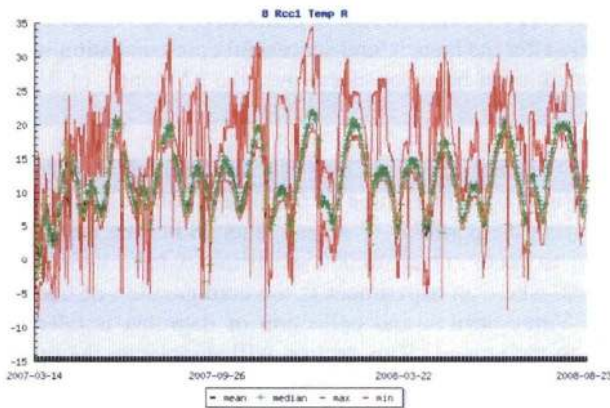


Figure 3. RCC1 FPGA A Die Temperature History

Another important concern on CFE is the power dissipation of the FPGAs. All power on the spacecraft is generated from solar panels and stored in Lithium Ion batteries. The power available to the payload is limited by the power generation from these panels. The FPGA configurations that are downloaded to the spacecraft and configured onto the FPGAs must be carefully scheduled to insure that the FPGA power consumption does not exceed the power production. The current consumption of each FPGA is carefully monitored – Figure 4 plots the current consumption of one of the FPGAs in the system. The maximum peaks in current consumption correspond to different experiments that are executed on the platform. These experiments, however, are not run for long periods of time as there is not sufficient power generation to support them. These high-throughput, high-power applications are mixed with other low-power experiments to keep the average power consumption within an acceptable range (note the relatively low mean current consumption). Power intensive designs run when more power is available, while lower power applications run when power constraints dictate. The highly dynamic power profile drives the thermal cycling and stresses the thermal management system.

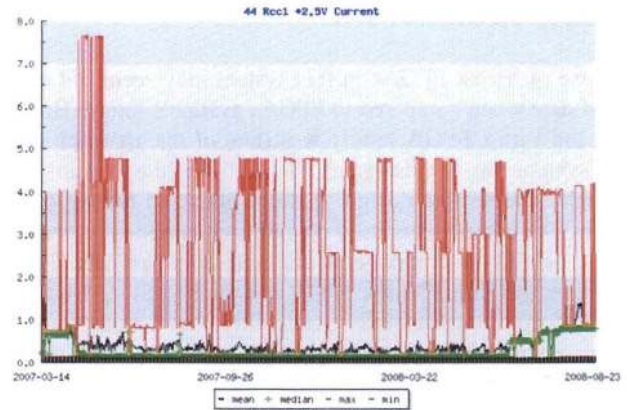


Figure 4. RCC1 Board Level +2.5V Current Consumption (Amps)

In-Orbit SEU Rate

As described earlier, CFE was designed to operate while SEUs occur within the FPGA configuration bitstreams. Several studies were performed to estimate the upset rate of the FPGAs in this orbit [13], [14]. These estimates were made using the CREME96 modeling environment and results from radiation testing on Xilinx Virtex devices [7]. The estimated SEU upset rates for the Virtex in this low-earth orbit are summarized in Figure 5. As seen in Figure 5, the estimated SEU rate for its orbit varies from 0.5 SEUs per device day (solar max, best case estimate) to 26 SEUs per device day (solar minimum, peak trapped protons).

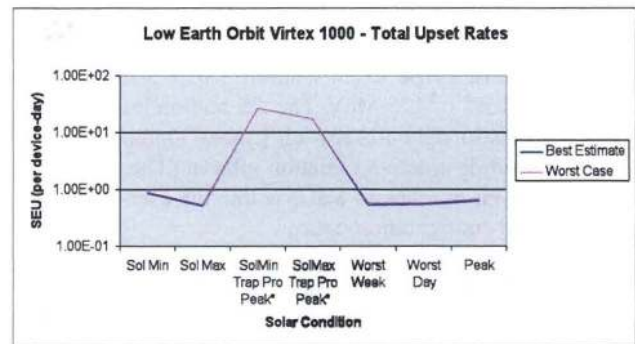


Figure 5. Anticipated Upset Rate Graph

All SEUs within the device have been logged during the 22 months of CFE to measure the actual SEU rates of the system. Through configuration scrubbing, 642 SEUs have been detected over 2436.3 device days resulting in an average upset rate of .264 upsets per device day. This is far lower than the best case estimate and much lower than any worst-case conditions. With nine FPGAs in the payload, CFE averages 2.4 SEUs per day.

The SEUs do not occur uniformly as the spacecraft orbits around the earth. Figure 6 plots the location of the SEUs that have been detected in CFE FPGAs. The vast majority

of SEUs, detected by configuration readback, occurred in the area known as the South Atlantic Anomaly (SAA). This is the region where the Van Allen radiation belt passes closest to the Earth's surface.

CFE Designs

There have been three dozen different FPGA configurations uploaded and tested on the CFE satellite. From these, at least 18,000 experiments have been performed. These design experiments can be divided into two broad categories: analog signal processing/reconfigurable computing and SEU measurement/mitigation.

The signal processing circuits interface directly to the on-board ADC to process sampled data from the satellite antennae. These circuits exploit the parallelism, specialization, and customization of the FPGAs to provide far more computational density than is available with traditional radiation-hardened processors. Examples of this class of circuits that have been run on the satellite include several software defined radios (SDR), demodulators, decoders, and high-throughput FFT engines. In all cases, these circuits successfully demonstrate the computational benefits of using FPGAs in a remote sensing satellite environment.

An important challenge of these signal processing circuits is their high power dissipation. As described in Section 3, these circuits exhibit high peak power consumption, which stresses the energy and thermal management systems of the satellite. Because of this, the scheduling of these circuits must be carefully managed to insure that the FPGAs do not consume more power than is generated or generate more heat than can be dissipated.

The second group of circuits tested on CFE are those used to measure SEU rates and test SEU mitigation strategies. A number of novel SEU mitigation techniques were developed during this project. Several of these techniques are being tested on the CFE FPGAs. These experiments provide data collected in the genuine environment that yields insight into the behavior of the FPGAs and appropriate mitigation approaches. Section 4 will describe several detection experiments and the results in more detail.

One challenge faced by these SEU mitigation experiments is the low SEU rate compared to accelerator experiments or fault injection experiments. At a rate of one SEU upset/device day, it requires long experiment times to collect data and generate meaningful results to validate these techniques. As described in Section 3, only 642 SEUs have been observed during the 674 days of flight time. This is orders of magnitude less data than the data generated through artificial means.

4. DETECTION EXPERIMENTS

An important class of applications that have executed on CFE are SEU detection experiments. These experiments were

created to detect SEUs from *within* the FPGA fabric using additional logic and well known fault detection techniques. This in-circuit SEU detection operates in parallel with the scrubbing-based SEU detection scheme implemented in the Actel FPGA.

The SEU detection within the FPGAs on CFE employs a technique known as duplication with compare, or DWC (see Figure 7). To detect upsets in a circuit with DWC, two identical copies of the circuit run continuously while circuit outputs are compared at different points by comparator circuitry. If the outputs of the two circuit copies disagree at any point, an error has occurred in one of the circuit copies, and the comparator at that point in the circuit outputs an error code. The outputs of all comparators in the circuit are merged to form a circuit-level error code which signifies the presence or absence of upsets in the FPGA [15].

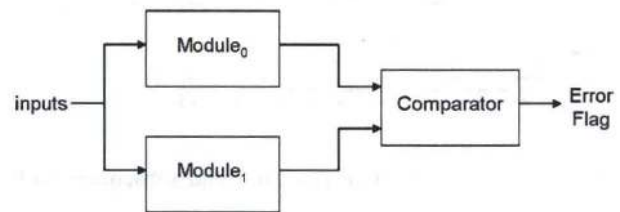


Figure 7. Duplication With Compare (DWC)

The in-circuit duplication experiments will only detect configuration SEUs for configuration bits that actively impact the circuit configured on the device. As described in [16], only a fraction of the upsets that occur will be detected because only a fraction of the configuration bits are used to configure any given circuit. Designs that utilize most of the FPGA logic resources typically use 10% or less of the configuration bits. Because of this, the DWC detection circuits will only detect a fraction of the SEUs that are detected by the readback mechanism.

One of the goals of these experiments is to detect as many upsets as possible. To do this, the design experiments must be as large as possible to provide sufficiently large "targets" for the high-energy particles. If the circuits are small, these experiments will not generate sufficient data. Further, these design experiments must consume as little power as possible. These experiments were scheduled onto CFE as "background" tasks when other high-throughput experiments were not or could not be scheduled.

Several detection experiments were created over a period of time as the detection methodology was refined and new detection mechanisms were added. Each subsequent experiment added onto the abilities of the previous experiment. The following subsections will summarize each experiment and the experimental results.

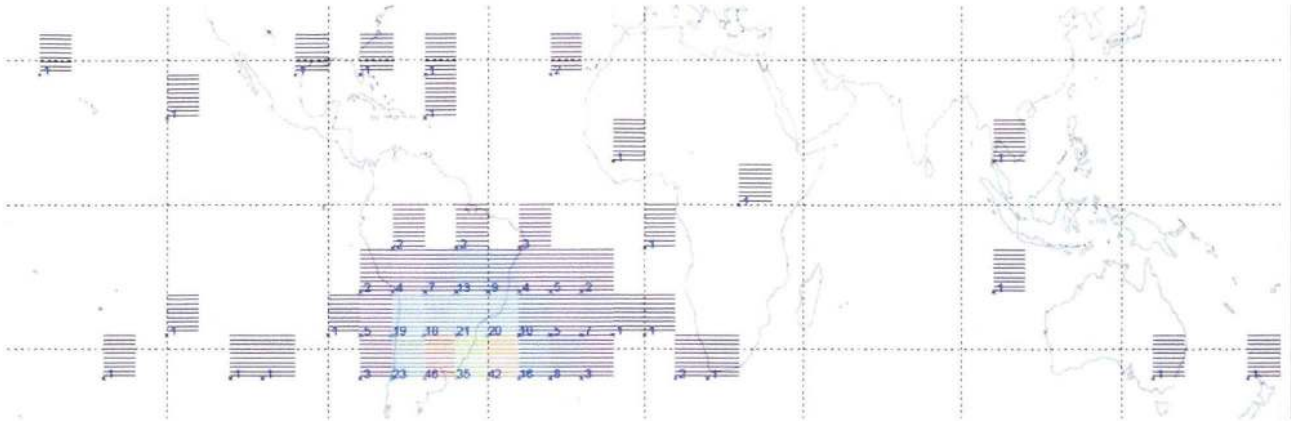


Figure 6. SEUs by Region

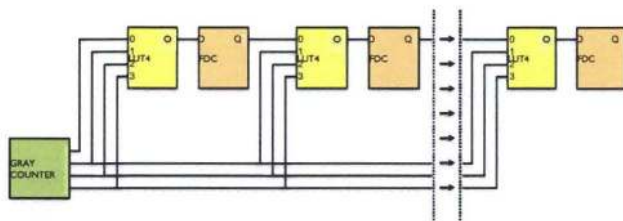


Figure 8. The Gray code generator and subsequent shift register.

SEU1 - Configuration Upsets

The first SEU detection experiment, named *SEU1*, was designed as a low-power simple circuit that does *not* perform in-circuit detection. In this experiment, all 9 Xilinx FPGAs in the payload are configured with a simple circuit containing little logic and consuming minimal power. This simple experiment relied on satellite's readback and configuration scrubbing technique for detecting and correcting SEUs in FPGA configuration memory. This experiment was created before the in-circuit detection techniques were available.

SEU1 executed for 455.3 device days of operation (all 9 FPGAs operating for a total of 50.6 days). During this period, the readback process detected 216 SEUs indicating an upset rate of .47 upsets per day.

SEU2 - Online Detection

SEU2 is a more sophisticated test than *SEU1* and the first experiment to implement the in-circuit detection using DWC. The base circuit of *SEU2* (i.e., the circuit before DWC is applied) includes a long 32-bit wide shift register driven by a gray code pattern generator (see Figure 8). A gray code was used to minimize the dynamic power. LUTs are inserted between each shift register with a pre-determined logic pattern. The use of LUTs between the registers provides more logic "area" for SEUs to hit. The output of each LUT drives the input of a flip-flop and the LUT inputs are driven by upstream flip-flops and the gray code counter.

In order to accommodate future detection designs, the base circuit of *SEU2* was designed to be entirely parameterizable in depth. Parameterization simplifies the process of creating a design that "fills" a device. This base circuit will be used in subsequent SEU test experiments.

SEU2 replaced *SEU1* on June 17, 2008 and operated for 101.6 device days. During this time, 46 SEUs were detected with 4 of the 46 SEUs detected by the DWC circuitry (8.7% sensitivity).

SEU3 - BRAM

The *SEU3* experiment extended *SEU2* by detecting and reporting SEUs that occur within the block RAMs (BRAM) on the Virtex FPGAs. In the previous tests, there was no way to discriminate between upsets in any particular region of the device. For this test, a custom circuit was designed to detect BRAM SEUs by continuously scanning the entire BRAM memory, identifying SEUs, and reporting the total number to the processor. After receiving confirmation from the processor that the number has been recorded, the circuit proceeds to scrub (repair) the BRAM with predefined data.

Figure 9 shows the architecture of this BRAM scrubber and detector. This circuit includes a single gray code address generator (to reduce dynamic power) to drive all BRAM circuits, an error detector, and a scrubber. The scrubber inserts a 0xAAAA pattern into the BRAM and repairs this value whenever an upset is found. If any upsets were present when the BRAM has completed a scan, the processor is interrupted and the number of upsets is reported.

In addition to the BRAM scrubbing/detector circuit, *SEU3* includes the gray code shift register used in *SEU2* (Figure 8). Because additional logic is needed for the BRAM scrubber, the shift register is smaller in *SEU3*. The BRAM scrubber/detector is also sensitive to upsets. DWC is applied to this circuit as well to prevent erroneous data being reported due to SEUs in the detection circuitry. Should the DWC comparison circuitry detect an upset, an interrupt to the processor

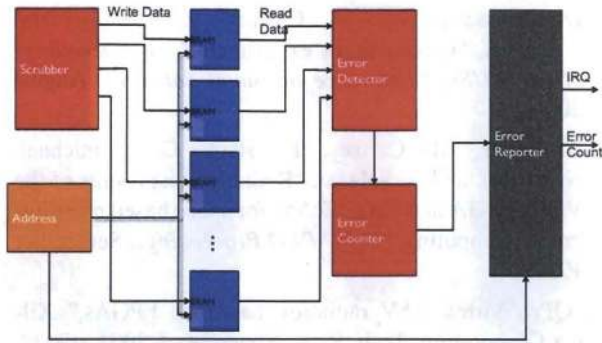


Figure 9. BRAM Scrubber and SEU Detector

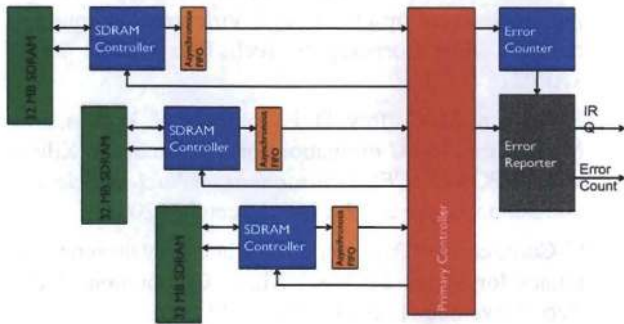


Figure 10. SDRAM scrubber

causes the FPGA to be reset and the configuration frame is fixed through conventional scrubbing.

SEU3 replaced *SEU2* on July 14, 2008 and has been operational for 976.7 device days. During this time, 274 SEUs were detected with readback and 20 of these SEUs were detected by the DWC detection logic (7.3% sensitivity). One of these 20 SEUs occurred within the BRAM scrubbing logic. In addition, 23 BRAM upsets were detected by the scrubber. Twenty-two of these upsets involved single bit upsets while one of the 23 included two upsets within the BRAM.

SEU4 - SDRAM

The final detection test, *SEU4*, was designed to detect upsets within the SDRAM memory associated with each RCC FPGA (see Figure 2). A basic SDRAM controller was designed to run at the SDRAM clock rate of 52 MHz. As there are three 32 MB SDRAM banks for each FPGA, three SDRAM controllers were required in each FPGA (see Figure 10).

The SDRAM control circuit initializes the SDRAM memory by writing the pattern 0xAAAA in all 96 MB of SDRAM. After initialization, it continuously scans the SDRAM, one bank at a time, looking for deviations from this pattern. SDRAM refresh is integrated with the scanning/scrubbing process to insure valid data. Upon completing a scan in which upsets are detected, the circuitry interrupts the processor to report the final upset count. When the processor has acknowledged

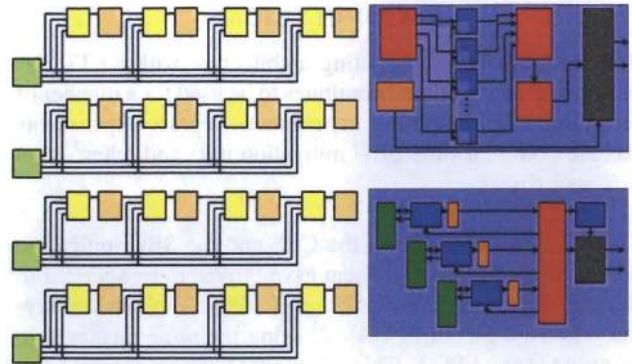


Figure 11. *SEU4* consists of both the BRAM and SDRAM detection tests, with the remaining space filled with the detection test of *SEU2*.

Table 1. CFE SEU Application Results

	Device Days	Config SEUs	SEUs / D.D.	DWC SEUs	BRAM Upsets
<i>SEU1</i>	455.3	216	.47	N/A	N/A
<i>SEU2</i>	101.6	46	.45	4 (8.7%)	N/A
<i>SEU3</i>	976.7	274	.28	20 (7.3%)	23
<i>SEU4</i>	N/A	N/A	N/A	N/A	N/A

this interrupt, the SDRAM circuitry scrubs the entire array of SDRAM and resumes its scan.

The SDRAM controller and scrubber/scanner is triplicated using the BL-TMR in order to minimize the possibility of an upset occurring within the circuitry and causing erroneous data to be reported. The *SEU4* test merges the SDRAM circuitry with the existing *SEU3* detection test to provide detection for logic, BRAM, and SDRAM. The combined *SEU4* detection experiment is shown in Figure 11.

The *SEU4* detection experiment has not yet been scheduled for CFE flight time. We expect to configure CFE with *SEU4* sometime in the month of January².

Results

The four SEU detection experiments have been operational for a total of 1533.6 device days (see Table 1). Within this time, 536 SEUs have been detected through readback, 24 SEUs have been detected with on-circuit error detection, and 23 SEUs within the BRAM have been detected with BRAM scrubbing. The detection experiments provide operational validation of the DWC approach and provide greater visibility into the impact of SEUs on the device. These and other SEU detection experiments will continue to be used on CFE.

²Note to reviewers: we expect data from the *SEU4* experiment by April and will update the paper to include these results when they are received.

5. CONCLUSIONS

The reconfigurable computing architecture within CFE has performed very well and continues to be used for a number of reconfigurable computing experiments. Future experiments include both real-time SEU mitigation tests and other signal processing tests.

The RCC modules within the CFE and the SEU mitigation approach used to protect them have proved to be successful. Several techniques are worth mentioning. A symmetric layout was used for all FPGAs allowing the same bitstream to be used for any FPGA. This symmetric layout was very helpful in simplifying the design and reuse of bitstreams across the platform. The dynamic command dictionary and on-orbit run-time linking was very convenient for allowing run-time scheduling and uploading of new FPGA bitstreams and the SEU scrubber design worked flawlessly.

While the Xilinx Virtex FPGAs have worked very well for this experiment, newer FPGA architectures will have a big impact on computational density and power. Specifically, the DSP48 primitives found in Virtex II and successor FPGAs would significantly reduce the size and power of the signal processing circuits used in this system. Also, the high speed serial I/O found on next generation FPGAs would significantly reduce the number of I/O pins needed for inter-FPGA communication. Even more importantly, a high speed serial network incorporating a runtime reconfigurable cross-point switch would allow the network topology to change for each application. This increased flexibility would allow the FPGAs to be used more efficiently than a hardwired network topology. This approach also increases the robustness of the system by allowing degraded or failed components to be gracefully removed from the system. A number of FPGA architectures succeeding the Virtex have been qualified for space operation and can be used on future missions. CFESat, as a technology pathfinder, has effectively demonstrated the importance of high-performance reconfigurable computing.

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