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On the Characterization and Separation of Trapping and Ferroelectric Behavior in HfZrO FET

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ABSTRACT *N*-channel FETs with ferroelectric (FE) HfZrO gate oxide are fabricated, showing steep subthreshold slope under certain conditions. Possible origins of I_D–V_G hysteresis, the hysteresis versus subthreshold slope tradeoff, dependence on the bias voltage and temperature and the competition between trapping and FE behavior are reported and discussed. A band of active traps in the FE layer responsible for charge trapping during device operation is characterized. Transient I_D–V_G measurements are introduced to facilitate differentiating between trapping and FE behavior during subthreshold slope measurements.

INDEX TERMS Steep-slope FET, ferroelectric FET, trap characterization.

I. INTRODUCTION

The transfer characteristic of MOSFETs has a fundamental thermodynamic limit in its steepness known as "Boltzmann tyranny" that restricts the minimum possible subthreshold slope to ~60 mV/dec at room temperature. In recent years, ferroelectric (FE) FETs have been experimentally demonstrated to break this limit [1]–[8]. Despite such successful demonstrations, some critical challenges need to be addressed for the FEFET to be of use to the industry. Firstly, a FE material is needed to be compatible with the existing CMOS processing technology, i.e., deposited by ALD. In addition, as FE films are known to lose its ferroelectric properties below certain critical thickness, the material to be used must possess its ferroelectricity at a thickness that would allow metal gate and gate dielectric (DE) to fit in the fin-to-fin space and gate trench. Previously, doped HfO_2 has been demonstrated to meet these criteria. However, in doped HfO_2, the required mole fraction for Si, Al, Y, Gd, La and Sr as a dopant are less than 15% to get the FE phase [9]. Such dopants can be used in the thick FE oxide-based devices but may become impractical in ultra-scaled ones.

In this work we therefore use planar n-channel FEFET fabricated by gate-last process with $Hf_{0.5}Zr_{0.5}O_2$ FE gate oxide as it is more scalable. Even though the gate stack is not optimized for steep slope operation [10], the devices show $<$ 60 mV/dec threshold under certain measurement conditions. We discuss possible mechanisms contributing to the device hysteresis, the hysteresis vs. subthreshold slope tradeoff and we report the effect of oxide thickness, lateral scaling, anneal and measurement temperatures, and bias voltage on trapping and polarization behavior [11].

Charge trapping in the gate oxide of FET originates from oxide defects and leads to various degradation effects, such as bias temperature instability (BTI) [12]. These defects can be located at any spatial position within the oxide as well as can have different ionization energies. In this extended work [11] we extract the defect energy band active in our $Hf_{0.5}Zr_{0.5}O_2$ n-channel FEFET from Non-radiative Multi-Phonon (NMP) theory using BTI-like methodology [13] below the device ferroelectric coercive voltage. Finally, we propose a simple method to separate the trapping and ferroelectric behavior in the FEFET during I_D-V_G characterization using transient-current measurements.

II. EXPERIMENTAL

The following device fabrication and electrical characterization were employed in this work.

i) Device fabrication: We used gate-last process for fabricating planar FEFETs. The high-k oxide of 3nm, 5nm and 8nm thickness has been deposited using ALD, followed by

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the deposition of 10nm TiN on top of the oxide as gate metal. Finally, to crystallize the oxide, post-metallization-annealing was done at 500^0C, 550^0C and 600^0C. The interfacial SiO_2 layer has a thickness of 0.8nm. Fabricated devices have the dimensions (width × gate length) of 10μm × 10μm, 1μm × 1μm and 1μm × 70nm. The GIXRD data shown in Fig. 1 confirm that we have properly crystallized oxide. In the 8nm HfZrO, we have ~40% of the oxide crystallized as orthorhombic phase (the rest are a mixture of other, non-polar phases), needed to induce FE behavior. Al doped HfO_2 based FET was fabricated in which the oxide did not show ferroelectric behavior. To compare the performance of FEFETs, we also fabricated other dielectric (DE) FETs of the same device dimensions with HfO_2 and SiO_2 as gate oxide. Neither of the reference HfO_2 stacks received a high-temperature anneal.

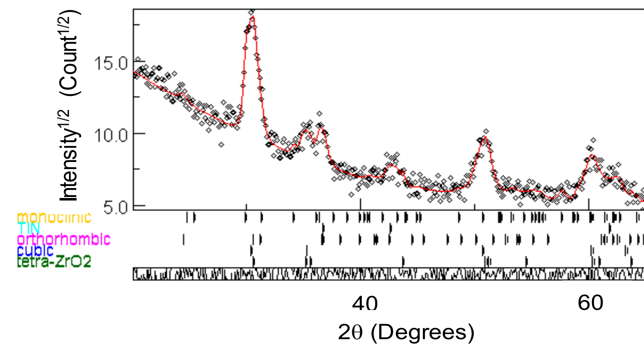

FIGURE 1. **GIXRD spectrum showing crystalline phase of 8nm $Hf_{0.5}Zr_{0.5}O_2$ annealed at 550°C.**

ii) Electrical characterization: We performed basic FEFET characterization by measuring the I_D-V_G transfer characteristics in the linear regime (drain bias $V_D = 50$ mV), sweeping gate bias V_G from either 0 to Vm or $-V_m$ to V_m and back. Different values of V_m have been used for the double sweep. For the extraction of defect energy band we used the extended Measurement-Stress-Measurement (MSM) sequence [14]. Finally, as will be discussed in detail below, we have designed a multiple-sweep *transient* I_D-V_G measurement, in which the drain current I_D is measured as a function of time after every V_G step. Analysis of the I_D transients facilitates separating trapping and ferroelectric behavior.

III. ORIGINS OF FEFET HYSTERESIS

Several phenomena are known to cause and impact the FEFET transfer characteristics, particularly its hysteresis and the corresponding threshold voltage shift ΔV_{th}.

- In response to the oxide electric field E_{ox} generated by the application of V_G, FE dipoles are reoriented along the direction of the field, or in other words, polarize the oxide. When the E_{ox} field is removed, the FE experiences a depolarization field as it is connected in series with another capacitor that arises from the Si channel [15]–[17]. In addition, presence of non-polar phase in the FE oxide creates the same effect [16].
- In addition to FE polarization, gate-oxide *charging* will typically take place during FEFET operation due to charge carriers tunneling into and out of the insulator preexisting oxide defect centers [18]. Charge trapping/detrapping at the channel side (CS) will generally result in ΔV_{th} with the opposite sign from FE polarization (Fig. 2a) as electrons are trapped during the forward V_G sweep. On the other hand, detrapping of electrons at the gate side (GS) will result in the same sense of hysteresis as FE polarization and may be therefore convoluted or confused with FE polarization switching [19], [20]. When the E_{ox} field is removed (during reverse sweep), the trapped charge can get de-trapped (Fig. 2b) [20].

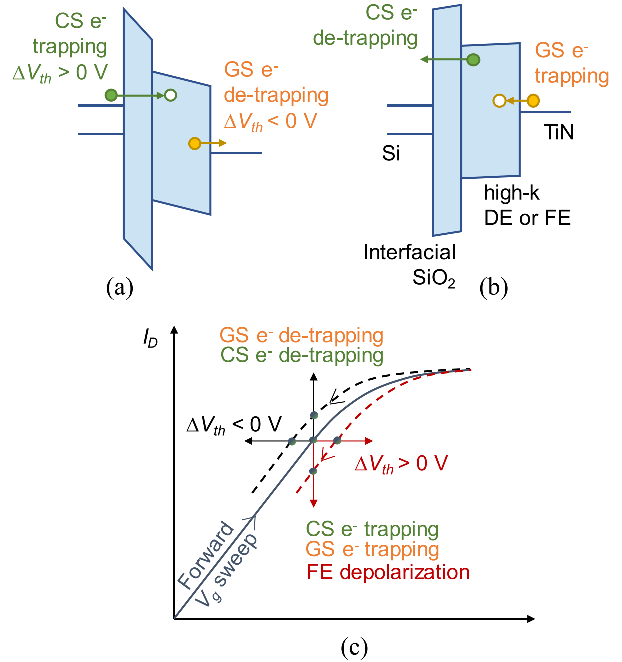

FIGURE 2. **Direction of threshold voltage shift ΔV_{th} caused by channel side (CS) and gate side (GS) trapping, detrapping and FE depolarization. At constant V_G, the effects result in change of drain current with time.**

- Apart from charge trapping, V_{th} shift may also arise from ionic motion inside the oxide [21]. This latter mechanism is not considered in this study.

The directions of hysteresis and the impact on the full n-channel FEFET double-sweep I_D-V_G characteristic are summarized in Fig. 2c.

Results and discussion: In this section we show the results obtained from the measurements and discuss the physical origin of the observations. The section is divided into three sections: basic device operation, extraction of the oxide defect bands, and the transient I_D-V_G technique.

A. BASIC DEVICE OPERATION

We start with a fresh ferroelectric FET device, the oxide of which is not woken up by any electric field cycling. Double-sweep I_D-V_G transfer characteristics of this FEFET

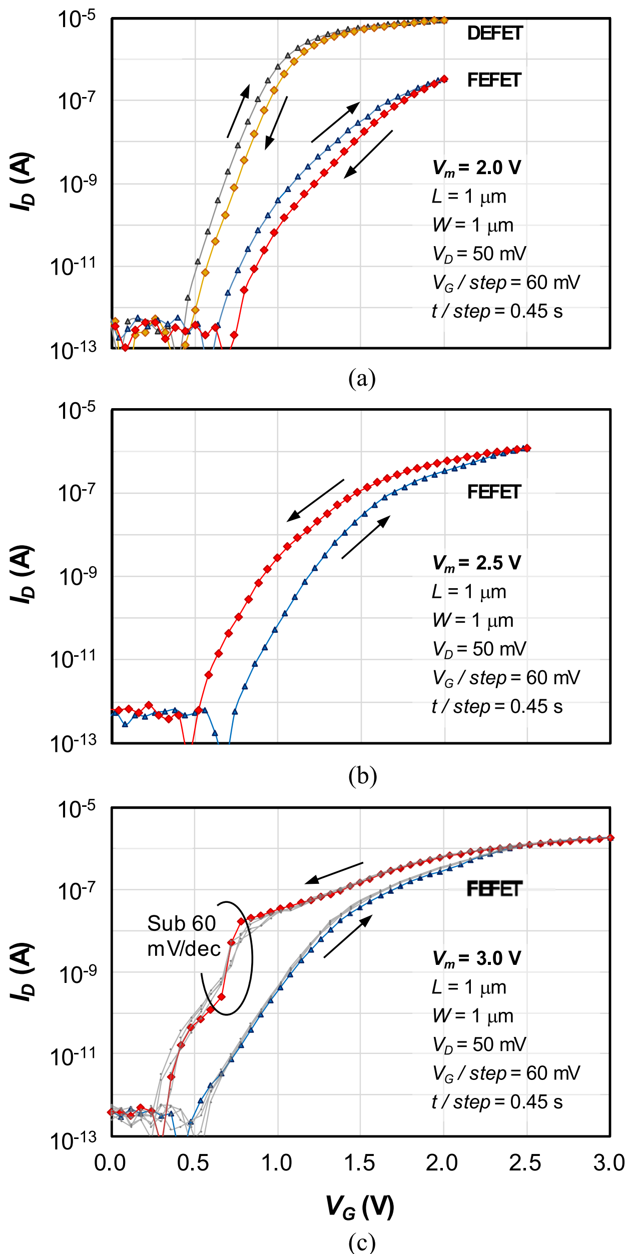

FIGURE 3. **Transfer characteristics of a HfZrO (8 nm) FEFET showing the effect of the maximum sweep value V_m. (a) At low V_m, hysteresis is likely due to CS trapping; (b) at higher V_m, hysteresis from polarization switching dominates; (c) at even higher V_m, the same hysteresis sense *with steep subthreshold slope* is observed. Stress-Induced Leakage Current (SILC) and significant degradation of the gate oxide is observed at even higher values of V_m (not shown). The results are repeatable shown by light gray lines. (a) A non-ferroelectric HfO_2 (5nm) DEFET characteristic is shown for comparison.**

from 0V to $V_m = 2.0$, 2.5, and 3.0 V are shown in Fig. 3. Hysteresis in the transfer characteristics is clockwise for $V_m = 2$ V, which is typical for CS trapping behavior (see Fig. 2). When compared against the non-ferroelectric DEFET, the ferroelectric device shows a larger threshold voltage and a poorer SS. As V_m is increased, the hysteresis changes direction. This is typically explained as a wakeup (or polarization) of the FE oxide followed by polarization switching. Once the polarization switching dominates, sub 60mV/dec slope is observed but only in the reverse trace of the V_G sweep. The results are reproducible in repeated measurements.

Since during the forward sweep the FE oxide becomes polarized, it should result in principle in sub 60mV/dec slope as well. We assume that progressive trapping of channel electrons during forward sweep causes a positive shift in V_{th}, which in turn results in poor SS [22]. During the reverse sweep, the depolarization field increases with decreasing V_G. In addition to that, CS electron de-trapping from oxide defect states takes place in the reverse trace. As a consequence, the steep SS in the reverse trace is observed.

Figure 4 shows the subthreshold slope (SS) obtained in the reverse V_G trace for different oxide thicknesses, anneal temperatures of the oxide, and for different values of V_m. It is clearly noticed that as the V_m value increases, the minimum value of SS decreases below 60 mV/dec for all reported samples.

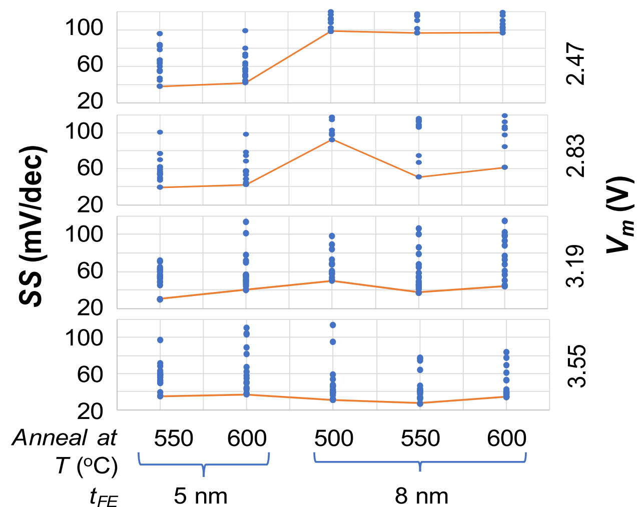

FIGURE 4. **Subthreshold slope *SS* for different oxide thicknesses, anneal temperatures, and V_m. Red lines connect the minimum values at each V_m. 3nm HfZrO does not manifest steep SS in the measured range (not shown).**

Figure 5 reports the scalability of the device—the average value of hysteresis is plotted, along with its standard deviation for different values of V_m, for different device dimensions (width × gate length). Although there is some distribution in the data, the trend clearly shows polarization switching behavior dominates over trapping behavior as V_m increases, down to $L_g = 70$ nm.

In Fig. 6 it is seen that at lower temperatures the FE behavior gets stronger. We assume that it is because fewer oxide traps are filled, as gate oxide trapping is a thermally activated process. This leads to a weaker influence of trapping phenomena over the FE behavior.

Our data also indicate a clear hysteresis vs. *SS* tradeoff, shown in Fig. 7. Specifically, we observe that the lower the SS value, the higher the hysteresis and vice versa. The link

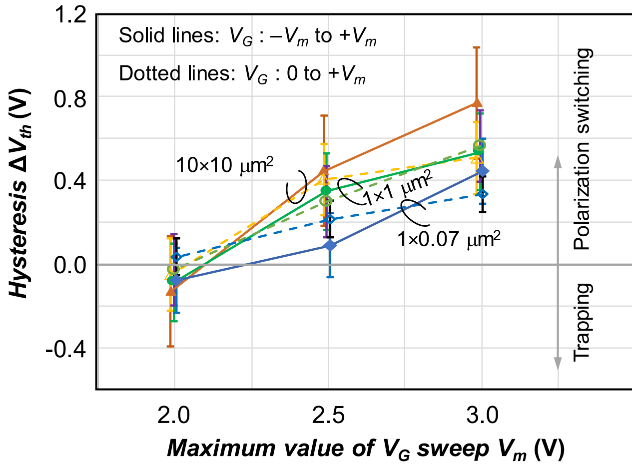

FIGURE 5. Hysteresis of FEFET for different device dimensions as a function of V_m, documenting all device dimensions show stronger FE polarization at larger V_m.

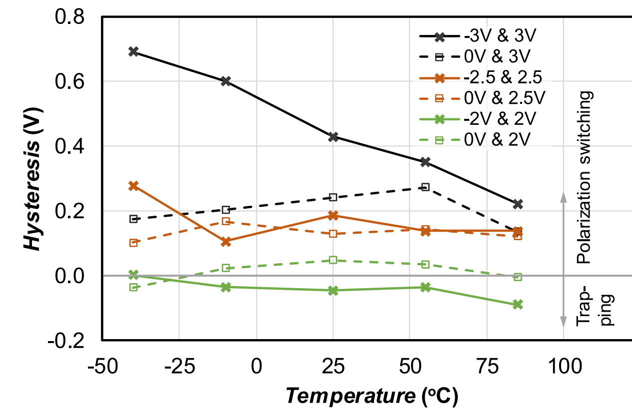

FIGURE 6. Hysteresis of FEFET for different V_G sweep ranges as a function of temperature, showing the FE polarization becomes stronger at lower temperature.

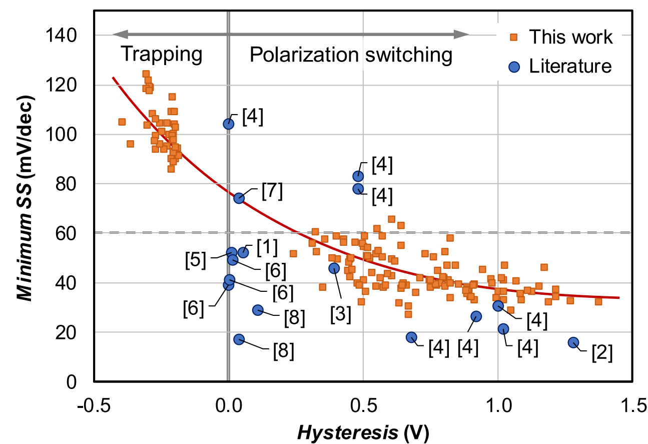

FIGURE 7. Hysteresis vs. subthreshold slope tradeoff matches well the trend observed in the literature. The line is a guide to the eye.

between SS and hysteresis could lie in V_m. We see that in order to get lower SS, higher V_m is needed. But higher V_m will result in more polarization and a higher hysteresis. We cross check this correlation against other published works by different groups and find a similar trend.

We note that, e.g., Lee *et al.* [6] showed nearly zero hysteresis with sub-60mV/dec switching; their result, however, was found to be dependent on measurement speed. It is already established that trapping is a transient phenomenon—the longer the measurement time the more trapping occurs in the oxide. Consequently, variation of measurement speed leads to a variation of the net trapped charge and a subsequent variation of the trapping component of ΔV_{th}. Note in Fig. 2 the trapping and depolarization give ΔV_{th} of opposite sign. It is therefore possible that at a right measurement speed, the two components compensate each other, giving apparently zero hysteresis. In fact, with the increase in measurement speed Lee *et al.* [6] observed larger hysteresis in counter-clockwise direction (less trapping / more depolarization).

B. EXTRACTION OF THE DEFECT BAND

Electrically active defects such as oxygen vacancies are commonly observed in high-k oxides like HfO_2, ZrO_2 and $Hf_{0.5}Zr_{0.5}O_2$ [23]. Such defects may occur due to the imperfection of the oxide material, presence of grain boundaries, or due to the polycrystalline nature. At non-zero absolute temperature defects may be present even in a perfect crystal due the thermodynamic effects. In order to characterize the active defects in our gate oxide stack, we used a measurement scheme consisting of multiple charging ("stress") and discharging ("measurement") cycles (Fig. 8), originally developed for BTI reliability testing [14]. Briefly, the "stress" phases ($V_G = V_{stress}$) with exponentially increasing durations allow to characterize the trap capture time distributions, while measuring the detrapping ("relaxion") during the "measurement" phase ($V_G = V_{meas} \sim V_{th}$) allows evaluating the trap emission time distributions. Repeating the measurement at multiple V_{stress} voltages and temperatures then enables determining the complete trap properties, including their energy distribution in the $Hf_{0.5}Zr_{0.5}O_2$ oxide band gap [13].

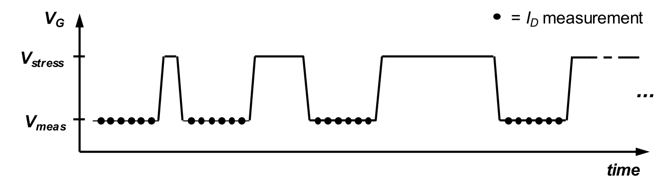

FIGURE 8. Schematic of the V_G bias sequence of trap charging ("stress") and discharging ("measurement") phases used to determine the distributions of trap properties.

Fig. 9 shows the result of this procedure at a fixed total "stress" time and at increasing stress V_G values, for a FE HfZrO FET and for a reference HfO_2 dielectric DEFET. In case of the reference DEFET, only charge trapping occurs under the application of E_{ox}. Larger E_{ox} results in more trapping and consequently, ΔV_{th} increases with the increase

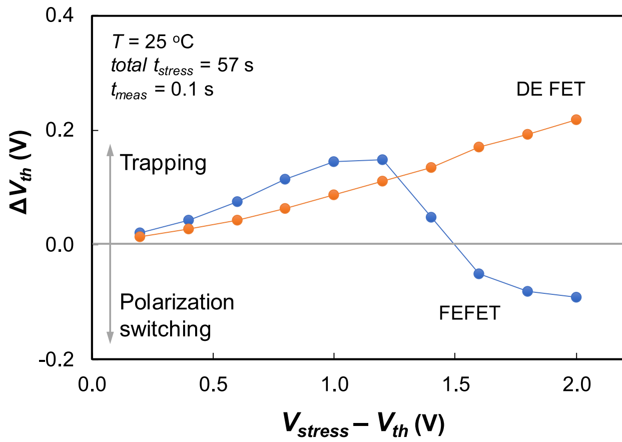

FIGURE 9. Unlike in a reference FET with dielectric (DE) HfO_2 (5 nm) oxide, the threshold voltage shift ΔV_{th} (hysteresis) in our FEFET switches sign at high V_G biases.

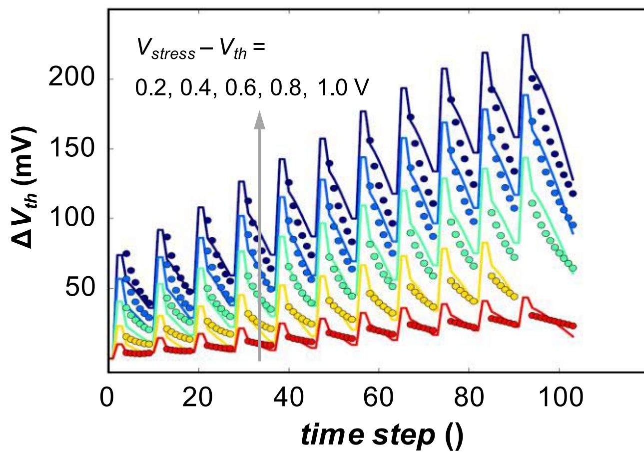

FIGURE 10. An aggregate plot of ΔV_{th} values of $Hf_{0.5}Zr_{0.5}O_2$ FEFET during measurement phases vs. time steps (symbols), fitted assuming defect bands in Fig. 11 (lines) [13].

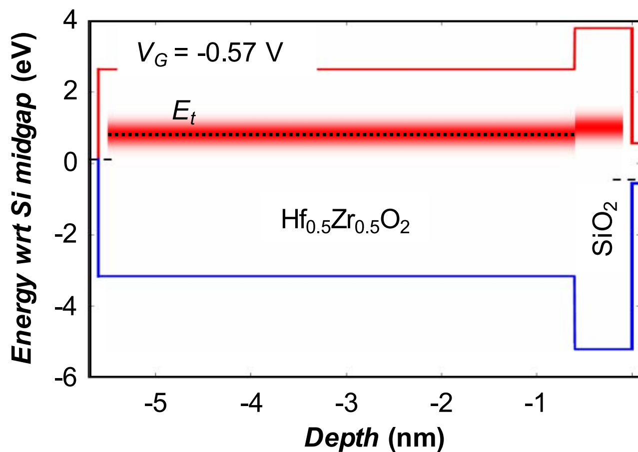

FIGURE 11. Graphical representation of extracted trap bands in FE and the interfacial SiO_2.

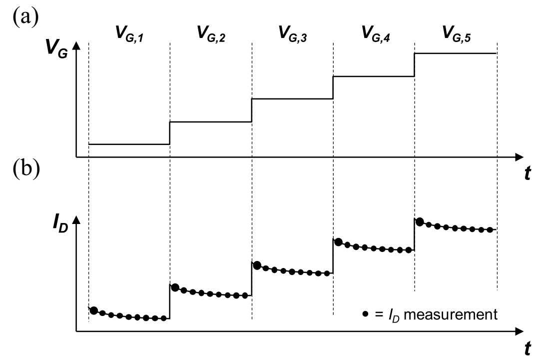

FIGURE 12. During the *transient* I_D-V_G measument, (a) V_G is stepped (forward sweep shown) as a function of time, while (b) at each bias value, multiple current measurements are done. (Each first measurement desigated by a larger symbol.)

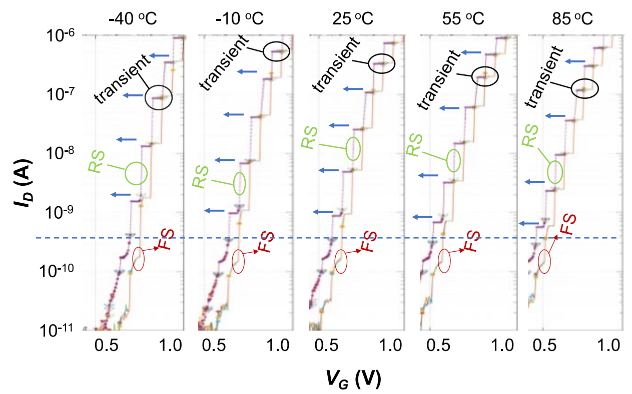

FIGURE 13. Forward- and reverse-sweep (FS and RS) *transient* I_D-V_G characteristics showing transient I_D at every V_G step measured at different temperatures on a reference FET with 5nm thick SiO_2. In the transient part, V_G is kept constant (Fig. 12). Downward triangles indicate first current measurement after each V_G step that corresponds to large symbon in Fig. 12 b. The arrows indicate the I_D transient trends during reverse sweep. Below the horizontal dotted line (sub nA current), the transients are caused by instrumentation and should be disregarded.

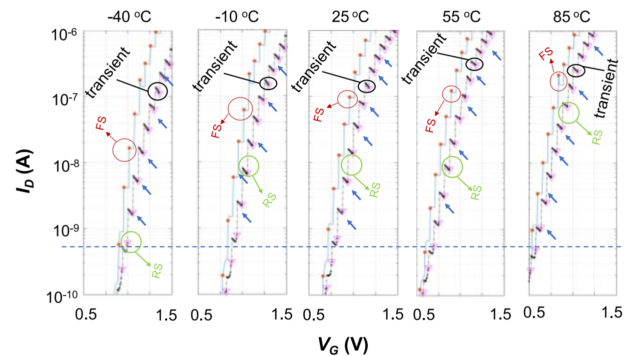

FIGURE 14. Forward- and reverse-sweep (FS and RS) *transient* I_D-V_G characteristics of a FET with 8nm thick Al-HfO_2measured at different temperatures. In the transient part, V_G is kept constant (Fig. 12). Drain current I_D always increases after every voltage down-step during reverse sweeps (indicated by the arrows) above the horizontal dotted line (sub nA current), consistent with CS detrapping. No steep slope is found in this wafer.

of V_{stress}. The same trend is observed in our FEFET at lower voltages. Above $V_{stress} - V_{th}$~1.2 V, E_{ox} is high enough for the FE oxide to start polarizing during the stress phase, resulting in negative ΔV_{th} during the measurement phase. The defect band properties in the FE oxide can therefore be extracted from the measurements at $V_{stress} - V_{th} < 1.2$ V.

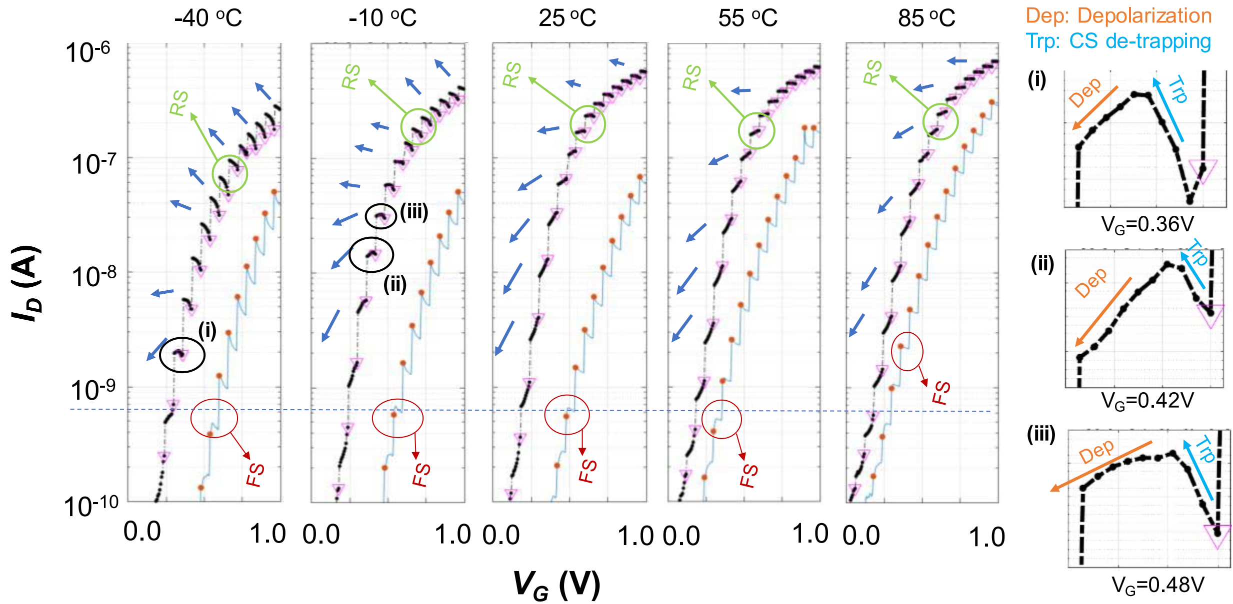

FIGURE 15. Forward- and reverse-sweep (FS and RS) *transient* I_D-V_G characteristics of a FEFET with 5nm thick HfZrO measured at different temperatures. In the transient part, V_G is kept constant (Fig. 12). Downward triangles indicate first current measurement after each V_G step that corresponds to large symbon in Fig. 12 b. s During reverse sweeps (above the horizontal dotted line indicating sub nA current) this wafer showed steep subthreshold slope. The I_D transients trend changes with the temperature (indicated by the arrows). Insets (i), (ii) and (iii) show the trend reversal of the current transient from CS detrapping to depolarization, at different current level and at two different temperatures.

TABLE 1. Parameters describing the defect band of HfZrO ferroelectric oxide.

Parameter	Value
Trap type	Acceptor
$E_{t\,(mean)}$ (w.r.t. Si midgap)	0.83 eV
$E_{t\,(sigma)}$	0.22 eV
N_t	2.6×10^{20} cm^{-3}
R	0.32
$S_{(mean)}$	1.93 eV
$S_{(sigma)}$	1.21 eV

Fig. 10 shows ΔV_{th} of $Hf_{0.5}Zr_{0.5}O_2$ FEFET during measurement phases for varying V_{stress}. The measured data are then fitted by 2-state NMP theory incorporated into our "Comphy" tool [24] to extract the defect band properties. Both CS and GS trapping are natively considered. Details of the procedure are available elsewhere [13]. The result is shown in Fig. 11.

In addition to the defect band in the HfZrO layer, a defect band in the interfacial SiO_2 is also assumed in the fit. Table 1 then summarizes the parameters describing the defect band in the HfZrO layer (see Fig. 11) active at positive V_G biases (n-channel FET operation), i.e., the traps responsible for counteracting FE polarization switching in our FEFET. We note that the defect band is relatively deep in energy (close to the Si midgap), which is in agreement with the nearly linear ΔV_{th} vs. $V_{stress} - V_{th}$ dependence in Fig. 9 [25]

C. TRANSIENT I_D-V_G MEASUREMENTS

To better understand the impact of trapping and polarization switching mechanisms on the I_D-V_G sweeps, we introduce the *transient* I_D-V_G measurement technique. Shown in Fig. 12, we measure ten I_D values at ~30 ms steps after every V_G step of the I_D-V_G sweep. Using this technique, we therefore measure *the time dependence of* I_D *after every* V_G *step*. For *visualization purposes* we then map the measured I_D values (Fig. 12b) onto the gate bias V_G axis (Fig. 12a) using time as the common variable between them. The trends in the resulting *composite* graph (upward, flat, downward, or a combination) are then compared with the standard I_D-V_G (Fig. 2) to find out which effect dominates the operating regime of the device. We next apply the *transient* I_D-V_G to SiO_2, Al-HfO_2 and HfZrO based FETs.

Figure 13 shows this *composite* plot obtained on a *SiO_2*-based FET at different temperatures. At *high* I_D / *high* V_G levels, the transient trend is always flat, as well as independent of temperature, owing to the low trap density in SiO_2. At *lower* I_D levels (~1nA to ~100nA) some upward and downward transients in the forward and reverse V_G sweeps, respectively, are observed, which we believe may be a signature of weak trapping. At the *lowest* I_D levels (~10pA to ~1nA) the transients are most likely low current measurement artefacts—they are seen in all our devices and at all measurement conditions.

In an Al-HfO_2 based FET, the I_D transient trend during reverse V_G sweep is always strongly upward (Fig. 14), consistent with CS detrapping. It is related to the fact that trap density in the high-k oxide is significantly higher as compared to that in SiO_2.

Figure 15 then shows the same measurement on a HfZrO based FEFET. At -40^0C it is seen during the reverse sweep at low V_G that the trend is again upward in the beginning (a signature of CS de-trapping). Interestingly, we observe in

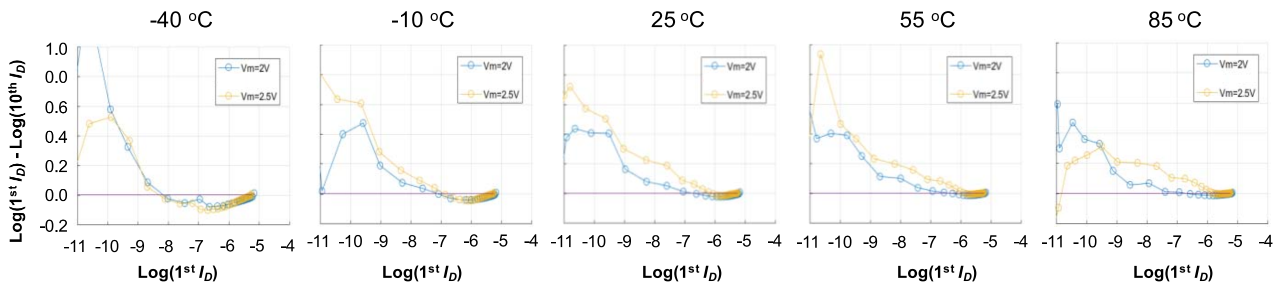

FIGURE 16. The 1st and the 10th measured I_D values are taken from the reverse sweeps of *transient* I_D-V_G measurements. The difference of their logarithms represents the direction of the transients in Fig. 11. Positive values correspond to the transients coming from polarization switching while negative values correspond to detrapping. Results are plotted for different temperatures and V_m as a function of log (I_D).

some transients that when some of the trapped charge get detrapped the trend switches its direction in the middle of the transient (inset of Fig. 15). *Hence there is an apparent competition between CS de-trapping and either GS trapping or FE depolarization.* Since we don't observe domination of GS trapping in Al-HfO_2 and we assume it is the case in HfZrO as well, we conclude the main cause must be FE depolarization. The trend reversal in the transient I_D-V_G happens at low V_G because the depolarization field increases as V_G is ramped down [15].

As temperature increases, the depolarization effect becomes visible even at higher V_G values. It is because with increasing temperature the energy barrier for polarization switching goes down, which results in a decrease of coercive field [26]. Consequently, a lower depolarization field is necessary to cause the depolarization of the polarized oxide.

In Fig. 16 we plot the transient trends during the reverse sweep of V_G by plotting difference between the logarithm of the 1st and 10th measured I_D values. The positive values thus represent downward transient (depolarization) while negative values represent trapping. The crossover point from negative to positive value represents the level of current at which the trend reversal of the transient happened in Fig. 15. Figure 16 documents that as temperature increases, depolarization gets prominent at higher current values. In addition, it shows higher values of V_m lead to increased depolarization effect. This is most visible at 85°C—the depolarization occurs up to $I_D = \sim 5 \times 10^{-8}$A for $V_m = 2$ V, while it occurs up to $I_D = \sim 10^{-6}$A for $V_m = 2.5$ V.

IV. CONCLUSION

We have reported HfZrO-based FEFETs scaled down to 70nm gate length. The devices show steep subthreshold slope in reverse V_G sweep only, along with V_{th} hysteresis. Gate oxide trapping and polarization switching greatly depends on the bias voltage range and operating temperature. Negligible effect of anneal temperature is observed. A band of active traps in the ferroelectric layer is characterized. Using our *transient* I_D-V_G measurement technique we demonstrated the competition between trapping and FE behavior taking place d*uring* I_D-V_G measurement. This measurement scheme thus facilitates understanding of mechanisms impacting the FEFET subthreshold slope.

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