On the Design of Power-Rail ESD Clamp Circuit with Consideration of Gate Leakage Current in 65-nm Low-Voltage CMOS Process

Ming-Dou Ker[1, 2], Po-Yen Chiu[2], Fu-Yi Tsai[3], and Yeong-Jar Chang[3]
[1] Dept. of Electronic Engineering, I-Shou University, Kaohsiung, Taiwan.
[2] Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan.
[3] Faraday Technology Corporation, Hsinchu, Taiwan.

***Abstract* — A new low-leakage power-rail electrostatic discharge (ESD) clamp circuit designed with the consideration of gate-leakage issue is proposed and verified in a 65-nm low-voltage CMOS process. The new proposed design has a very small leakage current of only 228 nA at 25 °C in the silicon chip. Moreover, it can achieve ESD robustness of over 8kV in human-body-model (HBM) and 750V in machine-model (MM) ESD tests, respectively.**

I. Introduction

In order to protect the internal circuits against electrostatic discharge (ESD) stresses, on-chip ESD protection circuits must be provided at all I/O and power (VDD/VSS) pads. The concept of the whole-chip ESD protection design is illustrated in Fig. 1 [1]. The power-rail ESD clamp circuit plays an important role in the whole-chip ESD protection design, because it can significantly increase the overall ESD robustness of the IC chip [1]. With the turn-on efficient power-rail ESD clamp circuit between the VDD and VSS power lines, the internal circuits of CMOS ICs can be effectively protected against ESD damages. In the traditional design, power-rail ESD clamp circuits were often realized with the RC-based ESD-detection circuit and one main ESD clamp device (as shown in Fig. 1). The power-rail ESD clamp circuit was designed to provide ESD current path between VDD and VSS during ESD stresses, and to be kept off under normal circuit operating conditions.

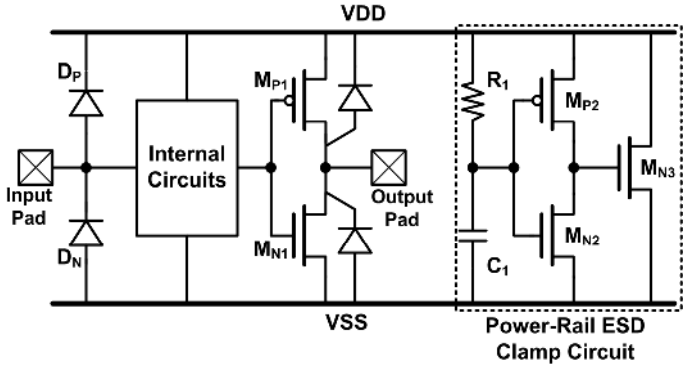

Figure 1. Typical whole-chip ESD protection scheme.

With consideration of area efficiency and fabrication cost, the capacitor in the ESD-detection circuit was often realized by the MOS capacitor, because MOS capacitors have the largest capacitance per unit area in the baseline CMOS processes. In nanoscale CMOS technology, the gate oxide thickness becomes thinner, which makes the gate-tunneling issue more significant and can not be ignored at all. The gate leakage issue had been studied and the gate-direct-tunneling current mechanism had been modeled for circuit simulation [2], [3]. With the increased gate leakage current in the nanoscale CMOS process, the traditional power-rail ESD clamp circuit with a large NMOS as capacitor in the ESD-detection circuit will cause huge leakage issue in CMOS ICs [4]. In this work, a new circuit design to effectively reduce the overall leakage current of the power-rail ESD clamp circuit is proposed and verified in a 65-nm CMOS process with the thin-gate oxide devices.

II. Impacts of Gate Leakage on Power-Rail ESD Clamp Circuit

The gate leakage in the nanoscale CMOS process causes the leakage current through the MOS capacitor, which in turn introduces more circuit leakage paths in the power-rail ESD clamp circuit. The power-rail ESD clamp circuit with the traditional RC-based ESD-detection circuit and the silicon-controlled rectifier (SCR) as main the ESD clamp device for 1-V application in a 65-nm CMOS process is shown in Fig. 2. Due to the gate leakage of the MOS capacitor, the PMOS (M_{P1}) in the ESD-detection circuit cannot be fully turned off, which causes another leakage path through the inverter in the ESD-detection circuit under normal circuit operating conditions.

If the ESD clamp device is realized by NMOS (as M_{N3} shown in Fig.1), the ESD clamp NMOS will leak more current because its gate voltage cannot be fully biased to VSS under normal circuit operating conditions. Some previous works have addressed this leakage issue, and the modified design to reduce the leakage current by adding the restorer (M_{PR}) in the ESD-detection circuit is shown in Fig. 3 [4], [5]. However, the MOS capacitor (M_{CAP}) in

the nanoscale CMOS process always has some leakage current because there is always a voltage drop on it.

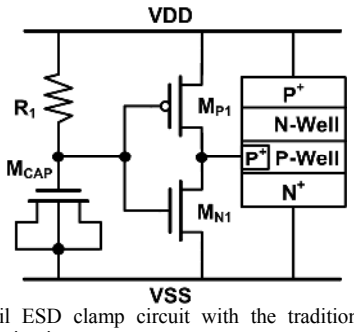

Figure 2. Power-rail ESD clamp circuit with the traditional RC-based ESD-detection circuit.

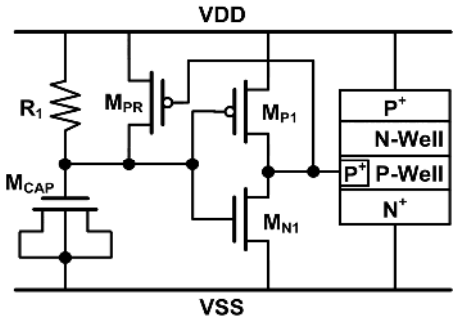

Figure 3. Modified Power-rail ESD clamp circuit with an additional restorer to reduce leakage current.

III. New Proposed Power-Rail ESD Clamp Circuit

Although some previous works can reduce the leakage current [4] or reduce required RC value [5] in the power-rail ESD clamp circuit, their ESD-detection circuits still utilize the traditional RC-based configuration. When such RC-based ESD-detection circuit was fabricated in the nanoscale low-voltage CMOS process, the MOS capacitor (M_{CAP}) in the ESD-detection circuit always conducts some leakage current due to the voltage drop across the MOS capacitor under normal circuit operating conditions.

In the BSIM4 MOSFET model [6], the gate-direct-tunneling current mechanism had been modeled. Equations of the gate-direct-tunneling current model indicate that the leakage current through the MOS capacitor can be reduced by reducing the voltage across the MOS capacitor. The new proposed design of this work is shown in Fig. 4, where the MOS capacitor (M_{CAP}) is connected between the V_A and V_B nodes. Diode-connected PMOS transistors (M_{diode}) are used to bias the node of V_B to reduce the voltage across the MOS capacitor. The static current through diode-connected PMOS (M_{diode}) transistors can be reduced by increasing their channel lengths and number of the stacked PMOS transistors. With enough diode-connected PMOS transistors stacked between VDD and VSS, the voltage across the MOS capacitor can be decreased to reduce the leakage current. In this work, the SCR is used instead of the large NMOS device as the main ESD clamp device, because SCR had been proven to have the highest ESD robustness under the smallest device size [7]. Besides, no gate-oxide structure existed in the SCR device, so the leakage current of SCR can be quite small. During ESD stresses, with the RC-delay effect from R_1 and M_{CAP}, M_{P1} is initially turned on to inject trigger current to turn on the substrate-triggered SCR. During the VDD power-on transition, the diode-connected PMOS (M_{diode}) string provides the bias voltage of ~V_{DD} to V_B (the gate terminal of the PMOS capacitor). As a result, the leakage current of M_{CAP} is effectively reduced. With the significantly reduced gate leakage current through the MOS capacitor, the potential at V_A node can be charged to VDD to fully turn off M_{P1} and to reduce the overall leakage current in this new proposed design.

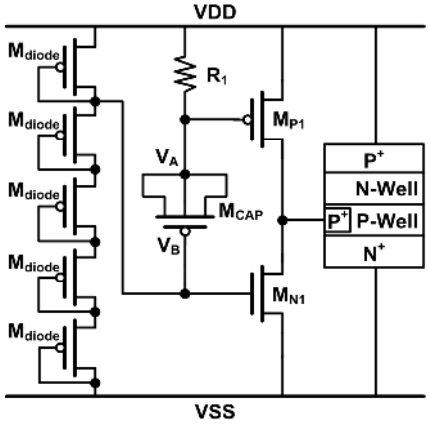

Figure 4. New proposed power-rail ESD clamp circuit with low-leakage design.

IV. Experimental Results

The new proposed power-rail ESD clamp circuit and the two traditional designs have been fabricated in a 65-nm low-voltage CMOS process. Layout pictures of three fabricated power-rail ESD clamp circuits are shown in Fig 5. Since the MOS capacitor is connected to VSS in Figs. 1 and 2, the NMOS capacitor is used in the traditional and modified power-rail ESD clamp circuits. However, the PMOS capacitor is used in the new proposed power-rail ESD clamp circuit because the MOS capacitor is not connected to VSS.

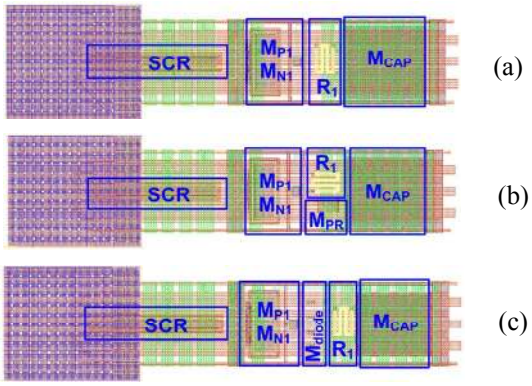

Figure 5. Layout photos among three fabricated power-rail ESD clamp circuits. (a) Tradition Design, (b) Modified Design With Restorer, and (c) New Proposed Design.

The device dimensions used in the traditional and the new proposed power-rail ESD clamp circuits are listed in Table I. Figs. 6 and 7 show the measured gate leakage currents of the PMOS and NMOS capacitors (W = 30μm, L = 25μm) with gate-oxide thickness of ~16Å in a 65-nm CMOS low-voltage process, respectively. Under 1-V bias, the gate leakage current of PMOS capacitor (NMOS capacitor) at 125 °C is as high as 22 μA (85 μA). All of the power-rail ESD clamp circuits studied in this work use the same SCR with identical device dimensions as the ESD clamp device, whose leakage current is quite small and is shown in Fig. 8. Fig. 9 shows the measured DC I-V curves of the SCR. The holding voltage (~2 V) of the SCR is larger than the supply voltage of 1 V, so it will not cause latch-up trouble in 1-V IC applications even under the high-temperature environments.

TABLE I. DEVICE DIMENSIONS IN POWER-RAIL ESD CLAMP CIRCUITS

Device Dimensions	R1 (Ω)	M_{CAP} (W/L)	M_{P1} (W/L)	M_{N1} (W/L)	M_{diode} (W/L)	SCR (WxLxM)
Traditional Design	20 kΩ	30 μm / 25 μm	100 μm / 0.15 μm	5 μm / 0.15 μm		60 μm x 3.9 μm x 2
Modified Design With Restorer	20 kΩ	30 μm / 25 μm	100μm / 0.15 μm	5 μm / 0.15 μm		60 μm x 3.9 μm x 2
New Proposed Design (This Work)	20 kΩ	30 μm / 25 μm	100μm / 0.15 μm	5 μm / 0.15μm	0.2 μm / 1 μm	60 μm x 3.9 μm x 2

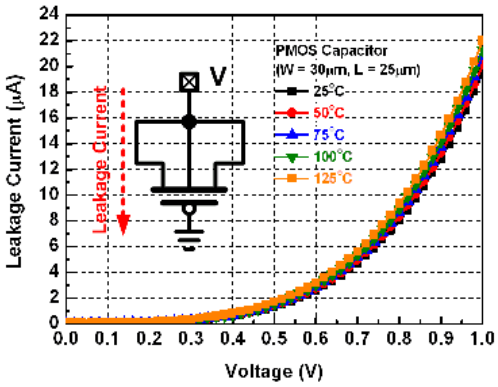

Figure 6. Measured gate leakage current of the 65-nm PMOS capacitor at different temperatures.

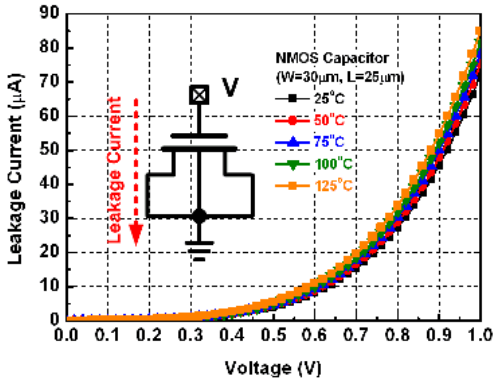

Figure 7. Measured gate leakage current of the 65-nm NMOS capacitor at different temperatures.

The leakage currents among the three fabricated power-rail ESD clamp circuits under different VDD voltages at 25 °C and 125 °C are compared in Figs. 10 and 11, respectively. The leakage currents of the power-rail ESD clamp circuits under 1-V VDD voltage are listed in Table II. Compared with the leakage current of the stand-alone MOS capacitor, much higher leakage current is observed in the traditional design, which implies that the leaky MOS capacitor causes other leakage path in the ESD-detection circuit. Although the leakage current is reduced by adding the PMOS restorer (M_{PR}) in the modified design, it is still as high as 88 μA under 1-V VDD bias at 25 °C.

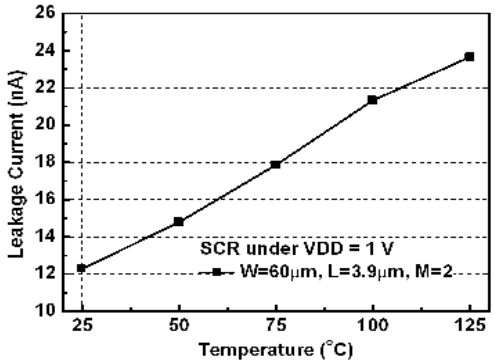

Figure 8. Measured leakage current of stand-alone SCR under 1-V bias at different temperatures, which is fabricated in a 65-nm CMOS process.

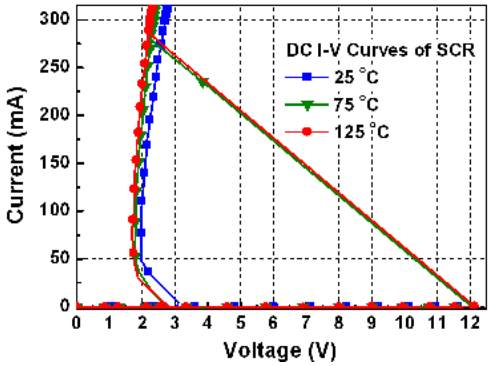

Figure 9. Measured DC I-V curves of SCR at different temperatures.

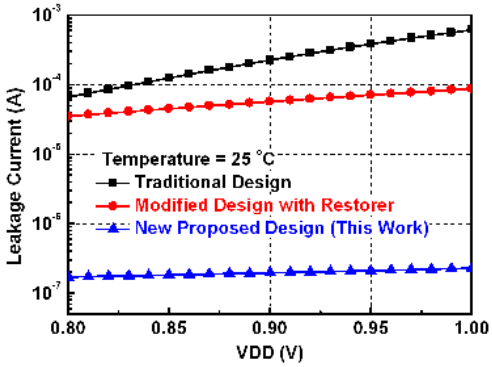

Figure 10. Comparison of leakage currents at different VDD biases among the traditional and the new proposed power-rail ESD clamp circuits at room temperature of 25 °C.

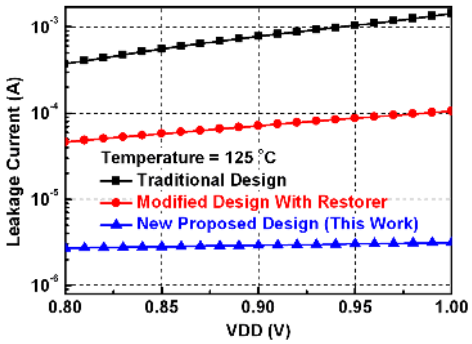

Figure 11. Comparison of leakage currents at different VDD biases among the traditional and the new proposed power-rail ESD clamp circuits at high temperature of 125 °C.

TABLE II. MEASURED LEAKAGE CURRENTS OF POWER-RAIL ESD CLAMP CIRCUITS

Leakage Current at VDD = 1V	25 °C	125 °C
Traditional Design	613 μA	1.43 mA
Modified Design With Restorer	88 μA	106 μA
New Proposed Design (This Work)	228 nA	3.14 μA

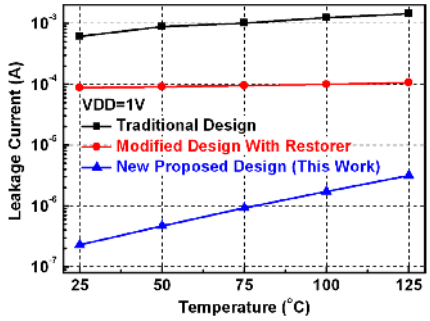

Figure 12. Comparison of leakage currents at VDD of 1 V among the traditional and the new proposed power-rail ESD clamp circuits at different temperatures.

The new proposed design (this work) has the lowest leakage current of only 228 nA (3.14 μA) at 25 °C (125 °C). The leakage currents among the three power-rail ESD clamp circuits at different temperatures are compared in Fig. 12 with VDD of 1 V. The leakage current of the new proposed design is two orders smaller than those of two traditional designs.

To verify the turn-on speed of the power-rail ESD clamp circuits, a fast rising-edge voltage pulse is applied to the VDD node to emulate the ESD-like stress. When a 5-V ESD-like voltage pulse with 2-ns rise time and 100-ns pulse width is applied to VDD, it is rapidly clamped to around 2 V within 5 ns, as shown in Fig. 13. Thus, the internal circuits can be well protected by the new proposed power-rail ESD clamp circuit. With a holding of ~2 V, the SCR did not cause latch-up trouble for 1-V IC applications. The human-body-model (HBM) and machine-model (MM) ESD robustness among these three designs are listed in Table III. The new proposed design has the highest ESD level of over 8 kV in HBM and 750 V in MM, respectively.

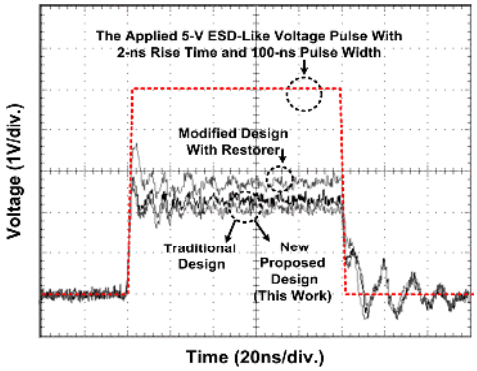

Figure 13. Comparison of the turn-on efficiency among the three power-rail ESD clamp circuits under the applied 5-V voltage pulse with a rise time of 2 ns and a pulse width of 100 ns.

TABLE III. HBM AND MM ESD ROBUSTNESS OF POWER-RAIL ESD CLAMP CIRCUITS

ESD Robustness	HBM	MM
Traditional Design	6 kV	600 V
Modified Design With Restorer	> 8 kV	750 V
New Proposed Design (This Work)	> 8 kV	750 V

V. CONCLUSION

A new power-rail ESD clamp circuit designed with the consideration of gate-leakage issue has been proposed and successfully verified in a 65-nm low-voltage CMOS process. With very low leakage current and high ESD robustness, the proposed power-rail ESD clamp circuit is very suitable for whole-chip ESD protection design in CMOS ICs realized with only low-voltage devices in advanced nanoscale CMOS processes.

REFERENCES

[1] M.-D. Ker, "Whole-chip ESD protection design with efficient VDD-to-VSS ESD clamp circuit for submicron CMOS VLSI," *IEEE Trans. Electron Devices*, vol. 46, no.1, pp. 173-183, Jan. 1999.

[2] K.-M. Cao, W.-C. Lee, W. Liu, X. Jin, P. Su, S.-K. Fung, J.-X. An, B. Yu, and C. Hu, "BSIM4 gate leakage model including source-drain partition," in *IEDM Tech. Dig.*, 2000, pp. 815-818.

[3] W.-C. Lee and C. Hu, "Modeling CMOS tunneling currents through ultrathin gate oxide due to conduction- and valence-band electron tunneling," *IEEE Trans. Electron Devices*, vol. 48, no. 7, pp. 1366-1373, Jul. 2001.

[4] S. Poon and T. Maloney, "New considerations for MOSFET power clamps," in *Proc. EOS/ESD Symp.*, 2002, pp. 1-5.

[5] J. Smith, R. Cline, and G. Boselli, "A low leakage low cost PMOS-based power supply clamp with active feedback for ESD protection in 65-nm CMOS technologies," in *Proc. EOS/ESD Symp.*, 2005, pp. 298-306.

[6] M. Dunga, W.-W. Yang, X.-M. Xi, J. He, W.-D. Liu, K.-M. Cao, X.-D. Jin, J. Ou, M.-S. Chan, A. Niknejad, and C. Hu, *BSIM4v6.1 MOSFET Model Users' Manual*.

[7] M.-D. Ker and K.-C. Hsu, "Overview of on-chip electrostatic discharge protection design with SCR-based devices in CMOS integrated circuits," *IEEE Trans. Device and Materials Reliability*, vol. 5, no. 2, pp. 235-249, Jun. 2005.