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On the fault tolerance of a clustered single-electron neural network for differential enhancement

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Abstract: A clustered neural network, in which neuronal information is represented by a cluster (population of neurons), rather than a single neuron, is a possible solution to construct fault-tolerant single-electron circuits. We designed single-electron circuits based on a clustered neural network that performs differential enhancement where differences between the cluster's outputs receiving various magnitudes of inputs are enhanced after the processing. Simulation results showed that the degradation of the performance of the clustered single-electron neural network was significantly lower than that of a non-clustered network, which indicates that this approach is one possible way to construct fault-tolerant computing systems on nanodevices.

Keywords: single-electron circuit, neural network, fault tolerance

Classification: Electron devices

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1 Introduction

The development of systems that imitate the behavior of living neural networks opens a promising area of research in nanoelectronics. To proceed toward this goal, we propose a clustered neural network with a single-electron circuit. Such a network circuit will have a fault- and noise-tolerant operation.

The single-electron device is a nanometer-scale device whose behavior is based on quantum effects such as the Coulomb blockade and electron tunneling. Temperature of operation, electrical noise, as well as random device failure due to background charge effects are key issues that influence the reliability of such nanodevices.

A competitive neural network that exhibits the winners-share-all (WSA) solution, in which a cluster of neurons remain activated in steady states, is particularly useful for enhancing differences between noisy inputs, owing to collective competition among the clusters. The performance will be improved significantly when a single neuron is built based on a fault-tolerant architecture [2]. In this report, we incorporate single-electron circuits with a fault-tolerant WSA neural network, and examine the tolerance for the device failure.

2 Fault-tolerant circuit architecture

The fault-tolerant architecture consists of four layers in which data is strictly processed in a feed-forward manner (Fig. 1 (a)). The first layer is denoted as the input layer. The core operation is performed in the second layer, which consists of a cluster of identical redundant units implementing the desired Boolean logic function. The fault immunity increases as the number of redundant units increases, yet the operation is quite different from the classical majority-based redundancy. The third layer receives the outputs of the redundant logic units in the second layer, creating a weighted averaging with rescaling. Finally, the fourth layer is the decision layer where a binary output value is extracted using a simple threshold function. By using this architecture, the circuit can operate correctly under high error density in logic elements [2].

In this paper, we report on a spiking neuron circuit that uses single-electron circuits we designed based on this architecture. The details are explained in the following section.

3 Competitive neural network with single robust neuron circuits

Our single-electron spiking-neuron circuit operating with the fault-tolerant architecture is shown in Fig. 1 (b). This circuit, named "single robust neuron (SRN)," consists of three layers according to the fault-tolerant architecture. The first layer is denoted as an input layer. In this neuron circuit, the input signal is a periodic spiking signal. The second layer is a spiking neuron layer consisting of a cluster of identical redundant single-electron spiking-neuron circuits. The circuit consists of five single-electron nonlinear oscillators that

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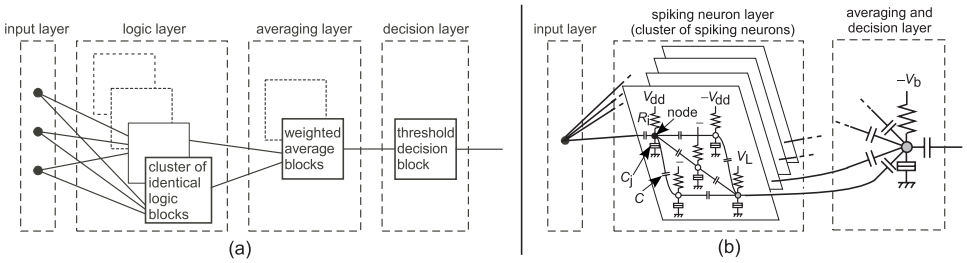

Fig. 1. (a) Fault-tolerant architecture based on multiple layers [2]. (b) Single robust neuron based on fault-tolerant architecture. In the second layer, cluster of single-electron spiking-neuron circuits are used instead of logic circuits.

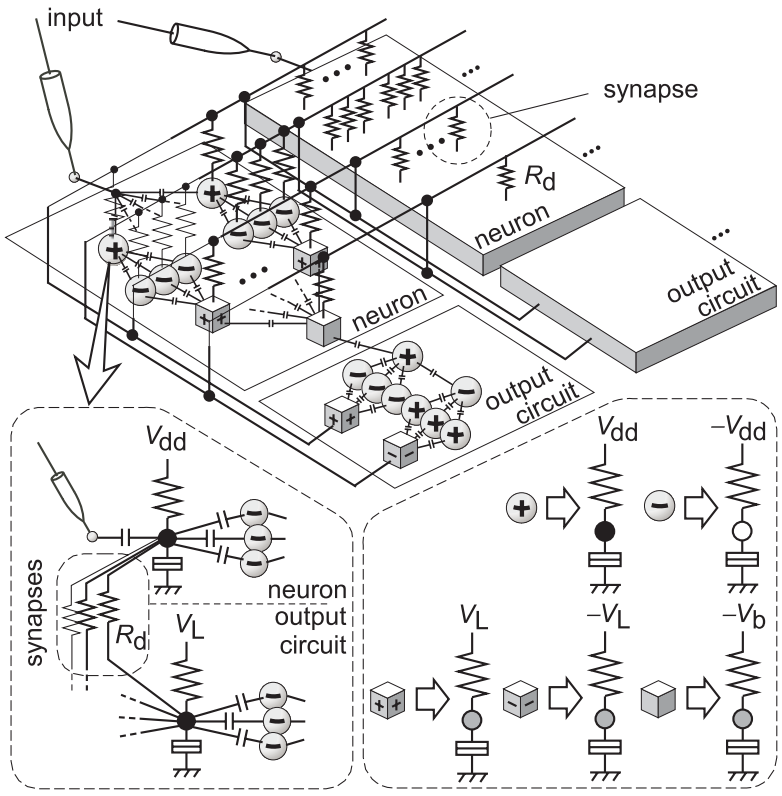

Fig. 2. Competitive neural network with single robust neuron. Each neuron is connected with output circuits and input terminals. Each oscillator that is biased by $+V_{\mathrm{L}}$ (or $-V_{\mathrm{L}}$) in output circuit is connected with every other oscillator in neurons by R_{d}.

mimic the generation of an action potential in a living neuron and that guarantee correct direction of data flow [3]. The nonlinear oscillator consists of a tunneling-junction (C_{j}) and resistance (R_{i}) of a large value connected in a series to a common node and biased by the voltage source ($\pm V_{\mathrm{dd}}$). The oscillator produces a nonlinear voltage oscillation that is caused by electron tunnelings at low temperatures. This is when the Coulomb-blockade effect

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occurs [4]. The electron tunneling phenomenon is defined as a spike. In the spiking-neuron circuit, the oscillators are connected with coupling capacitors (C). The polarity of V_{dd} is set opposite to that of neighboring nodes to transmit spikes, and the magnitude of the bias voltage on the output element (V_L) is set lower than V_{dd} to guarantee correct spike flow [3]. The third layer is an averaging and decision layer where a single-electron oscillator is operating. The oscillator is biased by $-V_b$ and produces an output spike when it receives some input spikes from the second layer. The actual threshold value that dictates the firing of a spike is dependent on the oscillator bias voltage $-V_b$, which relates to the number of required simultaneous input spikes.

We designed a competitive spiking neural network that uses the SRN as shown in Fig. 2. In this network, the SRN is connected with an output circuit and input terminal. The output circuit connects with each single-electron oscillator that is in the neuron through a coupling resistance (R_d). When the spike travels from the input to the output through the neuron, a difference in electric potential is generated at both terminals of R_d. Consequently, a current flows through R_d until the voltage difference vanishes. Therefore, R_d performs the role of an inhibitory synapse. As long as the synaptic current flows, the magnitude of the node voltage of the oscillator in the neuron decreases, making it hard for any electron to tunnel through the oscillator.

4 Simulation results

Extensive computer simulations using a modified Monte Carlo method were carried out to validate the circuits we described (See the Appendix in [5]). The results of SRN's operations are shown in Fig. 3 (a), where R is the redundancy factor that indicates the number of identical spiking-neuron circuits in the spiking-neuron layer of the SRN. The probability of correct operation is defined as the proportion of correct output spikes over the total number of input spikes. Random circuit failures were applied to the neuron causing local disruption of correct behavior. The probability of correct operation, or the success rate, was observed for a sweep of various probabilities of error occurrences. Also the impact of increased redundancy was determined.

Clearly, the original spiking-neuron circuit that had been initially built with no consideration for fault-tolerance (Fig. 3 (a), solid line) shows a larger failure rate as error densities increase. However, a redundancy factor of seven to nine allows absorbing a significant error density of up to 30% (0.3) with unaffected circuit behavior.

A competitive neural network of 100 cross-connected neurons was simulated. Excitatory input spike frequencies are provided in linearly decreased ranking. The task of the network is to enhance the difference between the inputs [1]. The similarity rate as a function of the applied error density for the neural networks is shown in Fig. 3 (b). The original neural network where the fault-tolerant architecture is not applied does not operate properly under an error density of more than 0.05. A moderate value of R allows absorbing

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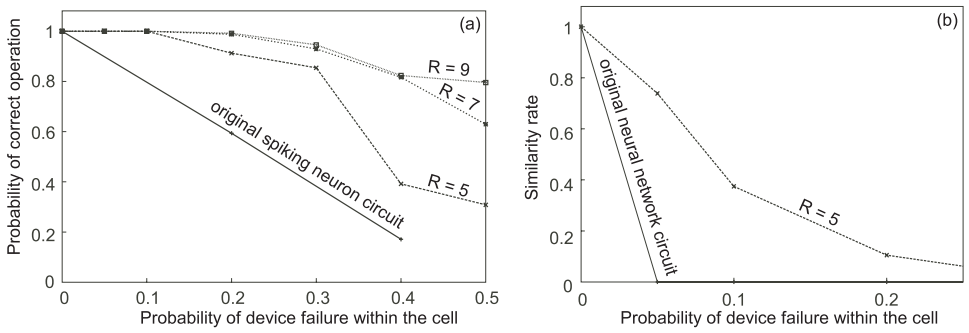

Fig. 3. Simulation results. (a) The probability of correct operation as a function of the probability of device failure in the SRN ($R = 5$, 7, and 9) and original spiking-neuron circuit (with no fault immunity). (b) the similarity rate as a function of the probability of device failure in the network with the SRN ($R = 5$) and original spiking-neuron circuit.

a higher level of error densities, as shown in Fig. 3 (b) for $R = 5$. Thus, we have provided evidence that determining circuit-level fault-tolerant architectural design improves the error immunity of single-electron artificial neural networks.

5 Conclusion

A fault-tolerant winners-share-all (WSA) neural network was implemented with noisy single-electron devices to demonstrate its redundancy in a differential enhancement task. We showed that the performances of both neurons and networks were significantly improved when the redundancy factor $(R) > 5$.

Where does the redundancy come from? From neurons or a network, or both? Our results clearly showed that single robust neurons produced a part of the redundancy in the network (Fig. 3). If the redundancy results from both neurons and a network structure with WSA solutions, we should define the number of winners (W) to evaluate the redundancy. When $W = 1$ (conventional winner-takes-all case), a network-level redundancy will not be produced because such a sole winner will be strongly affected by external noises [1]. As W increases, the redundancy increases because a cluster of neurons represents the winner and the responsibility of each neuron decreases. Examining these properties is another subject altogether. However, our future work should involve finding an appropriate value of R (e.g., $R = 5$ from Fig. 3) and re-simulating the WSA network with $R = 5$ and $W = 1, 2, \ldots M$, until the similarity rate saturates. With the results thus obtained, one can clearly observe that both the neurons and network produce the redundancy.

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