# On the Performance of Single-Gated Ultrathin-Body SOI Schottky-Barrier MOSFETs

Joachim Knoch, Min Zhang, Siegfried Mantl, *Member, IEEE*, and J. Appenzeller, *Senior Member, IEEE*

***Abstract*—The authors study the dependence of the performance of silicon-on-insulator (SOI) Schottky-barrier (SB) MOSFETs on the SOI body thickness and show a performance improvement for decreasing SOI thickness. The inverse subthreshold slopes $S$ extracted from the experiments are compared with simulations and an analytical approximation. Excellent agreement between experiment, simulation, and analytical approximation is found, which shows that $S$ scales approximately as the square root of the gate oxide and the SOI thickness. In addition, the authors study the impact of the SOI thickness on the variation of the threshold voltage $V_{\rm th}$ of SOI SB-MOSFETs and find a nonmonotonic behavior of $V_{\rm th}$. The results show that to avoid large threshold voltage variations and achieve high-performance devices, the gate oxide thickness should be as small as possible, and the SOI thickness should be $\sim$ 3 nm.**

***Index Terms*—Carrier injection, Schottky-barrier MOSFET, threshold voltage shift, ultrathin body SOI.**

## I. Introduction

SCHOTTKY-BARRIER (SB) MOSFETs have recently attracted a renewed interest as an alternative to conventional MOSFETs with doped source and drain contacts [1]–[4]. However, SB-MOSFETs still show an inferior performance if compared with conventional MOSFETs due to the presence of SB at the contact–channel interfaces that reduce the carrier injection into the channel. It is therefore desirable to either achieve SB as low as possible or render the tunneling probability through the barrier as high as possible to realize high-performance SB-MOSFETs. On the other hand, it has been pointed out that negative SB would be needed to obtain the same ON-state performance as a conventional MOSFET [5], [6]. SB to date, however, are positive and exhibit values of, e.g., 0.28 eV for erbium silicide or larger for electron injection [4]. Hence, increasing the carrier injection is indispensable to improve the SB-MOSFET performance. With a simulation study, we were recently able to show that in silicon-on-insulator (SOI) SB-MOSFETs, the tunneling probability through the SB increases with decreasing SOI thickness, allowing for an excellent electrical performance with steep inverse subthreshold slopes $S$ and high transconductances [5], [6]. Here, we will show this performance improvement in an experimental study. To this end, we fabricated a number of SB-MOSFET devices with varying SOI thickness and nickel-silicided source/drain electrodes. The experimental results will be compared with quantum simulations of a fully depleted SOI SB-MOSFET based on the nonequilibrium Green's function formalism [7]. It will be shown that the experimentally found improvement with decreasing SOI thickness can be very well reproduced with our simulations and is indeed a consequence of the improved carrier injection in SOI SB-MOSFETs. An approximation of the tunneling probability through the SB allows to set up an analytical expression of the dependence of the inverse subthreshold slope on the SOI thickness $d_{\rm soi}$. This expression shows that $S$ scales as $\sqrt{d_{\rm soi}}$, suggesting that strong improvements of the switching behavior are accessible in case of ultrathin-body (UTB) SOI. However, despite a significant performance improvement, the use of UTB SOI leads to a shift of the threshold voltage $V_{\rm th}$ [8], [9]. Here, we investigate this $V_{\rm th}$ shift in SOI SB-MOSFETs and show that they exhibit a nonmonotonic dependence of the threshold voltage on the SOI thickness with a minimum $V_{\rm th}$ for $d_{\rm soi}$ in the range of 2–4 nm. An analytical expression for the threshold voltage is given, which allows setting up design rules on how to optimize the performance and minimize the threshold voltage shift of single-gated SOI SB-MOSFETs.

## II. Experiment

SB-MOSFETs with fully nickel-silicided source/drain electrodes were fabricated on SOI wafers with a p-type doping of $1 \times 10^{15}$ cm$^{-3}$ of varying thickness. A cycle of dry/wet thermal oxidation and HF stripping was used to thin down the wafers to the desired thickness. After mesa isolation, an $\sim$ 3.5-nm-thick gate oxide was grown by low-temperature wet thermal oxidation [10] followed by the deposition of a 200-nm n-type polysilicon. Subsequently, the gate is patterned and spacers are formed. The last steps include nickel deposition, silicidation at 500 °C for 20 s, and removal of superficial nickel. Only long-channel devices with a channel length of $L = 2$ $\mu$m are fabricated to avoid any influence of short-channel effects. The inset in Fig. 1 shows a transmission electron microscopy (TEM) image of the source area of a readily fabricated device on a 25-nm-thick SOI. One clearly sees the encroachment of the nickel silicide underneath the gate, which ensures that there is no gap between the silicided source and the source-side edge of the gate such that the gate has a good electrostatic control of the SB at the silicide–silicon interface. The main panel of Fig. 1 shows typical transfer characteristics of three devices

Manuscript received December 28, 2005; revised April 13, 2006. The review of this paper was arranged by Editor V. R. Rao.

J. Knoch, M. Zhang, and S. Mantl are with the Institute of Thin Films and Interfaces, ISG1-IT, and The Center of Nanoelectronic Systems for Information Technology, 52454 Jülich, Germany (e-mail: j.knoch@fz-juelich.de).

J. Appenzeller is with the IBM T. J. Watson Research Center, Yorktown Heights, NY 10598 USA.

Digital Object Identifier 10.1109/TED.2006.877262

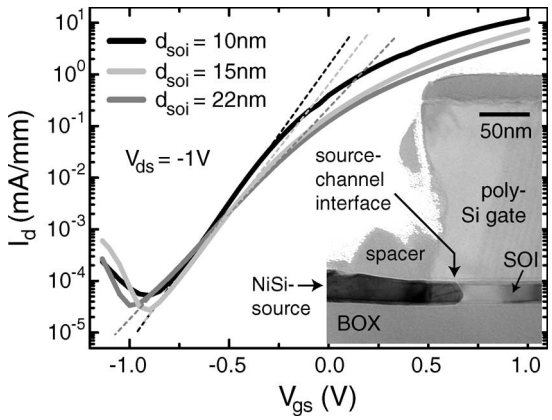


Fig. 1. Transfer characteristics of SOI SB-MOSFETs with $d_{\rm soi} = 10$, 15, and 22 nm at $V_{\rm ds} = -1$ V. The inverse subthreshold slope is extracted from the electron branch as indicated by the dashed lines. The inset shows a TEM image of the contact area of a fabricated device with NiSi source/drain electrodes.

with different SOI body thicknesses of 10, 15, and 22 nm, respectively. It is apparent that the inverse subthreshold slope as well as the on-current of the devices are improved for decreasing SOI thickness. As will become clear below, the improvement seen experimentally is exactly what is expected from simulations (see [5], [6]), proving that the use of UTB SOI allows improving the carrier injection through the SB in SB-MOSFETs.

## III. $S$ Dependence on the SOI Thickness—Comparison of the Experiment and Theory

Decreasing the SOI thickness improves both the switching behavior and the on-current of SOI SB-MOSFETs (cf. Fig. 1). However, to study the effect of varying SOI body thickness on the performance of SOI SB-MOSFETs in more detail, the ON-state does not provide an appropriate measure due to its sensitivity to process-induced fluctuations of the SB height and to the parasitic source/drain resistances.[1] On the other hand, for typical SB heights (such as 0.28 eV for erbium silicide [4], 0.24 eV for PtSi [3], or 0.64 eV for NiSi), two inverse subthreshold slopes can be found in the OFF-state characteristics of SB-MOSFETs for small $V_{\rm ds}$ [3], [5], [6]; if the bulk potential in the channel is larger than the SB, the current is determined by thermionic emission alone, and an ideal inverse subthreshold slope can be expected in an electrostatically well-tempered device. Once the gate voltage pushes the conduction band (in case of an n-type SB-MOSFET) below the SB, the OFF-state current is determined by a thermionic and a tunneling part, i.e., $I_{\rm th}$ and $I_T$, respectively. However, for feasible experimental SB heights, the thermionic fraction $I_{\rm th}$ is rather small, and the OFF-state is mainly determined by the tunneling component of $I_d$. In particular, if UTB SOI is employed as required for ultimately scaled transistor devices, the effective SB is increased as will be discussed below. Hence, $S = (((\partial I_{\rm th}/\partial V_{\rm gs}) + (\partial I_T/\partial V_{\rm gs}))(1/(I_{\rm th} + I_T)))^{-1} \approx ((\partial I_T/\partial V_{\rm gs})(1/I_T))^{-1}$, and therefore, the inverse subthreshold slope is insensitive to process-induced fluctuations and therefore is taken as the relevant figure-of-merit here, representing a robust measure to quantify the impact of varying SOI thickness. This is confirmed by simulations and by the fact that different experimental devices with the same $d_{\rm soi}$ and $d_{\rm ox}$ exhibit a different ON-state current but the same value for $S$. In the present study, the high barrier of nickel silicide allows an unambiguous determination of the impact of $d_{\rm soi}$ and $d_{\rm ox}$ on the performance of SOI SB-MOSFETs.

[1]In Fig. 1, we chose representative examples of transfer characteristics to demonstrate the improvement of the ON-state gained when decreasing the SOI thickness. However, devices with an SOI thickness of 8 nm exhibit a lower ON-current, owing to increased parasitic source/drain resistances when silicided 8-nm SOI.

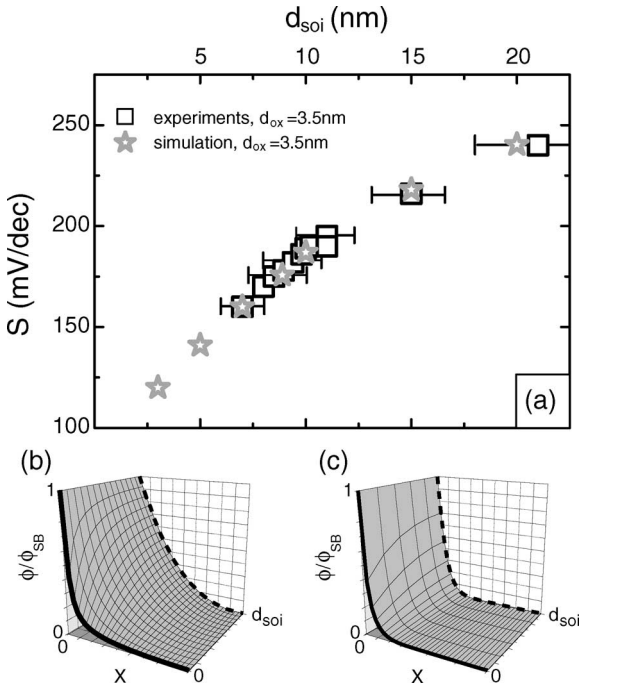


Fig. 2. (a) $S$ versus SOI thickness extracted from experimental devices (black hollow squares) and simulations (gray stars); in all cases, $d_{\rm ox} = 3.5$ nm. Both sets of data are in excellent agreement. Two-dimensional potential profiles of the source Schottky diode for (b) thick and (c) thin $d_{\rm soi}$.

To be specific, the inverse subthreshold slope $S$ of the electron branch (as indicated by the dashed lines in Fig. 1) is extracted from the measured data. A range of SOI thicknesses between 7 and 22 nm have been realized on several sample chips. Since the exact SOI thickness is not known for each individual device, we first confirmed for a few samples that $S$ increases with increasing SOI thickness by determining $d_{\rm soi}$ with cross-sectional TEM images. Then, to get a functional dependence of $S(d_{\rm soi})$, we measured a large number (40–60 devices) of transistors on each sample chip and extracted the corresponding $S$ values. We then correlate the frequency of the appearance of $S$ values with the frequency of the appearance of SOI thicknesses (for each sample chip separately) extracted from an ellipsometer mapping of the samples taken prior to the fabrication process. Because a change in $d_{\rm soi}$ is the only device-to-device variation that influences $S$, the correlation allows to associate a certain SOI thickness with a certain value of $S$.

The result of the extraction of $S$ from the measurements as described above is shown in Fig. 2(a) (black hollow squares).

In the present case, all devices have a gate oxide thickness of $d_{\rm ox} = 3.5$ nm. It can be seen that the experimental data show a strong dependence of the inverse subthreshold slope on the SOI thickness. In particular, the inverse subthreshold slope decreases with decreasing $d_{\rm soi}$, leading to a significant performance improvement in terms of the switching behavior of the devices. The reason for this improvement is an increased carrier injection through the SB. This means that the SB can be made thinner by decreasing $d_{\rm soi}$ without doping the semiconductor in contact with the metal electrode. Note that an improvement of $S$, i.e., a larger carrier injection, also implies an improvement of the ON-state current as was already mentioned above. This is a very important point because the ON-state performance of SB-MOSFET is always determined by the SB (unless negative SB are feasible), and it is therefore always necessary to increase the carrier injection to improve the SB-MOSFET performance.

Next, we compare the experimental data with quantum simulations based on a one-dimensional model of a fully depleted SOI SB-MOSFET. This comparison will allow to qualify the model in use and, in turn, enables to set up an analytical expression for the dependence of $S$ on $d_{\rm soi}$, which facilitates predictions on how to design an SB-MOSFET properly.

The one-dimensional model is based on a modified Poisson equation [11] that has been successfully used to explore the electrical characteristics of conventional SOI MOSFETs [12]–[15]. This Poisson equation is used together with the nonequilibrium Green's function formalism to self-consistently determine the charge in and current through the SB-MOSFET [7], [16]. If the buried oxide thickness is large, the modified Poisson equation for the surface potential $\Phi_f(x)$ is as follows:

$$\frac{d^2\Phi_f(x)}{dx^2} - \frac{\Phi_f(x) - (\Phi_g + \Phi_{\rm bi})}{\lambda^2} = \frac{q^2\rho(x)\eta}{\varepsilon_{\rm si}} \qquad (1)$$

with $\lambda = \sqrt{(\varepsilon_{\rm si}/\eta\varepsilon_{\rm ox})d_{\rm soi}d_{\rm ox}}$ being the relevant length scale on which potential variations are screened. $\rho$ includes the density of mobile charge as well as a constant charge background due to doping. $\Phi_{\rm bi}$ is the built-in potential, and $\eta$ is a parameter that accounts for the nonuniformity of the lateral field across the SOI thickness [17]. It usually varies between 1.0 and 1.3; in the following, we set $\eta = 1.3$. Recently, we were able to show that (1) describes well the electrostatics of fully depleted SOI SB-MOSFETs if $d_{\rm soi}/\lambda \leq 1.5$ [18]. The effect of an energetic separation $\Delta E$ of the first subband due to vertical quantization is taken into account in the simulations as well. For simplicity, we consider $\Delta E$ as arising from the confinement of carriers within a hard-wall potential, which, in a low-doped SOI film, is a good approximation in the device's OFF-state [19]. In addition, the electric quantum limit is assumed with the first subband contributing most to the current; higher subbands are accounted for by a numerical factor $M_s$ as in [20]. Finally, ballistic transport is assumed, which, however, has no significant effect on the OFF-state of the device.

Inspecting (1), it already becomes apparent that the use of UTB allows to improve the device characteristics. Since in the OFF-state the density of mobile charge is small, $\rho \approx$ const. and (1) can be solved analytically, leading to an exponential screening of the SB on the length scale $\lambda$. This means that the barriers can be made thin, i.e., the tunneling probability can be made large if $d_{\rm soi}$ and $d_{\rm ox}$ are made as small as possible. Fig. 2 shows two-dimensional potential profiles of the source SB for the same gate oxide thickness but with a large $d_{\rm soi}$ [Fig. 2(b)] and a small $d_{\rm soi}$ [Fig. 2(c)]. Here, the black straight lines are the surface potential, whereas the dashed lines belong to the potential profile at the interface between channel and buried oxide. It is apparent that in case of a small body thickness [Fig. 2(c)], the SB becomes thinner, and hence, the tunneling probability is increased as has been discussed above.

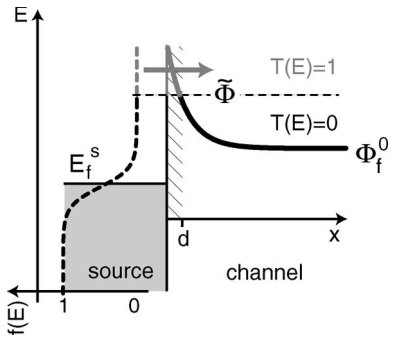


Fig. 3. Potential distribution at the source Schottky diode. For the analytical approximation, the tunneling probability $(T(E)) = 1$ for energies above $\tilde{\Phi}$ and zero otherwise. $\Phi_{\rm f}^0$ is the surface potential several $\lambda$ away from the interface.

We have performed simulations of various devices with $d_{\rm ox} = 3.5$ nm and different SOI thicknesses. The channel length was chosen such that short-channel effects are being avoided. At the electrode–channel interfaces, an SB of 0.64 eV was assumed as appropriate for NiSi, and a bias of 1.0 V was chosen as in the experiments. Fig. 2(a) shows the values of $S$ extracted from the simulated curves (gray stars). An excellent agreement is found between the simulated and experimental data, which confirms that decreasing the SOI thickness leads to an increasingly thinner SB and, hence, to an improved carrier injection into the channel of SOI SB-MOSFETs. Note that increasing the SOI thickness beyond $d_{\rm soi} > 1.5 \times \lambda$, i.e., if $d_{\rm soi} > 4.5 \times d_{\rm ox}$, the bulk limit is reached, and the inverse subthreshold slope in this case remains at a constant, rather large value [18].

## IV. Analytical Analysis of the OFF-State

Analytical expressions for the current in the OFF-state and hence for the inverse subthreshold slope and the threshold voltage of SOI SB-MOSFETs can be derived by approximating the tunneling probability through the SB as follows: If for a certain energy the barrier is thinner than a tunneling distance $d$, the tunneling probability is set to 1. On the other hand, if the barrier is larger than $d$, no tunneling occurs. Hence, the transmission function $T(E)$ is unity for energies above $\tilde{\Phi} = \Phi_f(d)$ and zero below as illustrated in Fig. 3. Since in the OFF-state the density of mobile carriers is small and a very lightly doped substrate is considered, we set $\rho = 0$ in the following. Thus, the Poisson equation (1) can be solved analytically yielding $\tilde{\Phi} = \Phi_f(d) = (\Phi_{\rm SB} - \Phi_f^0)\exp(-d/\lambda) + \Phi_f^0$ for a given $d$, where $\Phi_f^0 = \Phi_g + \Phi_{\rm bi}$ is the surface potential in the channel several $\lambda$

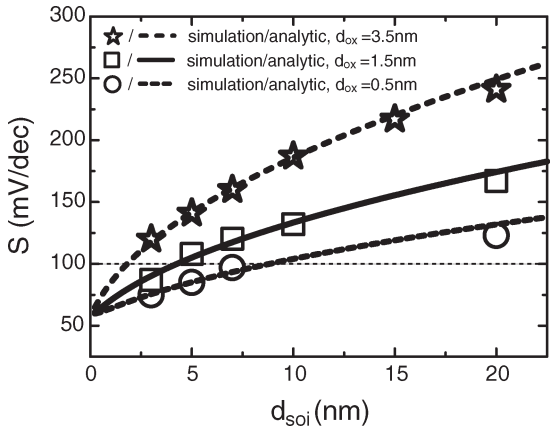


Fig. 4. $S$ versus SOI thickness extracted from simulations for devices with $d_{\rm ox} = 3.5$ nm (light gray stars), $d_{\rm ox} = 1.5$ nm (black squares), and $d_{\rm ox} = 0.5$ nm (gray circles). The corresponding results of the analytical approximation are shown as well. In all cases, the same tunneling distance $d$ was used.

away from the contact interface (see Fig. 3). Then, for large $V_{\rm ds}$ and $\tilde{\Phi} > kT$, the current in the OFF-state can be written as

$$I_d \approx M_s \frac{2e}{h^2} \int_{\tilde{\Phi}}^{\infty} dE \int_{\tilde{\Phi}}^{E} d\tilde{E} \sqrt{\frac{2m_l^\star}{\tilde{E}-\tilde{\Phi}}} f_s(E) \propto \exp\left(-\frac{\tilde{\Phi}-E_f^s}{kT}\right) \tag{2}$$

where $M_s$ accounts for higher subbands. With $S = \ln(10)((\partial I_d/\partial\tilde{\Phi})(\partial\tilde{\Phi}/\partial V_{\rm gs})(1/I_d))^{-1}$, a closed expression for $S$ can be found. Because in general $\lambda > d$, the result can be expanded, leading to

$$S = \frac{kT}{q}\ln(10)\frac{1}{1-\exp(-d/\lambda)} \approx \frac{kT}{q}\ln(10)\left(\frac{1}{2}+\frac{\lambda}{d}\right). \tag{3}$$

An estimation for $d$ can be obtained if the SB is approximated with a triangularly shaped potential of height $\Phi_{\rm SB}$ and width $\lambda$. Using the transmission probability calculated with the Wentzel–Kramers–Brillouin (WKB) approximation, an expression for $d$ can be calculated that shows a weak dependence on $\Phi_{\rm SB}$ as well as $d_{\rm soi}$ and $d_{\rm ox}$. If the transmission probability has dropped to $e^{-2}$, $d$ follows to be $\sim$ 3.1–3.9 nm for the SOI thicknesses considered above (note that the limiting case $d \to 0$ can only be achieved if $d/\lambda \to 0$).

Fig. 4 shows simulated data points for $S$ as well as results from the analytical calculation for devices with $d_{\rm ox} = 0.5$ nm (light gray stars and dashed line), $d_{\rm ox} = 1.5$ nm (black squares and straight line), and $d_{\rm ox} = 3.5$ nm (gray circles and dashed line). Since the tunneling distance $d$ is not exactly known, it was chosen as a constant fit parameter to get the best agreement with the simulated and experimental data. For all three different gate oxide thicknesses, best results were obtained with $d = 3.7$ nm, consistent with the range given above. The excellent agreement between the analytical results and simulated data (and hence with the experimental data in case of $d_{\rm ox} = 3.5$ nm) is apparent, showing that the analytical approximation describes the dependence of $S$ on $d_{\rm soi}$ and $d_{\rm ox}$ in SOI SB-MOSFETs very well. Since $\lambda$ is approximately proportional to $\sqrt{d_{\rm soi} d_{\rm ox}}$, this gives rise to the strong square-root dependence of $S$ on $d_{\rm soi}$ shown in Fig. 2(a). This finding seems to be in contrast to the results reported in [21], where the authors claim that $S$ is insensitive to changes in $d_{\rm soi}$. However, the reason for this discrepancy is that the devices investigated in [21] are double-gate SB-MOSFETs with $d_{\rm soi} = 5$ nm and $d_{\rm ox} = 0.5$ nm. The improved electrostatics in such devices leads to a smaller $\lambda$ if compared with single-gated devices. Hence, $d_{\rm soi} = 5$ nm in a double-gate device with $d_{\rm ox} = 0.5$ nm is already an SOI thickness where the square-root dependence of $S$ has become rather flat, comparable to the behavior around $d_{\rm soi} = 10$ nm of the single-gated device.

The derivation of expression (3) has an important implication: $S$ is independent of the doping concentration in the channel as long as we consider a fully depleted device. In fact, doping the channel leads only to a shift of the threshold voltage as can be seen by inspecting (1) but does not improve the carrier injection into the channel. Unless nonuniform doping profiles are used as has been realized employing dopant segregation during silicidation [22]–[24], the only way to improve the carrier injection for a fixed SB is to make $d_{\rm soi}$ and $d_{\rm ox}$ as small as possible.

## V. Variations of the Threshold Voltage

As was discussed above, the performance of SOI SB-MOSFETs improves with decreasing SOI thickness. However, it is well know from conventional SOI MOSFETs that the use of UTB SOI leads to threshold voltage shifts due to vertical quantization [8]. It has been argued in [21] that double-gate SB-MOSFETs are less vulnerable to such threshold voltage fluctuations. However, as will become clear below, this is only true in a narrow range of SOI thicknesses. Below and above this range, $V_{\rm th}$ exhibits a strong dependence on the SOI thickness.

Fig. 5 shows simulated transfer characteristics for SB-MOSFETs with $d_{\rm ox} = 3.5$ nm and different SOI thicknesses as indicated in the figure. In the simulation, the channel length $L$ was chosen long enough, i.e., $L \geq 100$ nm, to avoid any influence of short-channel effects.[2] To extract $V_{\rm th}$ from the curves, a constant current level of $10^{-5}$ A was chosen (see [25], for instance), consistent with a linear extrapolation of the $I_d - V_{\rm gs}$ curves to zero gate voltage. It is apparent that the threshold voltage significantly changes with $d_{\rm soi}$: First, $V_{\rm th}$ gets smaller with decreasing SOI thickness, but below $d_{\rm soi} = 3$ nm, it starts to increase again.

To understand this unusual nonmonotonic behavior, we make use of the analytical approximation discussed in the preceding section. For the determination of the threshold voltage, the same constant current definition is employed as mentioned earlier. Then, with the assumptions made above, i.e., that the Fermi function can be approximated with an exponential and that the first subband contributes most to the current, the following

[2]Since transport is being treated as ballistic, the exact channel length is irrelevant as long as short-channel effects are absent. This is justified because the SB represents the main scattering event, which is reflected in the fact that the ballistic simulations provide almost the same current level as the experimental devices (see, e.g., the device with $d_{\rm soi} = 10$ nm in Figs. 1 and 5).

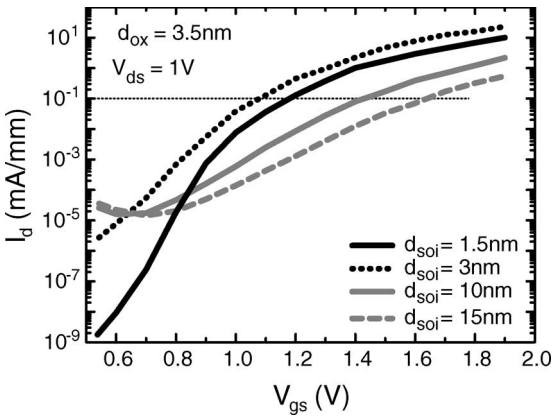


Fig. 5. Simulated transfer characteristics of SB-MOSFETs with $d_{\rm ox} = 3.5$ nm at $V_{\rm ds} = 1$ V for different SOI thicknesses. The threshold voltage is extracted using a constant current level as indicated by the dotted line.

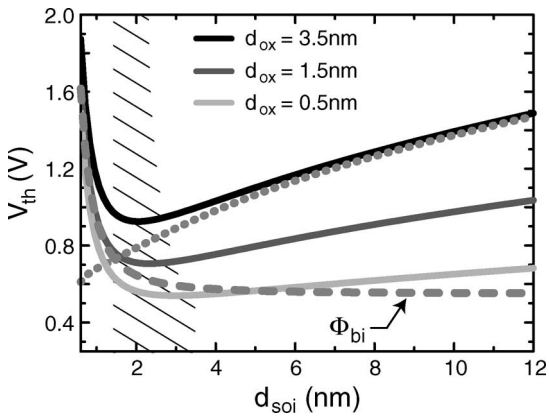


Fig. 6. Threshold voltage versus SOI thickness for devices with $d_{\rm ox} = 3.5$, 1.5, and 0.5 nm. The straight lines belong to the analytical approximation. The gray dashed line displays the $V_{\rm th}$ contribution of vertical quantization, whereas the gray dotted line refers to the contribution due to the effect of varying SOI thickness on the electrical behavior of SOI SB-MOSFETs.

closed expression for $V_{\rm th}$ can be derived if we set (2) equal to a constant current level of $I_0 = 10^{-1}$ mA/mm, i.e.,[3]

$$V_{\rm th} = \underbrace{\frac{kT}{q}\ln\left(\frac{I_0}{C}\right)\left(\frac{1}{2}+\frac{\lambda}{d}\right) + \frac{\Phi_{\rm SB}+\Delta E}{q}\left(\frac{\lambda}{d}-\frac{1}{2}\right)}_{\text{due to SB}} + \underbrace{\frac{\Phi_{\rm bi}+\Delta E}{q}}_{\text{due to subband splitting}} \tag{4}$$

where $C = M_s * (2e/h^2)\sqrt{2\pi m_l^\star}(kT)^{3/2}$. Again, carriers are considered to be confined within a hard-wall potential yielding $\Delta E \propto 1/d_{\rm soi}^2$, which gives comparable results to Omura *et al.* [8] in case of low-doped SOI (see also [16]). The first contribution to $V_{\rm th}$ stems from the presence of the SB, whereas the second one is due to vertical quantization only (note that vertical quantization also increases the effective SB height as accounted for by the term $(\Phi_{\rm SB}+\Delta E)/q$). Both contributions are plotted in Fig. 6 for a $d_{\rm ox} = 3.5$ nm. The first contribution decreases with decreasing SOI thickness (gray dotted line) due to an improved carrier injection for thinner SOI as discussed above. The contribution due to vertical quantization approaches $\Phi_{\rm bi}/q$ for large SOI thicknesses but strongly increases with decreasing $d_{\rm soi}$ (gray dashed line) because of the $1/d_{\rm soi}^2$ dependence. Therefore, one obtains a nonmonotonic behavior of $V_{\rm th}(d_{\rm soi})$ as shown in Fig. 6 for three different $d_{\rm ox}$ (straight lines). The two regions of increasing threshold voltage overlap, and $V_{\rm th}$ has a minimum at $d_{\rm soi} \sim 2{-}3$ nm. In a narrow range around this minimum, the threshold voltage of an SOI SB-MOSFET is less sensitive to changes in the SOI thickness than in case of vertical quantization alone, i.e., in case of a conventional SOI device. The range of SOI thicknesses where the $V_{\rm th}$ shift is small depends on $d_{\rm ox}$ and increases slightly with decreasing gate oxide thickness as indicated by the hatched area in Fig. 6. However, for smaller $d_{\rm soi}$, the SB-MOSFET exhibits the same threshold voltage shift as a conventional SOI MOSFET, and for larger SOI ticknesses, a substantial $V_{\rm th}$ shift is observed not seen in conventional SOI devices.

[3]Note that to obtain (4), $1/(1-\exp(-d/\lambda)) \approx 1/2 + \lambda/d$ and $1/(\exp(d/\lambda)-1) \approx \lambda/d - 1/2$ have been used, which is an excellent approximation even for $d_{\rm soi} = 3$ nm. For smaller $d_{\rm soi}$, the second term in (4) dominates.

## VI. Design Guidelines for SOI SB-MOSFETs

The discussion above, and in particular the analytical model, allows to set up the following design rules for SOI SB-MOSFETs. First, the gate oxide should be as small as possible to obtain a small $\lambda$ that guarantees a good carrier injection and, hence, an excellent electrical performance. Note that the requirement of having a gate oxide as small as possible even in long-channel devices is specific to SB-MOSFETs and in contrast to conventional MOSFETs where the first order $d_{\rm ox}$ should be as large as possible, still avoiding short-channel effects. Second, the SOI thickness should be scaled down to the range of minimum $V_{\rm th}$ to avoid threshold voltage variations. For realistic gate oxide thicknesses of 1–1.5 nm, the SOI thickness should be around 3 nm. In this case, an excellent carrier injection through the SB can be expected, leading to inverse subthreshold slopes significantly less than 100 mV/dec and small threshold voltage variations.

## VII. Conclusion

We studied the impact of the SOI body thickness and gate oxide thickness on the electrical behavior of UTB SOI SB-MOSFETs. To this end, transistor devices with varying body thickness were fabricated, and the inverse subthreshold slope was extracted. The experimental data show a square-root dependence on the SOI thickness resulting in an improved switching behavior if $d_{\rm soi}$ is scaled down. A comparison between the experimental and simulated data, as well as results from an analytical approximation, yields excellent agreement. In addition, we show that SOI SB-MOSFETs exhibit a nonmonotonic dependence of the threshold voltage on the SOI thickness. Our analysis shows that the gate oxide thickness should be as thin as possible, and the SOI thickness should be around 3 nm to facilitate an excellent performance in combination with small threshold voltage shifts.

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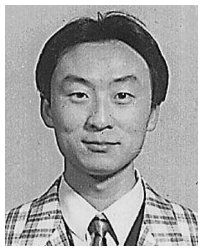
**Joachim Knoch** received the M.S. and Ph.D. degrees in physics from the Technical University of Aachen, Aachen, Germany, in 1998 and 2001, respectively.

At the Technical University of Aachen, he investigated quantum transport in superconductor/semiconductor hybrids based on III–V heterostructures as well as worked on the modeling and realization of ultrashort-channel silicon MOSFETs. From September 2001 to December 2002, he was with the Microsystems Technology Laboratory, Massachusetts Institute of Technology, Cambridge, where he worked on InP high-electron mobility transistor devices. Currently, he is a Research Scientist with the Institute of Thin Films and Interfaces, Research Center Juelich, Juelich, Germany. He is involved in the exploration of electronic transport in alternative field-effect transistor devices such as carbon nanotube field-effect transistors and ultrathin-body SB devices and MOSFETs based on strained-silicon.



**Min Zhang** was born in Shanghai, China, in 1974. He received the B.S. degree in physics from Shanghai University, Shanghai, in 1996, China, and the M.S. degree in microelectronics from the Technical University Dresden, Dresden, Germany, in 2002. He is currently working toward the Ph.D. degree in electrical engineering at RWTH Aachen University, Aachen, Germany.

In 1997, he joined Fujitsu LSI Technology Department and worked with low-power static random access memory design. His current research interests include Schottky MOSFET, salicide technology, and device characterization.

**Siegfried Mantl** (A'97–M'04) received the Ph.D. degree from the University of Innsbruck, Innsbruck, Austria, in 1976.

Since 1971, he has been with the Research Center Juelich, Juelich, Germany. He is the Head of the Ion Beam Technique Division of the Institute of Thin Films and Interfaces (ISG-1-IT) and a Professor of physics at RWTH Aachen University, Aachen, Germany. In 1981–1982, he spent a sabbatical year at the Materials Science Division, Argonne National Laboratory. He has authored or coauthored more than 250 journal articles, book chapters, and review articles. He is the holder of 15 patents. His research interests are focused on ion-beam techniques, epitaxial growth methods, modification and characterization of epitaxial materials, and development of nanoelectronic devices. A core emphasis is the processing and application of materials for silicon-based nanostructures and nanoscale MOSFETs, primarily exploiting the material properties of silicon, silicon germanium, and silicides.

**J. Appenzeller** (M'02–SM'04) received the M.S. and Ph.D. degrees in physics from the Technical University of Aachen, Aachen, Germany, in 1991 and 1995, respectively. His Ph.D. dissertation investigated quantum transport phenomena in low-dimensional systems based on III/V heterostructures.

He worked for one year as a Research Scientist with the Research Center Juelich, Juelich, Germany, before he became an Assistant Professor with the Technical University of Aachen in 1996. During his professorship, he explored mesoscopic electron transport in different materials, including carbon nanotubes and superconductor/semiconductor hybrid devices. From 1998 to 1999, he was with the Massachusetts Institute of Technology, Cambridge, as a Visiting Scientist, exploring the ultimate scaling limits of silicon MOSFET devices. Since 2001, he has been with the IBM T. J. Watson Research Center, Yorktown, NY, as a Research Staff Member mainly involved in the investigation of the potential of carbon nanotubes for future nanoelectronics.