

Received 20 December 2018; revised 4 February 2019; accepted 13 February 2019. Date of publication 18 February 2019; date of current version 8 March 2019.
The review of this paper was arranged by Editor P. Pavan.

Digital Object Identifier 10.1109/JEDS.2019.2899727

On the Physical Mechanism of Transient Negative Capacitance Effect in Deep Subthreshold Region

CHENGJI JIN^{1b} (Student Member, IEEE), TAKUYA SARAYA, TOSHIRO HIRAMOTO^{1b} (Member, IEEE),
AND MASA HARU KOBAYASHI^{1b} (Member, IEEE)

Institute of Industrial Science, University of Tokyo, Tokyo 153-8505, Japan

CORRESPONDING AUTHOR: C. JIN (e-mail: cjin@nano.iis.u-tokyo.ac.jp)

This work was supported in part by JST PRESTO.

ABSTRACT We have investigated the physical mechanism of steep subthreshold slope (SS) in ferroelectric FET (FeFET) based on a dynamic ferroelectric (FE) model without traversing the negative capacitance (NC) region of the S-shaped polarization-voltage predicted by Landau theory. The dynamic FE model is applied to an FE-dielectric (FE-DE) series capacitor as well as FeFET after calibration and verification by transient measurement of an FE-HfO₂ capacitor. By investigating current through the FE-DE series capacitor and the gate capacitor of FeFET, we find that incomplete screening of spontaneous polarization charge results in transient NC and sub-60 mV/dec SS. Also, it should be noted that, for FeFET, small depletion layer capacitance has an important role to cause strong depolarization effect and thus steep SS. Moreover, reverse drain induced barrier lowering happens even with this FE model. The model presented in this paper provides a reasonable interpretation for the previously reported steep SS of NC FETs.

INDEX TERMS Steep subthreshold slope (SS), ferroelectric, negative capacitance (NC).

I. INTRODUCTION

For future energy-efficient computing, ferroelectric FET (FeFET) with sub-60 mV/dec subthreshold slope (SS) caused by negative capacitance (NC) effect has attracted much attention [1]. NC effect was originally proposed based on the quasi-static NC (QSN) theory; there is a metastable NC region in the S-shaped P - V curve of ferroelectric (FE) predicted by phenomenological Landau theory, and NC in this region can be stabilized and accessible with an appropriate positive capacitor connected in series [1], [2]. According to the QSN theory, the capacitance matching for steep SS should be achieved near inversion region instead of subthreshold region with standard channel design [2]. However, many experimental results of long channel transistors show steep SS in deep subthreshold region with negligible hysteresis [3]–[5], which may not be fully explained only within the framework above. Moreover, the original QSN theory assumes a single-domain configuration in which all domains flip

simultaneously in response to the electric field as a large single-domain; this is not consistent with the classical FE physics. It is natural that multi-domain switching occurs via an anti-parallel configuration from the perspective of thermal dynamics [6], [7]. It is reported that NC cannot be stabilized for an FE-DE series capacitor (FE and DE are connected by metal) with reasonable device size according to the QSN theory considering multi-domain effect [8]. Whereas steep SS is observed for FeFET with internal metal gate as well [9]–[11]. In addition, some evidence shows polarization switching plays an important role in steep SS phenomenon as follows. While the stabilized NC in the S-shaped P - V curve can be accessed without polarization switching in unipolar sweep according to the QSN theory, it is reported that sub-60 SS happens only when the gate voltage sweep range is large enough to initialize polarization states and trigger large polarization switching in bipolar sweep [5]. NC is static and steep SS behavior should be time independent according to the

QSNCR theory. However, in [12], sub-60 SS is realized only within certain measurement time window determined by polarization switching dynamics, which indicates that NC effect has a transient aspect. Therefore, several groups have been exploring alternative interpretations for the NC effect as well as steep SS phenomenon [6], [13]–[17].

Recently, Preisach model which is a macroscopic model taking into account multi-domain effect and dynamic behavior of FE has been revisited. The model can well explain NC as a transient effect indicated by voltage drop and voltage snap back in measurements, if finite polarization switching delay is considered [13]–[16]. Since NC occurs only in transient conditions according to this theory, we call it the transient NC (TNC) theory. In our previous work, we show the simulation result of FeFET with sub-60 SS based on the TNC theory [17]. However, the physical mechanism of steep SS based on this theory are not fully clarified yet and need to be investigated.

In this paper, we further investigate the physical mechanism of steep SS in FeFET based on the TNC theory. By investigating current through the gate capacitor of FeFET, we find incomplete screening of spontaneous polarization charge results in TNC effect and sub-60 SS. In particular, small depletion layer capacitance has an important role to cause strong depolarization effect and thus steep SS in deep subthreshold region. Furthermore, we give a detailed explanation for sub-60 SS observed more prominently in reverse sweep than forward sweep in experiment. Finally, we show reverse drain induced barrier lowering (DIBL) observed in experiments can be explained even by the TNC theory considering polarization switching dynamics.

This paper is organized as follows. In Section II, the dynamic FE model and simulation methods implemented in this work are introduced. Then, in Section III-A, the dynamic FE model is verified by fitting simulation results to transient measurement of an FE-HfO₂ capacitor. Based on the fitting result, FE parameters are extracted for the following simulation. In Section III-B, an FE-DE series capacitor in response to a triangular waveform is simulated for understanding TNC with polarization switching and depolarization effect. In Section III-C, FeFET is simulated and a detailed analysis on physical mechanism of steep SS is presented. Finally, in Section IV, the conclusion is drawn.

II. FE MODEL DESCRIPTION AND SIMULATION METHODS

The dynamic FE model implemented in this work can be described as follows [16]–[22].

$$P_{\downarrow\uparrow}(V_{aux}) = P_s \tanh[w(V_{aux} \pm V_c)] \quad (1)$$

$$w = \frac{1}{2V_c} \ln \frac{P_s + P_r}{P_s - P_r} \quad (2)$$

$$\frac{dV_{aux}}{dt} = \frac{1}{\tau} (V_{fe} - V_{aux}) \quad (3)$$

where V_{fe} is voltage drop across FE, V_{aux} is auxiliary voltage introduced for simulating the impact of polarization switching delay, V_c is coercive voltage of FE, τ is polarization

switching delay due to domain nucleation and domain-wall propagation, P_r and P_s are remnant polarization and saturation polarization, respectively. It should be noted that, to focus on the physical mechanism by the simple model, minor loop caused by partial polarization switching at low sweep voltage amplitude is not fully implemented in this model.

Eq. (1) and (2) represent quasi-static P - V of FE. Eq. (3) represents dynamics of spontaneous polarization (P) with switching delay. For actual FE, a paraelectric (PE) component always co-exists. Therefore, free charge (Q) of an FE capacitor is expressed by [20]–[22]:

$$Q = P_{\downarrow\uparrow}(V_{aux}) + \frac{\epsilon_0 \epsilon_r V_{fe}}{t_{fe}} \quad (4)$$

The first term on the right-hand side of Eq. (4) represents the FE component and the second term represents the PE component. Here, t_{fe} is thickness of FE, ϵ_0 and ϵ_r are dielectric constant of vacuum and relative dielectric constant of FE, respectively. Note that the PE component is time-independent because of its much faster response compared to the FE component. Fig. 1 (a) illustrates the above-mentioned parameters in a quasi-static Q - V curve of FE. Fig. 1 (b) shows the equivalent circuit for an FE capacitor with time delay.

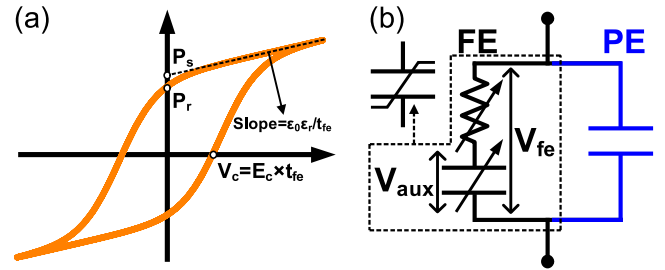


FIGURE 1. (a) The FE parameters illustrated in a quasi-static Q - V curve. (b) The equivalent circuit for an FE capacitor with time delay. In quasi-static conditions, V_{aux} equals to V_{fe} and the resistance is negligible.

The major difference between this model and the model based on the QSNCR theory is that in this model quasi-static capacitance of FE is always positive [16]. For FeFET simulation, Eq. (1)–(4) are self-consistently solved by combining with 2-D Poisson's equation and carrier continuity equations in technology computer-aided design (TCAD) [19].

III. RESULT AND DISCUSSION

A. FE MODEL VERIFICATION AND PARAMETER EXTRACTION

To verify this model and extract parameters of FE, the quasi-static Q - V curve of a 10 nm FE capacitor is simulated and fitted to experimental result of an FE-HfZrO₂ (HZO) capacitor, see Fig. 2 (a) [23], [24]. The extracted P_r , P_s , ϵ_r , and E_c (quasi-static parameters) are 20.1 $\mu\text{C}/\text{cm}^2$, 23 $\mu\text{C}/\text{cm}^2$, 35, and 1.16 MV/cm, respectively. Meanwhile, the experimental displacement current of the FE capacitor in response to a triangular waveform can be reproduced with the same fitting parameters shown in Fig. 2 (b).

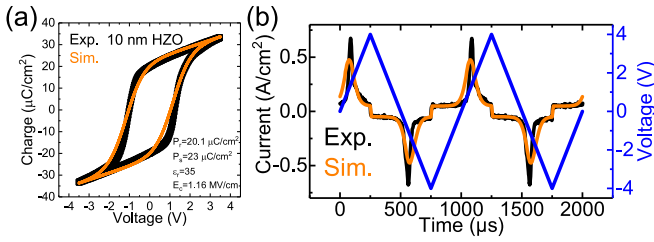


FIGURE 2. (a) The Q-V curve (100 Hz) of a 10 nm FE capacitor with parameter fitting. (b) Displacement current of the FE capacitor in response to a triangular waveform with the same fitting parameters [23].

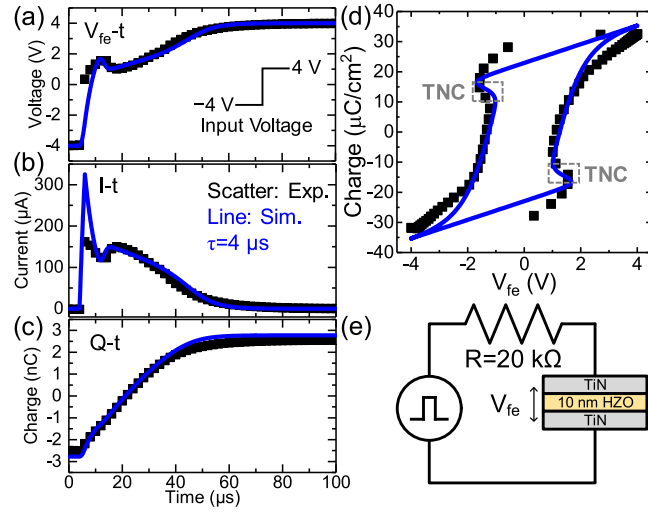


FIGURE 3. (a)-(c) Measured and simulated transient responses of the R-MFM. (d) Reconstructed $Q_{fe} - V_{fe}$ curves for both measurement and simulation. (e) The experiment and simulation set-up [23], [24].

In order to extract the dynamic parameter (τ), a resistor-metal/ferroelectric/metal (R-MFM) netlist which is the same as the experimental set-up in [23] and [24] is reconstructed in the simulation. Fig. 3 (a)-(c) show transient responses of the R-MFM netlist (Fig. 3 (e)) where $R = 20 \text{ k}\Omega$ and the input voltage pulse is from -4 V to 4 V . For the best fitting, $\tau = 4 \mu\text{s}$ is obtained. Fig. 3 (d) shows reconstructed $Q_{fe} - V_{fe}$ curves for both measurement and simulation where TNC is directly observed as a voltage snapback [25]. Similar transient responses are observed for an R-MFM netlist with $\text{Pb}(\text{Zr}_{0.2}\text{Ti}_{0.8})\text{O}_3$ (PZT) and explained as reverse domain nucleation and unrestricted domain growth according to time dependent Landau theory in [26]. However, in this paper, we use a different approach to explain this phenomenon.

Dynamic Q-V curves of a 10 nm FE capacitor in response to triangular waveforms with different frequencies are simulated by using the extracted FE parameters, see Fig. 4. As the frequency increases, the hysteresis window becomes larger due to polarization switching delay. Therefore, the model can appropriately describe dynamic FE properties.

B. TNC IN FE-DE SERIES CAPACITORS

By using the dynamic FE model and the FE parameters extracted above, transient characteristics of an FE-DE series

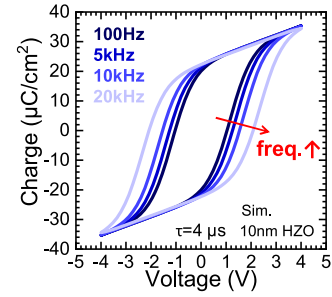


FIGURE 4. Simulated Q-V curves of a 10 nm FE capacitor in response to triangular waveforms with different frequencies by using the extracted FE parameters.

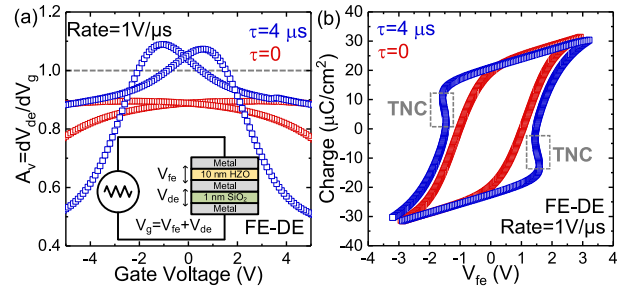


FIGURE 5. (a) Simulated internal voltage amplification (A_v) as a function of gate voltage (V_g) for an FE-DE series capacitor. (b) The corresponding $Q_{fe} - V_{fe}$ curves. A_v is larger than 1 and TNC is observed as a voltage snapback for $\tau = 4 \mu\text{s}$, while A_v is always smaller than 1 and no TNC is observed for $\tau = 0$ (quasi-static conditions).

capacitor which is a simplified model of an FeFET gate capacitor is simulated in response to a triangular waveform (Fig. 5 (a) inset). Fig. 5 (a) and (b) plot the simulated internal voltage amplification (A_v) as a function of gate voltage (V_g) and the corresponding $Q_{fe} - V_{fe}$ curves, respectively. A_v is larger than 1 in a certain V_g region and TNC is observed as a voltage snapback for $\tau = 4 \mu\text{s}$, while A_v is always smaller than 1 and no TNC occurs for $\tau = 0$ (quasi-static conditions). This means that finite polarization switching delay is responsible for TNC [17]. In fact, TNC was experimentally demonstrated in an FE-DE series capacitor in [27].

To better understand the physical mechanism of TNC, Fig. 6 (a) shows simulated polarization switching current (dP/dt), free charge current (dQ/dt), and voltage drop across FE (V_{fe}) as a function of time for $\tau = 4 \mu\text{s}$. TNC can be understood as the consequence of incomplete screening of spontaneous polarization charge (depolarization effect) [12], [28]–[30]. Fig. 6 (b) shows the schematic illustration of the physical mechanism for TNC in an FE-DE series capacitor. Initially, as V_g is swept in forward direction from the maximum negative value, V_{fe} increases by charging the PE component. After a certain time period, dP/dt increases due to the response of spontaneous polarization. When the increased dP/dt is larger than dQ/dt , in order to satisfy the charge balance condition: $Q = \epsilon_0 \epsilon_r E_{fe} + P$, V_{fe} has to drop, which is regarded as TNC. Meanwhile, there is a voltage gain in the internal node because of the reduced V_{fe} .

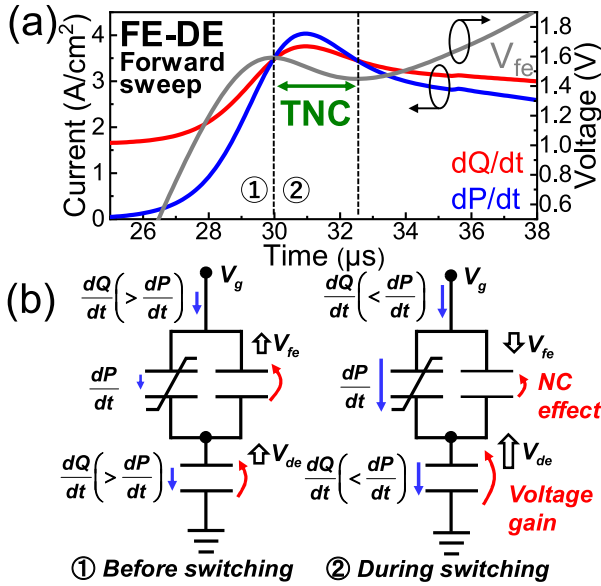


FIGURE 6. (a) Simulated polarization switching current (dP/dt), free charge current (dQ/dt), and voltage drop across FE (V_{fe}) as a function of time for $\tau = 4 \mu s$ in an FE-DE series capacitor. (b) Schematic illustration of physical mechanism for TNC in an FE-DE series capacitor.

and more increased V_{de} . Note that in quasi-static conditions, dP/dt is never larger than dQ/dt and TNC is not observed.

C. SIMULATION OF FEFET WITH STEEP SS

The transient behavior of FeFET is simulated by the dynamic FE model and parameters extracted above. Fig. 7 illustrates the simulated device structures and parameters. Reference MOSFET is also simulated for comparison. The amplitude of sweep voltage applied to the gate (V_{g_max}) is set to be high enough to make sure minor loop does not happen. First, $V_g = -V_{g_max}$ is applied for $10 \mu s$ to initialize the polarization state. Then, forward sweep from $-V_{g_max}$ to V_{g_max} is applied at a rate of $1 V/\mu s$, which is followed by reverse sweep from V_{g_max} to $-V_{g_max}$ at the same rate. Source and substrate are grounded. Drain voltage (V_d) is $50 mV$ for all the transistor simulations, unless otherwise specified.

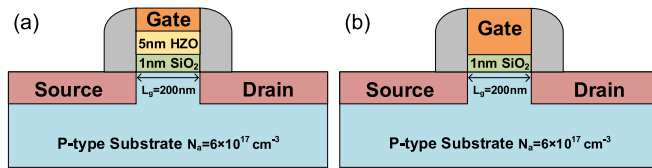


FIGURE 7. The simulated device structures and parameters. (a) FeFET with metal/ferroelectric/insulator/semiconductor (MFIS) gate stack, (b) reference MOSFET.

Fig. 8 (a)-(c) plot simulated $I_d - V_g$ curves and SS. Sub-60 SS is observed more prominently in reverse sweep and counter-clockwise hysteresis is caused by polarization switching for FeFET. FE-type hysteresis can be compensated by threshold voltage shift due to charge trapping and detrapping [14], [31], [32], which can be a reasonable explanation

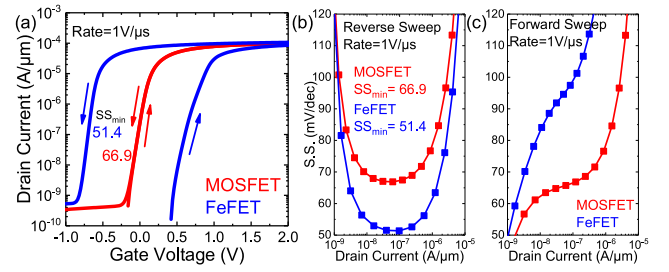


FIGURE 8. (a) Simulated $I_d - V_g$ curve for both FeFET and reference MOSFET with $\tau = 4 \mu s$ and sweep rate of $1 V/\mu s$. (b) SS in reverse sweep. (c) SS in forward sweep.

for sub-60 SS with negligible hysteresis observed in some experiments. Note that SS is also lower than 60 at very low I_d level in forward sweep for both FeFET and reference MOSFET mainly due to the displacement current at such high sweep rate. However, it is confirmed that TNC also has contribution to sub-60 SS for FeFET in forward sweep at very low I_d level, which will be discussed shortly.

Surface potential (ψ_s) amplification ($A_{vs} = d\psi_s/dV_g$) at $V_d = 0$ and the corresponding $Q_{fe} - V_{fe}$ relationship are extracted to further confirm the above simulated sub-60 SS of FeFET, see Fig. 9 (a) and (b). A_{vs} is larger than 1 in a certain V_g region and TNC is observed as a voltage snapback for both forward and reverse sweeps. Therefore, besides displacement current, TNC contributes to sub-60 SS in forward sweep at low I_d level as well.

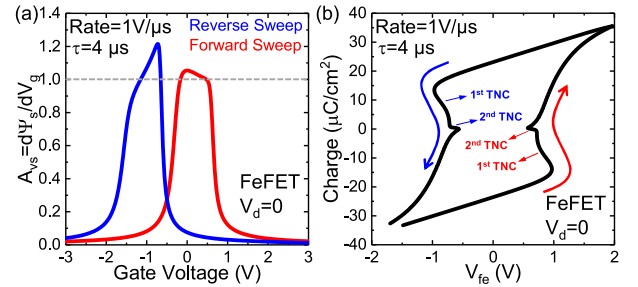


FIGURE 9. (a) Simulated surface potential amplification ($A_{vs} = d\psi_s/dV_g$) as a function of V_g when $V_d = 0$. (b) The corresponding $Q_{fe} - V_{fe}$ relationship. Two TNC regions with different slopes exist in each sweep direction.

Similarly to the discussion for the FE-DE series capacitor, dP/dt and dQ/dt versus time are plotted in Fig. 10 (a) and (b) for further understanding the relationship between TNC and steep SS phenomenon. During forward (reverse) sweep, two TNC regions ($|dP/dt| > |dQ/dt|$) are observed: the first one is in the accumulation (inversion) region and the second one is in transition from the accumulation (inversion) to the inversion (accumulation) region, see Fig. 10 (a) and (b). These two TNC regions can also be observed as two negative slope regions with different slopes in Fig. 9 (b). In subthreshold region, small depletion layer capacitance suppresses both dQ/dt and dP/dt and causes strong depolarization effect with $dP/dt > dQ/dt$, thus steep SS. Sub-60 is observed in wide I_d range only for reverse

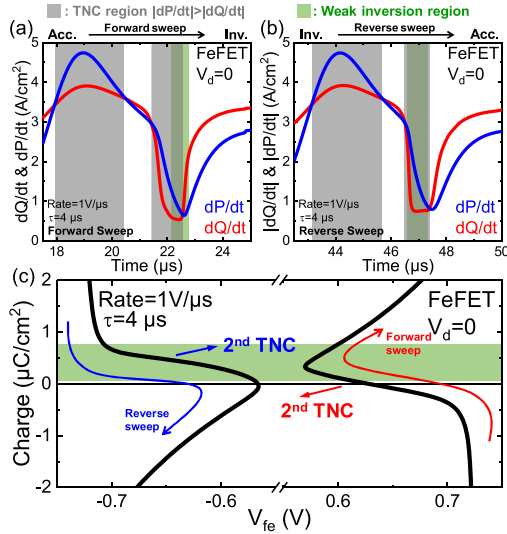


FIGURE 10. Simulated polarization switching current (dP/dt) and free charge current (dQ/dt) as a function of time for (a) forward and (b) reverse sweeps. (c) The zoomed-in $Q_{fe} - V_{fe}$ curve around 0 charge from Fig. 9 (b).

sweep, since the second TNC covers most of the weak inversion and depletion regions for reverse sweep (Fig. 10 (b)) but not forward sweep (Fig. 10 (a)). Fig. 10 (c) plots the zoomed-in $Q_{fe} - V_{fe}$ curve in Fig. 9 (b) around 0 charge corresponding to the subthreshold region in Fig. 10 (a) and (b), which also indicates that TNC is more prominent in wide I_d range in reverse sweep. With different FE parameters, it is possible to make TNC cover most of the weak inversion region in forward sweep as well, thus leading to sub-60 SS near V_{th} bidirectionally.

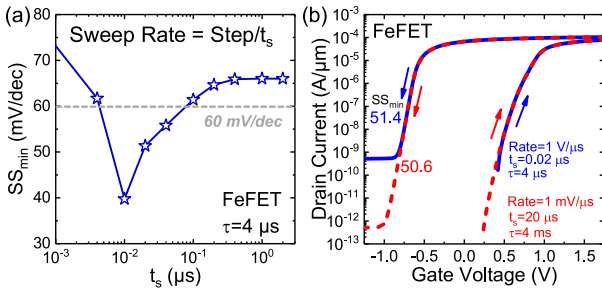


FIGURE 11. (a) Simulated SS_{min} in reverse sweep as a function of measurement time for each V_g step (t_s). (b) Simulated $I_d - V_g$ with two sets of τ and t_s . The reduced off-state current is due to reduced displacement current at lower sweep rate.

The sweep rate or measurement time dependence of subthreshold behavior is also simulated. Fig. 11 (a) plots simulated SS_{min} in reverse sweep as a function of measurement time for each V_g step (t_s). The result is similar to the experiment in [12]; sub-60 SS can be realized within a time window in which t_s is comparable to polarization switching delay (τ). For too fast sweep, spontaneous polarization will not respond due to its slow switching. For too slow sweep, spontaneous polarization charge can be fully screened by free charge (quasi-static conditions), thus no TNC occurs.

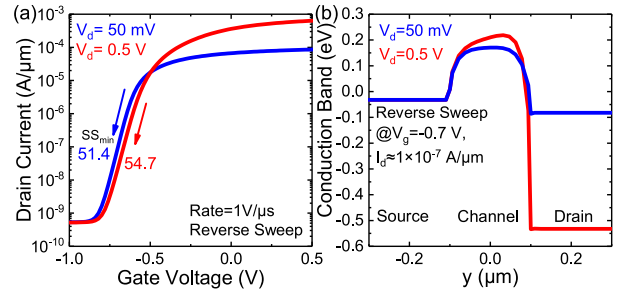


FIGURE 12. (a) Simulated $I_d - V_g$ curves of FeFET at $V_d = 50$ mV and 0.5 V in reverse sweep. (b) Conduction band diagrams of FeFET along the channel direction at $V_g = -0.7$ V for $V_d = 50$ mV and 0.5 V cases.

Moreover, if τ and t_s are increased (decreased) by the same order of magnitude, the shape of $I_d - V_g$ remains the same as illustrated in Fig. 11 (b). This means the $SS_{min} - t_s$ curve in Fig. 11 (a) shift to the slower (faster) t_s side with larger (smaller) τ . The reported τ for 10 nm Si:HfO₂ integrated in FeFET is from μs to ms magnitude [33]. With large τ of thin FE-HfO₂, it is possible to achieve sub-60 SS even in nearly quasi-static conditions.

Lastly, the previously reported reverse drain induced barrier lowering (DIBL) also happens with our simulation framework considering polarization switching dynamics [31], [34]. Fig. 12 (a) plots $I_d - V_g$ curves of FeFET at $V_d = 50$ mV and 0.5 V in reverse sweep. Fig. 12 (b) shows conduction band diagrams of FeFET along the channel direction at $V_g = -0.7$ V for $V_d = 50$ mV and 0.5 V cases. Unlike conventional MOSFET, FeFET with steep SS shows reverse DIBL attributed to TNC of FE and drain-to-gate coupling [35]–[37].

IV. CONCLUSION

We have developed an FE model based on polarization switching dynamics and verified the model by fitting simulation results to transient measurement of FE-HfO₂. Transient behaviors of an FE-DE series capacitor and FeFET are simulated based on this model to explore physical mechanism of TNC and steep SS phenomenon. We find TNC is caused by incomplete screening of spontaneous polarization charge ($dP/dt > dQ/dt$: depolarization effect). In addition, small depletion layer capacitance boosts depolarization effect, thus leading to steep SS in subthreshold region of FeFET. According to this model, sub-60 SS can be realized only within certain t_s window, which is determined by switching dynamics of spontaneous polarization. Moreover, the previously reported reverse DIBL can be observed even with our simulation framework with TNC. The theory described here can be an alternative explanation for experimentally demonstrated NCFETs with steep SS. However, more work is required to see if steep SS observed in the previous experiments is really caused by TNC with polarization switching as shown in this paper or not.

REFERENCES

- [1] S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," *Nano Lett.*, vol. 8, no. 2, pp. 405–410, 2008. doi: [10.1021/nl071804g](https://doi.org/10.1021/nl071804g).
- [2] A. I. Khan, C. W. Yeung, C. Hu, and S. Salahuddin, "Ferroelectric negative capacitance MOSFET: Capacitance tuning & antiferroelectric operation," in *IEDM Tech. Dig.*, Washington, DC, USA, Dec. 2011, pp. 3–11. doi: [10.1109/IEDM.2011.6131532](https://doi.org/10.1109/IEDM.2011.6131532).
- [3] M. H. Lee *et al.*, "Physical thickness 1.x nm ferroelectric HfZrO_x negative capacitance FETs," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2016, pp. 12.1.1–12.1.4. doi: [10.1109/IEDM.2016.7838400](https://doi.org/10.1109/IEDM.2016.7838400).
- [4] C.-C. Fan, C.-H. Cheng, Y.-R. Chen, C. Liu, and C.-Y. Chang, "Energy efficient HfAlO_x NCFET: Using gate strain and defect passivation to realize nearly hysteresis-free sub-25mV/dec switch with ultralow leakage," in *IEDM Tech. Dig.*, Dec. 2017, pp. 561–564. doi: [10.1109/IEDM.2017.8268444](https://doi.org/10.1109/IEDM.2017.8268444).
- [5] P. Sharma *et al.*, "Impact of total and partial dipole switching on the switching slope of gate-last negative capacitance FETs with ferroelectric hafnium zirconium oxide gate stack," in *Proc. IEEE VLSI Technol.*, Jun. 2017, pp. T154–T155. doi: [10.23919/VLSIT.2017.7998160](https://doi.org/10.23919/VLSIT.2017.7998160).
- [6] S. J. Song *et al.*, "Alternative interpretations for decreasing voltage with increasing charge in ferroelectric capacitors," *Sci. Rep.*, vol. 6, Feb. 2016, Art. no. 20825. doi: [10.1038/srep20825](https://doi.org/10.1038/srep20825).
- [7] M. Kobayashi, "A perspective on steep-subthreshold-slope negative-capacitance field-effect transistor," *Appl. Phys. Exp.*, vol. 11, no. 11, pp. 1–20, Oct. 2018. doi: [10.7567/APEX.11.110101](https://doi.org/10.7567/APEX.11.110101).
- [8] M. Hoffmann, M. Pešić, S. Slesazek, U. Schroeder, and T. Mikolajick, "On the stabilization of ferroelectric negative capacitance in nanoscale devices," *Nanoscale*, vol. 10, pp. 10891–10899, May 2018. doi: [10.1039/C8NR02752H](https://doi.org/10.1039/C8NR02752H).
- [9] A. Rusu, G. A. Salvatore, D. Jiménez, and A. M. Ionescu, "Metal-ferroelectric-meta-oxide-semiconductor field effect transistor with sub-60mV/decade subthreshold swing and internal voltage amplification," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2010, pp. 395–398. doi: [10.1109/IEDM.2010.5703374](https://doi.org/10.1109/IEDM.2010.5703374).
- [10] J. Zhou *et al.*, "Ferroelectric HfZrO_x Ge and GeSn PMOSFETs with sub-60 mV/decade subthreshold swing, negligible hysteresis, and improved I_{DS}," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2016, pp. 12.2.1–12.2.4. doi: [10.1109/IEDM.2016.7838401](https://doi.org/10.1109/IEDM.2016.7838401).
- [11] J. Jo and C. Shin, "Negative capacitance field effect transistor with hysteresis-free sub-60-mV/decade switching," *IEEE Electron Device Lett.*, vol. 37, no. 3, pp. 245–248, Mar. 2016. doi: [10.1109/LED.2016.2523681](https://doi.org/10.1109/LED.2016.2523681).
- [12] P. Sharma, J. Zhang, K. Ni, and S. Datta, "Time-resolved measurement of negative capacitance," *IEEE Electron Device Lett.*, vol. 39, no. 2, pp. 272–275, Feb. 2018. doi: [10.1109/LED.2017.2782261](https://doi.org/10.1109/LED.2017.2782261).
- [13] B. Obradovic, T. Rakshit, R. Hatcher, J. Kittl, and M. S. Rodder, "Modeling of negative capacitance of ferroelectric capacitors as a non-quasi static effect," *arXiv:1801.01842*, 2018. [Online]. Available: <https://arxiv.org/abs/1801.01842>
- [14] B. Obradovic, T. Rakshit, R. Hatcher, J. A. Kittl, and M. S. Rodder, "Ferroelectric switching delay as cause of negative capacitance and the implications to NCFETs," in *Proc. IEEE VLSI Technol.*, Jun. 2018, pp. T51–T52.
- [15] B. Obradovic, T. Rakshit, R. Hatcher, J. A. Kittl, and M. S. Rodder, "Modeling transient negative capacitance in steep-slope FeFETs," *IEEE Trans. Electron Devices*, vol. 65, no. 11, pp. 5157–5164, Nov. 2018. doi: [10.1109/TED.2018.2868479](https://doi.org/10.1109/TED.2018.2868479).
- [16] A. K. Saha, S. Datta, and S. K. Gupta, "'Negative capacitance' in resistor-ferroelectric and ferroelectric-dielectric networks: Apparent or intrinsic?" *J. Appl. Phys.*, vol. 123, no. 10, 2018, Art. no. 105102. doi: [10.1063/1.5016152](https://doi.org/10.1063/1.5016152).
- [17] C. Jin, T. Hiramoto, and M. Kobayashi, "On the physical origin of steep subthreshold slope in ferroelectric FET: Transient negative capacitance effect caused by polarization switching delay," in *Proc. Int. Conf. Solid-State Devices Mater. (SSDM)*, Sep. 2018, pp. 199–200.
- [18] B. Jiang, P. Zurcher, R. E. Jones, S. J. Gillespie, and J. C. Lee, "Computationally efficient ferroelectric capacitor model for circuit simulation," in *Proc. IEEE VLSI Technol.*, Jun. 1997, pp. 141–142. doi: [10.1109/VLSIT.1997.623738](https://doi.org/10.1109/VLSIT.1997.623738).
- [19] *Sentaurus Device User Guide Version: H-2014.09*, Synopsys, Mountain View, CA, USA, Mar. 2014.
- [20] S. L. Miller, J. R. Schwank, R. D. Nasby, and M. S. Rodger, "Modeling ferroelectric capacitor switching with asymmetric nonperiodic input signals and arbitrary initial conditions," *J. Appl. Phys.*, vol. 70, no. 5, pp. 2849–2860, 1991. doi: [10.1063/1.349348](https://doi.org/10.1063/1.349348).
- [21] K. Ni, M. Jerry, J. A. Smith, and S. Datta, "A circuit compatible accurate compact model for ferroelectric-FETs," in *Proc. IEEE VLSI Technol.*, Honolulu, HI, USA, Jun. 2018, pp. T131–T132.
- [22] K. Ni *et al.*, "Critical role of interlayer in Hf_{0.5}Zr_{0.5}O₂ ferroelectric FET nonvolatile memory performance," *IEEE Trans. Electron Devices*, vol. 65, no. 6, pp. 2461–2469, Jun. 2018. doi: [10.1109/TED.2018.2829122](https://doi.org/10.1109/TED.2018.2829122).
- [23] M. Kobayashi, N. Ueyama, K. Jang, and T. Hiramoto, "Experimental study on polarization-limited operation speed of negative capacitance FET with ferroelectric HfO₂," in *IEDM Tech. Dig.*, Dec. 2016, pp. 12.3.1–12.3.4. doi: [10.1109/IEDM.2016.7838402](https://doi.org/10.1109/IEDM.2016.7838402).
- [24] K. Jang, N. Ueyama, M. Kobayashi, and T. Hiramoto, "Experimental observation and simulation model for transient characteristics of negative-capacitance in ferroelectric HfZrO₂ capacitor," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 346–353, 2018. doi: [10.1109/JEDS.2018.2806920](https://doi.org/10.1109/JEDS.2018.2806920).
- [25] A. I. Khan *et al.*, "Negative capacitance in a ferroelectric capacitor," *Nat. Mater.*, vol. 14, no. 2, pp. 182–186, 2015. doi: [10.1038/nmat4148](https://doi.org/10.1038/nmat4148).
- [26] M. Hoffmann *et al.*, "Ferroelectric negative capacitance domain dynamics," *J. Appl. Phys.*, vol. 123, no. 18, 2018, Art. no. 184101. doi: [10.1063/1.5030072](https://doi.org/10.1063/1.5030072).
- [27] A. I. Khan *et al.*, "Differential voltage amplification from ferroelectric negative capacitance," *Appl. Phys. Lett.*, vol. 111, no. 25, 2017, Art. no. 253501. doi: [10.1063/1.5006958](https://doi.org/10.1063/1.5006958).
- [28] P. Zubko *et al.*, "Negative capacitance in multidomain ferroelectric superlattices," *Nature*, vol. 534, no. 7608, pp. 524–528, Jun. 2016. doi: [10.1038/nature17659](https://doi.org/10.1038/nature17659).
- [29] S.-C. Chang, U. E. Avci, D. E. Nikonov, S. Manipatruni, and I. A. Young, "Physical origin of transient negative capacitance in a ferroelectric capacitor," *Phys. Rev. Appl.*, vol. 9, Jan. 2018, Art. no. 014010. doi: [10.1103/PhysRevApplied.9.014010](https://doi.org/10.1103/PhysRevApplied.9.014010).
- [30] Q. Han *et al.*, "Subthreshold behavior of floating-gate MOSFETs with ferroelectric capacitors," *IEEE Trans. Electron Devices*, vol. 65, no. 10, pp. 4641–4645, Oct. 2018. doi: [10.1109/TED.2018.2863727](https://doi.org/10.1109/TED.2018.2863727).
- [31] M. Jerry *et al.*, "Insights on the DC characterization of ferroelectric field-effect-transistors," in *Proc. IEEE 76th Device Res. Conf. (DRC)*, Santa Barbara, CA, USA, 2018, pp. 1–2. doi: [10.1109/DRC.2018.844219](https://doi.org/10.1109/DRC.2018.844219).
- [32] E. Yurchuk *et al.*, "Charge-trapping phenomena in HfO₂-based FeFET-type nonvolatile memories," *IEEE Trans. Electron Devices*, vol. 63, no. 9, pp. 3501–3507, Sep. 2016. doi: [10.1109/TED.2016.2588439](https://doi.org/10.1109/TED.2016.2588439).
- [33] H. Mulaosmanovic *et al.*, "Switching kinetics in nanoscale hafnium oxide based ferroelectric field-effect transistors," *ACS Appl. Mater. Interfaces*, vol. 9, no. 4, pp. 3792–3798, Feb. 2017. doi: [10.1021/acsami.6b13866](https://doi.org/10.1021/acsami.6b13866).
- [34] M. Si *et al.*, "Steep slope hysteresis-free negative capacitance MoS₂ transistors," *Nat. Nanotechnol.*, vol. 13, pp. 24–28, Dec. 2017. doi: [10.1038/s41565-017-0010-1](https://doi.org/10.1038/s41565-017-0010-1).
- [35] H. Ota *et al.*, "Fully coupled 3-D device simulation of negative capacitance FinFETs for sub 10 nm integration," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2016, pp. 12.4.1–12.4.4. doi: [10.1109/IEDM.2016.7838403](https://doi.org/10.1109/IEDM.2016.7838403).
- [36] A. K. Saha, P. Sharma, I. Dabo, S. Datta, and S. K. Gupta, "Ferroelectric transistor model based on self-consistent solution of 2D Poisson's, non-equilibrium Green's function and multi-domain Landau Khalatnikov equations," in *IEDM Tech. Dig.*, Dec. 2017, pp. 13.5.1–13.5.4. doi: [10.1109/IEDM.2017.8268385](https://doi.org/10.1109/IEDM.2017.8268385).
- [37] J. Seo, J. Lee, and M. Shin, "Analysis of drain-induced barrier rising in short-channel negative-capacitance FETs and its applications," *IEEE Trans. Electron Devices*, vol. 64, no. 4, pp. 1793–1798, Apr. 2017. doi: [10.1109/TED.2017.2658673](https://doi.org/10.1109/TED.2017.2658673).



CHENGJI JIN received the B.S. degree in electronics engineering from the Zhejiang University of Technology, Hangzhou, China, in 2014 and the M.S. degree in electronics engineering from Xidian University, Xi'an, China, in 2017. He is currently pursuing the Ph.D. degree with the Institute of Industrial Science, University of Tokyo, Tokyo, Japan.



TAKUYA SARAYA received the B.S. and M.S. degrees in electrical and electronics engineering from Chiba University in 1993 and 1995, respectively. Since 1995, he has been a Research Associate with the Institute of Industrial Science, University of Tokyo. His research interests are device physics in silicon MOSFET and IGBTs.



TOSHIRO HIRAMOTO (M'92) received the B.S., M.S., and Ph.D. degrees in electronics engineering from the University of Tokyo, Japan, in 1984, 1986, and 1989, respectively. In 1989, he joined the Device Development Center, Hitachi Ltd., Ome, Japan. He joined the Institute of Industrial Science, University of Tokyo in 1994, where he has been a Professor since 2002. He is a fellow of the Japan Society of Applied Physics and a member of IEICE.



MASAHARU KOBAYASHI (M'09) received the B.S. and M.S. degrees in electronics engineering from the University of Tokyo, Tokyo, Japan, in 2004 and 2006, respectively, and the Ph.D. degree in electronics engineering from Stanford University, Stanford, CA, USA, in 2010. He joined IBM T.J. Watson Research Center, Yorktown Heights, NY, USA, in 2010. Since 2014, he has been an Associate Professor with the Institute of Industrial Science, University of Tokyo.