ON THE REALIZATION OF SWITCHED-CAPACITOR INTEGRATORS FOR SIGMA-DELTA MODULATORS

Examensarbete utfört i Elektroniksystem

vid Linköpings Tekniska Högskola

av

Krister Berglund

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Linköping 2007-12-21

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Linköping, 21 December 2007.

Date of presentation
December 14:th, 2007
Date of publication
December 21:th, 2007

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URL for electronic version
http://www.ep.liu.se

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On the realization of switched-capacitor integrators for sigma-delta modulators

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Abstract

The sigma-delta techniques for analog-to-digital conversion have for long been utilized when high precision is needed. Despite the fact that these have been realized by a numerous of different structures, the theory of how to construct a sigma-delta ADC is not very extensive.

This thesis will assume that an SFG description of the CRFB sigma-delta modulator has been designed and presents a structured method to obtain a circuit realization of the integrators in a specific modulator.

The first activity is to scale the inputs to each integrator in order to make sure that the produced outputs of each integrator is within the output-range of the OTA which is used. The next thing that is presented is an algorithmic way of descending from the SFG design of the modulator down to a switched-capacitor implementation of the system.

To be able to continue with the circuit realization, one needs to do a rigorous noise analysis of the modulator, which gives the sizes of the different capacitors in the SC-circuits. The last topic of this thesis is a method to obtain the specifications of the OTA in each integrator.

Keywords
Sigma-Delta modulator, Analog-to-digital converter, Switched-Capacitor, Scaling, Low-power, Analog IC design

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ACKNOWLEDGEMENTS

We would like to thank Dr. Per Löwenborg for support and inspiration, our opponents Anders Ödlund and Björn Lundgren for the comments on the thesis and Hanna Svensson for the comments and questions regarding this thesis.

Finally we would like to thank our familys for beeing our biggest fans and Svante Turesson for all the cheerful music with awful lyrics.

NOMENCLATURE

Most of the acronyms which is used in this thesis are explained here.

ADC	-	Analog-to-Digital Conversion
CRFB	-	Cascade of Resonators with distributed Feed-Back
DAC	-	Digital-to-Analog Conversion
DSP	-	Digital Signal Conversion
NTF	-	Noise transfer function
OTA	-	Operational Tranconductance Amplifier
OSR	-	Oversampling Ratio
P1	-	Phase 1 trigger signal
P2	-	Phase 2 trigger signal
PSD	-	Power Spectral Density
S&H	-	Sample-and-Hold
SC	-	Switched Capacitor
SFG	-	Signal Flow Graph
SNR	-	Signal-to-Noise Ratio
SQNR	-	Signal-to-Quantization Noise Ratio
STF	-	Signal transfer function
T&H	-	Track-and-Hold

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INTRODUCTION

1.1 PROJECT DESCRIPTION

Delta-sigma AD-conversion is a method which is commonly used when high resolution needs to be achieved and it has been used for a long time in the commercial world. The only problem is that there is no theory which really investigates the implementation details when building the loop-filter of the modulator and this needs to be done in order to be able to satisfy the industry's goal of low power dissipation.

1.2 OBJECTIVES

The goal of our work is to find a structured method to go from a given SFG description of a sigma-delta modulator to a circuit realization of the modulator, where the focus is upon the trade-off between power consumption and precision of the modulator.
We will also investigate the benefits of proper scaling and the modulators sensitivity to noise, since both of these activities are crucial when designing a sigma-delta modulator.

The last activity of this thesis is to construct a "cookbook" for setting the requirements of the OTA's, which is used to realize the SC-integrators in the circuit. This activity is particularily important since the OTA's are the main power consumers of a sigma-delta modulator.

A subgoal of this thesis is to always have in mind that the modulator should be able to realize a bandpass sigma-delta modulator. This is of interest because of the fact that bandpass sigma-delta ADC's with variable center frequency are the next to be accomplished within this technology.

1.3 LIMITATIONS

The limitations of this thesis is given by the fact that we will concentrate on the circuit realization of the loop-filter in the modulator. This basicly means that:

- The focus of this project will be the modulator which means that we are not going to consider the decimation filter, which is placed at the output of the modulator.
- We are not going the investigate how to realize the circuits of the ADC and the DAC, which are used to realize the feedback path. These components will instead be modeled as ideal components and the only thing that will be considered is the reference levels of the AAC, especially since these levels might be changed due to scaling.
- The switches in the design are going to be realized as ideal, but with limited on and off resistance.
- Due to lack of time, we were not able to build the bias network and common-mode feedback of the OTA. The bias network is instead realized by DC-voltage sources and the common-mode feedback is realized as an ideal stabilizer.

1.4 WORK METHODOLOGY

This thesis will be performed according to the Top-Down design methodology, which is the standard way of constructing a mixed-signal system. We will start with a SFG-description of a modulator according to the CRFB structure and work our way down to the finished circuit.

2

THEORY

2.1 ANALOG-TO-DIGITAL CONVERSION

To be able to process data by digital techniques, one often needs to transform pieces of the analog world to something on digital form. An example could be that one has some sensor data that have to be processed. Best way to look into the data is often by digital signal processing, but the sensors give analog voltages as data. Here one wants to convert these analog signals to digital discrete values. This is made by analog-to-digital conversion (A/D conversion) and the device for this is called the analog-to-digital converter (ADC).

The analog signal is divided into time-discrete samples, with the time of the sample period T_s between each sample. The digital data are samples quantized to 2^N discrete levels for N number of bits. The more bits, the more accuracy is achievable.

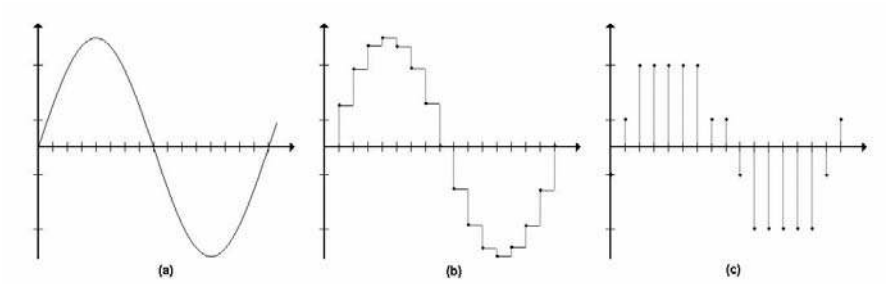

Figure 2.1: a) Analog signal. b) Sampled signal. c) Sampled and quantized signal.

The faster the signal is sampled, the higher signal frequencies can be converted to digital domain without loosing information by the phenomenom of aliasing.

Looking att sampling in the frequency domain, the Fourier transform of the analog continous input signal has a frequency spectrum streching over all frequencies from zero to infinity. Sampling the signal with sampling frequency f_s makes a time-discrete signal, with a Fourier transform that is periodic with the normalized period 2π, where π corresponds to half the sampling frequency, $f_s/2$. Every frequency component higher than $f_s/2$ will cause aliasing by appearing over the limits for the period. It will appear at undesired angular frequencies. In Fig. 2.2, this is shown.

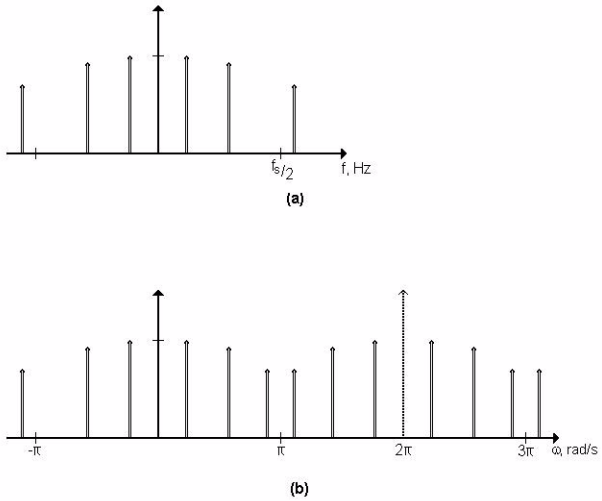

Figure 2.2: Ideal sampling. a) Magnitude spectrum of a continous-time signal. b) Magnitude spectrum of the sampled, time-discrete signal.

Thus, to be able to contain signal information, the signal frequencies should be smaller than half the sampling frequency. If the signal fulfills this request, the analog signal can ideally be reconstructed again by filtering the digital signal. This is known as the Nyquist theorem.[4]

The most common measurement of precision of an ADC is the signal-to-noise ratio (SNR). If the input signal is a perfect sinusoid, then the output signal from the ADC will be a perfect sinusoid with noise added. The power of the wanted signal at the output divided with the noise power at the output is the signal-to-noise ratio.

2.1.1 SAMPLE AND HOLD

A common approach to divide the continous analog signal into processible parts is to use a sample-and-hold circuit (S&H), that reads the signal value with equal time-steps T_s in between each reading, and holds that value at the output until next reading. The frequency at which the signal is read is the sample frequency f_s.

In most cases the device track-and-hold (T&H) can replace the S&H. Otherwise, the implementation of S&H is done by T&H's in series. The T&H tracks the signal for the first part of the sample period, and holds the signal for the second part of the period. The basic implementation of this device is straight-forward, as Fig. 2.3 shows. Still, aiming to make a sampling device that samples the correct voltage with good accuracy and is capable of holding it and send it further, one encounters problems mainly due to non-idealities in switches. Buffers at input and outputs, differential design and special techniques are required for good result.

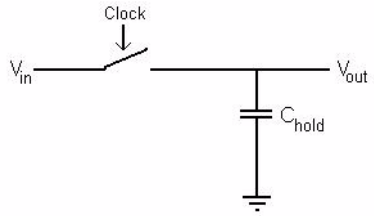

Figure 2.3: Basic implementation of track-and-hold.

2.1.2 QUANTIZATION

When converting to digital data, each sample has to be quantized to a discrete value. In the analog domain the value of the signal is determined by the signal voltage. To determine what digital value to assign the sample, a ladder of comparators can be used. Each comparator tells if the signal is higher or lower than a certain reference level. For N bits resolution, that is 2^N quantization levels, 2^N-1 comparators will be needed to place the sample in the right level. A structure built with a sample-and-hold and a ladder of comparators realizes the flash ADC.

Fig. 2.4 shows a 2-bit quantizer realization. Each comparator gives logic '1' (logic '0') as output if the differential input to the comparator is positive (negative), i.e., the V_{in}-signal is higher (lower) than the reference voltage in to the comparator. The quantizer outputs give three thermometer coded bits. A digital decoder converts the data to binary code.

The reference voltages are divided from the V_{ref}, which should be given from the power supply. If there are mismatches in resistace sizes, the quantisation levels will be non-uniformly distributed, causing non-linear behaviour.

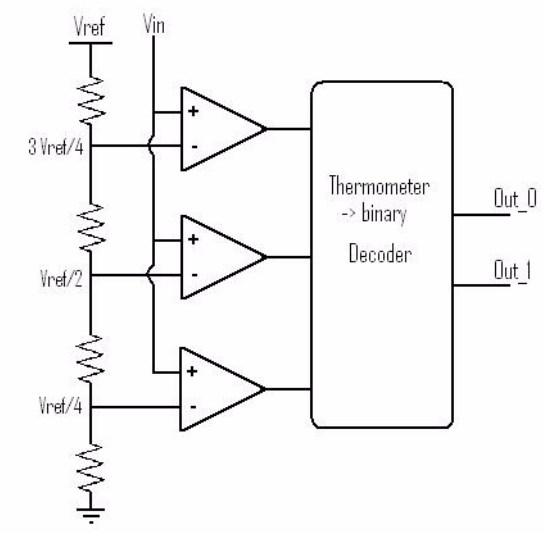

Figure 2.4: Realization of 2-bit quantizer.

The flash ADC is a realizable and widely used structure. However, for hard requirements on SNR, thus many bits of resolution, the number of comparators will be high, and the accuracy required for each comparator and its reference voltage will be difficult to achieve with non-ideal components. With special techniques to linearize the behavior of the flash ADC one can still not be able to achieve better than possibly 10-12 bits resolution.

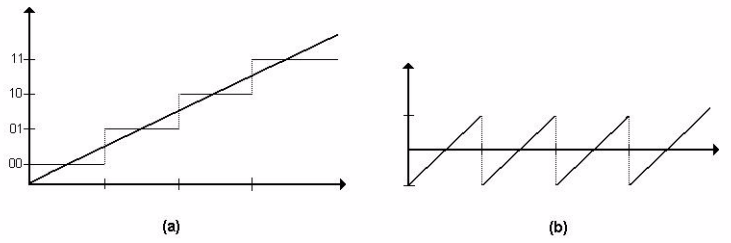

Figure 2.5: a) 2-bit quantization of a ramp as input signal. b) Plot of the quantization error.

The difference between the analog value and the quantized value is called the quantization error. With properly chosen reference voltages, the quantization error can be controlled not to be larger than half the quantization step size.

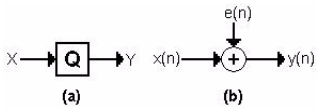

Figure 2.6: a) Y is the quantization of X. b) Linear model.

In the linear model, the quantization error is modelled as an uncorrelated zero-mean noise source, with amplitude inversely proportional to the number of quantizer levels. Looking at this noise in the frequency domain, the noise is assumed to be equally spread over all frequencies. It is called white noise.

2.1.3 OVERSAMPLING A/D-CONVERSION

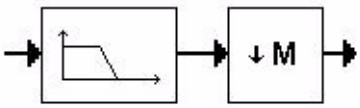

Figure 2.7: Decimation.

Oversampling A/D-conversion means that the ADC samples the signal faster than the digital system needs, and decimation is made after the A/D conversion. Decimation means low-pass filtering followed by downsampling.

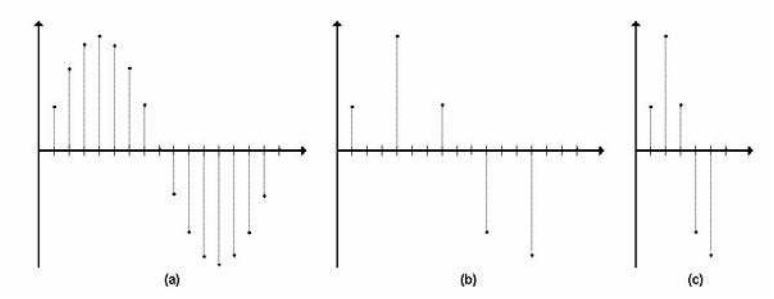

Figure 2.8: Downsampling of a sinusoid with M = 3. The result is a sinusoid with three times higher frequecy.

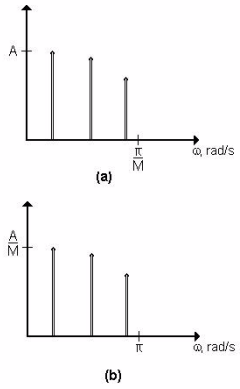

Figure 2.9: Downsampling in frequency domain. a) Filtered signal spectrum consisting of three in-band tones. b) Downsampled signal spectrum. The amplitudes are scaled down, and frequencies scaled up.

With ideal filtering we get rid of noise at frequencies above the stop band edge. Hence, by oversampling the analog signal, quantization noise power is decreased. This gain is on the cost of less signal frequency range.

A way to get even higher SNR is to shape the quantization noise, so that when the decimation filter attenuates the high frequencies, only a small amount of the quantization noise remains in the signal frequency band. This is the concept of sigma-delta A/D-conversion.

2.2 LOW-PASS SIGMA-DELTA A/D-CONVERSION

The most accurate ADC's of today, operating at relatively high frequenqies, are sigma-delta ADC's. For example, Texas Instruments' ADS1282 can give 130 dB SNR, for 24 bits, at a sample frequency of 4 kHz. With a resolution of 18 bits and SNR of 101 dB, the AD7678 from Analog Devices can operate at a sample frequency of 100 kHz.

The architecture of the converter can vary, but the concept is that the quantized signal is fed back to an analog integrating filter part, so that the noise transfer function (NTF) from the quantizer to the output of the modulator is high-pass-shaped. The transfer function from input to output of the modulator, the signal transfer function (STF), is instead shaped to get full signal swing out from low frequencies, while higher frequency components are either suppressed or not considered. They will be filtered out with the decimation filter before downsampling.

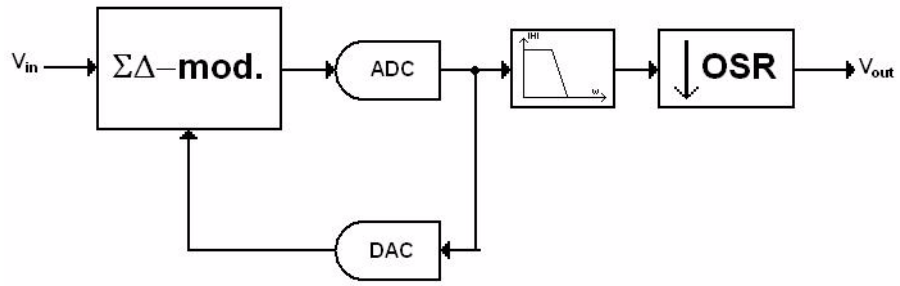

Figure 2.10: Sigma-delta ADC.

Implementation of a sigma-delta ADC requires the analog modulator, an internal ADC for quantization, digital-to-analog converter (DAC) for feedback, and digital filtering and downsampling for decimation.

2.2.1 PROPERTIES OF A SIGMA-DELTA MODULATOR

The heavier the NTF is high-pass shaped, the less quantization noise will distort the signal. However, with high amplidudes at high frequencies, there will be a risk of unstability of the modulator. The input signal swing have to be scaled down from full-swing for most modulator structures, not to force the signal energies in the integrators too high, giving unstable behaviour.

With several cascaded integrators, the NTF gets as many zeros and poles as the number of integrators. The number of integrators in a sigma-delta modulator is referred to as the modulator order. As in every filter implementation, the higher the modulator order, the more effective is the filter function.

To place a zero-pair of the NTF above zero frequency, two cascaded integrators with feedback can realize a resonator.

The oversampling ratio (OSR) means how much faster the analog signal is sampled, than what is given out from the digital decimation part. For a given sample frequency, with higher OSR, the signal band becomes smaller. That means that the bandwidth of the signal cannot be as large, but the NTF becomes more effective. Bandwidth is traded for accuracy.
To increase the signal frequency range, the sample frequency may be increased. Then components will have to work faster, forcing higher power consumption to still obtain the same accuracy. Obviously, there is also a limit for how fast components are able to work.

The excellent behaviour of the sigma-delta modulator makes it possible to reach very good signal-to-noise ratio (SNR) for a narrow-band signal, even with a quantization to two levels. In fact, sigma-delta ADC's with a 1-bit quantizer is commonly implemented, because of the simple implementation of both ADC and DAC. With quantization of more than one bit, non-linear behaviour of the DAC may occur. The design of the DAC has to be thoroughly done to minimize non-linearity, which can cause great degradation in SNR for the whole system.
With high OSR, the number of quantization bits can be made small, to still get good SNR out from the filtered and downsampled digital signal.

The trade-off between speed, accuracy and power consumtion is what will set requirements on the components in the sigma-delta modulator.
For low power one wants foremost to have low sample frecuency as well as OSR, to give the integrators good time to settle and thus small currents needed. But low modulator order and low number of quantiztion steps means few active components, thus low power consumption.
To get high SNR, one wants high OSR, high modulator order and many quantization levels.
For high speed, the OSR should be small, and the sampling frequency should be large.

If the wanted signal band is not the low-frequency band, band-pass sigma-delta A/D-conversion shoud be a good alternative. If the NTF is not high-pass shaped, but band-stop shaped, and the STF is well amplifying the frequencies of the NTF stop band, we have a band-pass sigma-delta ADC.

2.3 CRFB

The structure of a sigma-delta modulator (SDM) can be described by a signal flow graph (SFG). The cascade of resonators with distributed feedback (CRFB) [1] is the structure that will be discussed in this report.

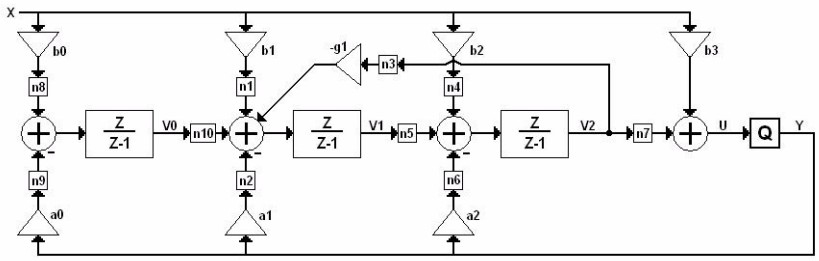

Figure 2.11: Third-order general CRFB SDM.

The SFG in Fig. 2.11 shows a general third-order CRFB modulator, in the Z-domain. The output *Y* is the quantized version of signal *U*. Interchanging the quantization with an addition of the quantization error makes it possible to calculate the NTF. Every box *n0* to *n10* can realize either a delay element or just interconnection. There are many possible realizations, still realizing a STF and NTF of third order.

The first integrator adds a zero placed in $z=-1$ in the Z-plane of the NTF. The other two integrators form a resonator, with adjustable zero placement, because of the feedback path through the multiplication with $-g1$.

An even-order CRFB structure, thus consisting of a number of resonators, can be realizing an NTF that suppresses noise at any wanted frequency band, depending of coefficients a_i and g_i. If all g_i are set to zero, all zeros of the NTF will be placed in $z=1$ in the Z-plane, thus the NTF will be purely high-pass shaped, i.e. low-pass sigma-delta modulation. To increase the signal pass-band and make the transition band of the NTF shorther, one might want g_i non-zero, moving zero-pairs through the unit circle in the Z-plane.

The STF depends on all coefficients a_i, b_i and g_i. Its zero-placement, though, is only dependent of the b_i coefficients. It is possible to find coefficients realizing the STF complementary to the NTF, or an all-pass STF. Both realizations are interresting choices.

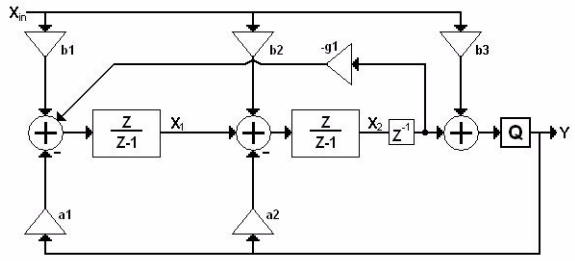

Figure 2.12: The example second-order SDM.

As an example througout the report, the structure of Fig. 2.12 will be considered. The modulator has one delay element in the resonator loop. If the *b3* coefficient is set to zero, the structure is fully symmetric and the implementation of the addition before the quantization is not needed. In the example, the *b3* coefficient will not be set to zero, to show how the implementation of the adder can be made.

2.4 ELECTRONIC COMPONENTS

The thesis is focused on the design of sigma-delta CRFB structure implemented in CMOS integrated circuits (IC). This means that the MOS transistor is the basic building block.
The analog filter realization is based upon the theory of switched-capacitor (SC) filters, consisting of switches, capacitors and operational amplifiers.

2.4.1 THE MOS TRANSISTOR

CMOS stands for complementary MOS, where MOS is short for MOSFET, that is metal oxide semiconductor field effect transistor. What is complementary, is that both NMOS and PMOS transistors are used. The NMOS transis-

tor operates best at low voltage levels, near ground, and the PMOS are better near the supply voltage.

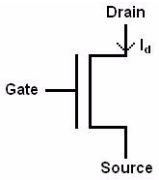

Figure 2.13: NMOS transistor. The potential is higher at drain than source.

The transistor can be seen as a voltage-controlled current source. The higher the gate-source voltage, the higher the current I_d, which flows from drain to source.

2.4.2 TRANSISTOR SWITCHES

The NMOS transistor can be used as a switch, that conducts when a high voltage is applied to its gate, and is non-conducting when a low voltage is applied to the gate. Similary, the PMOS transistor can be used, but with the inversed control signals, high gate potential for non-conducting, low for conducting.

The non-ideal MOS switch has non-zero on-resistance, and finite off-resistance. This means that when in conducting mode, some small voltage drop will appear over the swich, and in cut-off, a little leakage current will still flow through the component. The on-restance of the MOS transistors is potential dependent. For NMOS, the resistance is higher, the higher potential there is at the drain and source. The PMOS on-resistance is higher, the lower the potential.

By connecting an NMOS and a PMOS transistor in parallell one gets smaller and foremost less signal dependent on-resistance. This coupling is called the transmission gate. Depending on signal strength, the choice between simple NMOS or PMOS switch and transmission gate has to be decided for each individual design.

Unwanted effects in transistor switches can be thermal noise, leakage currents, charge injection, clock-feedthrough, flicker noise. Differential design, non-overlapping control signals and large loads suppresses noise.

2.4.3 OPERATIONAL AMPLIFIERS

The operational amplifier (OP-amp) is a differential amplifier that amplifies a signal highly from input to output. The device is used in circuits where negative feedback makes the closed-loop gain controllable. The higher the open-loop gain, the more accurate the closed-loop output signal.

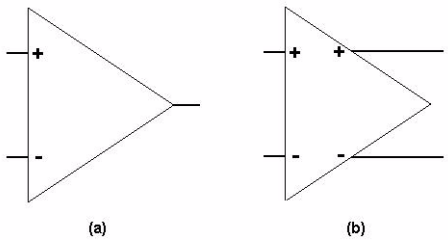

Figure 2.14: OP-amp symbols. a) Single-ended output. b) Differential output.

One source of amplifier is the voltage-to-voltage OP-amp, which is supposed to have very high input impedance, very low output impedance and very high voltage gain from input to output.

In applications with capacitive loads, the OP-amp can be constructed as a voltage-to-current amplifier, an operational transconductance amplifier (OTA). This device has high input as well as output impedance, and the transconductance should be large.

The OTA is the active component in SC-integrators, since it is the component that consumes current from the power supply. In low-power design, much consideration in the OTA design has to be taken.

When designing an OTA for minimum power consumtion, the following requirements have to be specified: DC-gain, unity-gain bandwidth, slew rate, common mode range, output range.

DC-gain usually refers to open-loop gain at zero frequency, the maximal open-loop gain. The unity-gain bandwidth is the frequency where the open-loop gain is unity.

If the OTA is to make fast transitions on its output, large currents are required. The slew rate is a measure of the maximum voltage change per unit time at the output. The slewrate is proportional to the supply current, and inversely

proportional to the load capacitance.

In differential design, the common-mode level (CM) defines the DC-level of the positive and negative signal.

Output range is an important factor when scaling voltage levels. The range between minimum and maximum output voltage of the OTA sets the output range. With differential output, the maximum output voltage is V_{max} - V_{min}, and the minimum becomes V_{min} - V_{max}, if the positive and negative output has the same limitations.

3

SCALING OF COEFFICIENTS

3.1 METHODOLOGY

When a SDM is being designed, an important step before realizing the circuit is to scale the inputs of the integrators so that the maximum output signal from the integrator can be realized according to the OTA's output range. It is very important to do this activity right since clipping in the integrators can reduce the SNR significantly.

3.1.1 INSERTION OF SCALE COEFFICIENTS

The idea of scaling is that all of the inputs to each integrator should be scaled by the same coefficient, and in order to fulfill the same transfer function of the SDM, the output of the integrator has to be scaled by the same factor. The output scaling factor cannot usually be realized within the current integrator, so the multiplication has to be passed on to the next integrator or, as a special case, to the next ADC. This particular issue will be discussed further in this chapter.

The second-order SDM is used as an example here and the modulator structure can be seen in Fig 3.1.

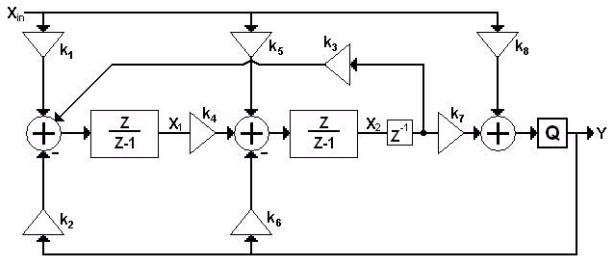

Figure 3.1: The second-order SDM.

Lets start by looking at the first integrator with the input coefficients k_1, k_2 and k_3. All of these coefficients shall now be scaled by a variable s_1 and, in order to preserve the transfer functions of the SDM, the output has to be scaled by $1/s_1$. The output scaling is realized with coefficient k_4, which is physically realized in integrator 2. The original values of the coefficient can be seen in column 1 and the resulting scaled coefficients can be seen in column 2 in table 3.1.

Coefficient	**1**	**2**	**3**
k_1	b_1	$b_1 s_1$	$b_1 s_1$
k_2	a_1	$a_1 s_1$	$a_1 s_1$
k_3	$-g_1$	$-g_1 s_1$	$-g_1 \frac{s_1}{s_2}$
k_4	v_1	$v_1 \frac{1}{s_1}$	$v_1 \frac{s_2}{s_1}$
k_5	b_2	b_2	$b_2 s_2$
k_6	a_2	a_2	$a_2 s_2$
k_7	v_2	v_2	$v_2 \frac{1}{s_2}$
k_8	b_3	b_3	b_3

Table 3.1. Scaling scenario of the modulator coefficients.

The next step is to scale the inputs and outputs of integrator 2. The scaling constant is here called s_2 and is inserted in the same way as with the first integrator. A special case is here that the output of integrator 2 also goes to the input with the coefficient k_3 of integrator 1, and this coefficient shall therefore also be scaled by $1/s_2$. The result of this can be seen in column 3 in table 3.1.

The last addition before the quantizer does not need to be scaled since it is directly connected to the quantizer. The quantizer cannot produce higher outputs than the highest reference level and the only thing that is required is therefore that these voltages can be produced.

The resulting SFG describing the second-order SDM with inserted scaling coefficients is now completely equvivalent to the original SFG. This can be shown by first calculating the transfer function of the SFG in Fig 3.1. The transfer function can be seen in equation (3.1).

$$H(z) = \frac{(k_8 z^2 - (2k_8 - k_7k_5 + k_8k_4k_3 - k_7k_4k_1)z + k_8 - k_7k_5)}{z^2 + (k_7k_6 - k_4k_3 + k_7k_4k_2 - 2)z + 1 - k_7k_6} \tag{3.1}$$

To be able to show that the transfer function of the SFG with scaled and unscaled coefficients are equal, one only needs to insert the coefficients from table 3.1 into equation (3.1). The unscaled coefficients can be found in column 1 and the scaled coefficients can be found in column 2.

$$H(z) = \frac{(b_3 z^2 - (-g_1b_3v_1 - b_1v_2v_1 + 2b_3 - b_2v_2)z + b_3 - b_2v_2)}{z^2 + (a_2v_2 + g_1v_1 + a_1v_1v_2 - 2)z + 1 - a_2v_2} \tag{3.2}$$

Both the scaled and the unscaled coefficients k_i results in the same transfer function, shown in equation (3.2), and this means that the scaled SFG's transfer function is equivalent to the original transfer function.

3.1.2 SCALING IN THE QUANTIZER

There exists SDM structures where there is no addition before the quantizer, which basically means that the scaling coefficient from the integrator, which is connected to the quantizer, must be realized within the quantizer. A good option is to scale the reference levels of the ADC by the scale constant of the last integrator and to still keep the output-voltages of the DAC the same. This can easily be done since the reference levels are produced by resistor nets and

will result in a gain in the quantizer by the inverse of the scaling factor of the reference levels.

3.2 SIMULATION

When insertion of scaling coefficients have been done one needs to set the coefficients s_1 and s_2. To be able to set the coefficients so that the integrators never reaches their maximum value one needs to simulate this model of the SDM with every possible input signal and this is of course not possible. A model suggested by [1] is to simulate the system with sinusoidal signals as inputs. The frequency of the input signal shall be varied over the whole pass-band of the modulator and the amplitude should be the maximum stable input-range. The value that overflows the most, according to the output range of the integrator, is the value which sets the scale coefficient s_i. A suggested way of simulating the system is to have the quantizer levels set to be symmetric around zero. The advantage of this is that one only has to look at the absolut value of the integrator output to find the maximum value.

In this simulation the maximum allowed input swing is 75% of the quantizer range, which is decided to be -1V to 1V. The modulator coefficients which is used can be seen in table 3.2.

Coefficient	**Value**
b_1	0.25
a_1	0.24
g_1	0.005
v_1	1
b_2	0.28
a_2	0.53
v_2	1
b_3	0.47

Table 3.2. Modulator coefficient values.

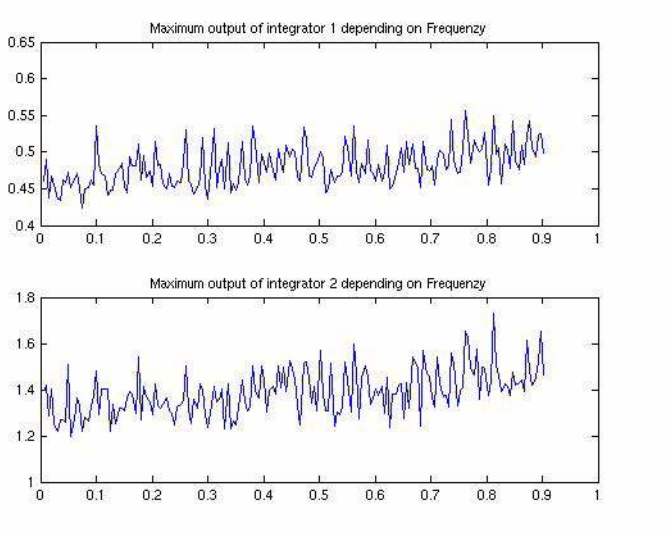

Figure 3.2: Maximum absolute value of the normalized output of the integrators plotted against normalized angular frequency.

One can see in Fig 3.2 that the maximum value at the output of the first integrator is 0.557 and the maximum value at the output of the second integrator is 1.729. The maximum output swing of the integrator is here supposed to be 1, and therfore the scale constant s_2 is supposed to be $s_2 = \frac{V_r}{1.729}$ and the scale constant s_1 is supposed to be $s_1 = \frac{V_r}{0.557}$. These coefficients are calculated according to equation (3.3) where V_r is the normalized maximum output swing of the integrator from V_{cm} and V_{out} is the maximum value at the integrator of index i.

$$s_i = \frac{V_r}{V_{out}} \tag{3.3}$$

The fact that s_1 is larger than one means that the output signal of the first integrator is upscaled and this feature means that thermal noise is moved from the input of the first stage to the input of the second stage. This will be discussed further in Chapter 5.

Another issue is that one here needs to decide the output range of the integrator V_r and this has to be estimated before building the OTA. If this estimation cannot be fullfilled, the only thing to do is to do the scaling all over again. However, if one want to use an OTA which already has been built, V_r can be

calculated according to equation (3.4). This parameter is usually smaller than one due to the fact that only a few OTA structures have the ability to drive the output voltage rail-to-rail.

$$V_r = \frac{min\{V_{out_{max}} - V_{cm}, V_{cm} - V_{out_{min}}\}}{min\{V_{DD} - V_{cm}, V_{cm} - V_{SS}\}} \tag{3.4}$$

3.2.1 OTA EXAMPLE

The OTA for which the scaling is supposed to be done has the parameters according to Table 3.3.

Parameter	Value
V_{DD}	3.3 V
V_{SS}	0 V
V_{cm}	1.65 V
V_{out_max}	2.9 V
V_{out_min}	0.3 V

Table 3.3. OTA parameters

The thing that needs to be done is to calculate the normalized maximum swing V_r, and this is done according to equation (3.5).

$$V_r = \frac{min\{V_{out_{max}} - V_{cm}, V_{cm} - V_{out_{min}}\}}{min\{V_{DD} - V_{cm}, V_{cm} - V_{SS}\}} = \frac{min\{2.9 - 1.65, 1.65 - 0.3\}}{min\{1.65, 1.65\}} = 0.818 \tag{3.5}$$

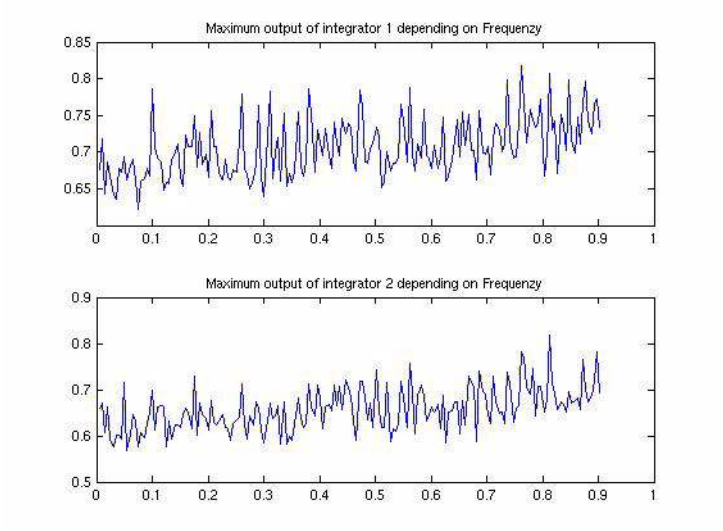

Figure 3.3: Maximum absolute value of the normalized output of the scaled integrators plotted against normalized angular frequency.

Fig 3.3 shows the normalized maximum values of the integrator outputs with scaled coefficients. Here V_r is set to 0.818, which means that the normalized output range of the integrators is -0.818 to 0.818. One can see that the output is never larger than 0.818, which means that the scaling has been done properly. The resulting coefficients after scaling can be calculated according to column 3 in table 3.1, where $s_1 = \frac{0.818}{0.577} = 1.469$ and $s_2 = \frac{0.818}{1.7291} = 0.47308$.

4

A METHOD FOR REALIZING CRFB SDM´S WITH SC-INTEGRATORS

4.1 INTRODUCTION

This chapter will guide the reader through the systematic design flow from a given CRFB modulator structure down to a circuit realization on a switched-capacitor filter level. The idea of this method is to move delay elements by equivalence transformations to get either whole or half delay into every integrator input, which directly gives the scheduling and the SC-realization. A special case in this theory is the addition before the quantizer, which has to be realized with no delay or half of a delay. This activity is suggested to be performed after the scaling of the given modulator has been done.

4.2 EQUIVALENCE TRANSFORMATIONS

To get a signal flow graph where all inputs to any integrator have either a whole or a half delay, and the inputs to the addition before the quantizer have either a half or no delay, one has to modify the original SFG by equivalence transformations.

4.2.1 RULES

Given a structure one is allowed to modify the difference equations as long as the result remains exactly the same. Timing of operations can be reordered by

a few rules. This is equivalent to moving delay elements in the SFG. When a signal passes through a component with one input and one output a delay element before the component is equivalent to a delay element after the component. When several signals are coupled together or a signal is split into several signals, equivalence transformations can be made as shown in Fig. 4.1 and Fig. 4.2.

The difference equations of Fig. 4.1:a gives the same bahaviour as the equations for Fig. 4.1:b.

$$u_3(n) = a \cdot u_1(n) + b \cdot u_2(n) \tag{4.1}$$

$$y_a(n) = u_3(n-1) = a \cdot u_1(n-1) + b \cdot u_2(n-1) \tag{4.2}$$

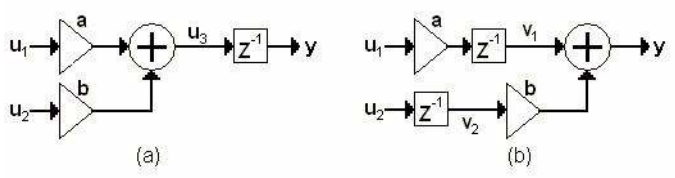

Figure 4.1: Equivalent SFG´s.

$$v_1(n) = a \cdot u_1(n-1) \tag{4.3}$$

$$v_2(n) = u_2(n-1) \tag{4.4}$$

$$y_b(n) = v_1(n) + b \cdot v_2(n) = a \cdot u_1(n-1) + b \cdot u_2(n-1) \tag{4.5}$$

Delay elements can be moved through nodes as shown in Fig. 4.2.

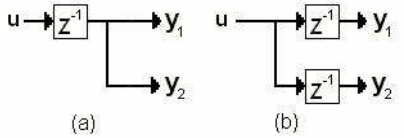

Figure 4.2: Equivalent SFG´s.

In this approach we also deal with movement of half-delays. This means that

it is allowed to transform the SFG´s of Fig. 4.1 and Fig. 4.2 into Fig. 4.3:a and Fig. 4.3:b, respectively.

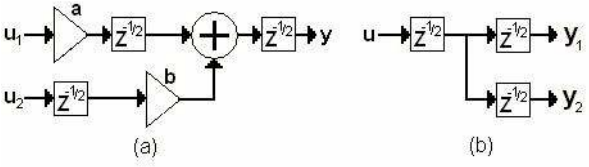

Figure 4.3: a) SFG equivalent to Fig. 4.1. b) SFG equivalent to Fig. 4.2.

As shown in section 4.4, half-delays as well as whole delays can be realized at any input to the swithed-capacitor integrators used to build the CRFB SDM, since the SC-integrators are utilizing two-phase clocking schemes.

It is also possible to realize integrator inputs without delay, but this will require an unnecessary long path to settle at one half period, and thus take longer time to settle, shown in section 4.5.6. Therefore this option is not to recommend.

4.2.2 METHOD

The task of equivalence transformations is to make sure there is either a full or half delay at every input to each integrator, which basicly means at every input to the adder before every integrator. This will give that two integrators never have to follow each other without some delay in between. In the SC realization, this means short paths to settle at a time, and gives good settling time constraints for the active components.

4.2.3 EXAMPLE: SDM2

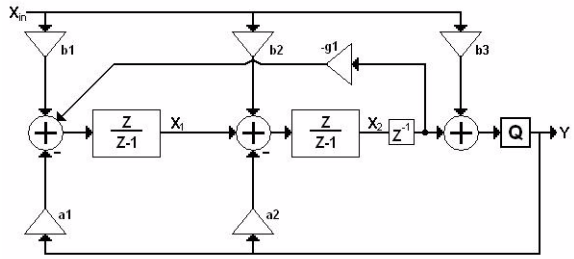

Figure 4.4: Original SFG of the second-order sigma-delta modulator.

The second-order sigma-delta modulator structure in Fig. 4.4 has one delay element after the second integrator. This can be moved back through the integrator and splitted into three delay elements at the inputs to the second integrator. Now take half the delay element that has appeared at the output of the first integrator, move back through the first integrator and split into three half-delays at the inputs to the first integrator. This gives the equivalent structure shown in Fig. 4.5.

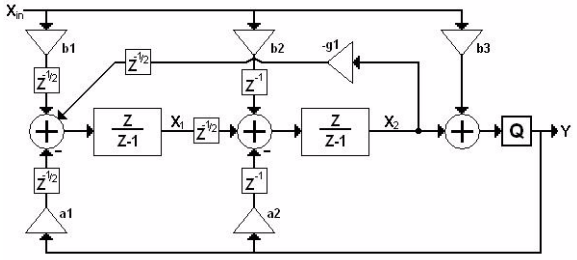

Figure 4.5: Transformed SFG of the second-order sigma-delta modulator.

4.3 SCHEDULING

The next thing to do after the transformation of the SFG is to make a proper schedule that later on can be implemented using SC-circuits. The most important thing to understand during this activity is how the notation in the schedule works, because the schedule is later on supposed to be translated directly into a SC-circuit.

4.3.1 DESCRIPTION OF THE SCHEDULE

The schedule, as can be seen in Fig. 4.6, is constructed of half clock periods since the SC-circuits is using a two-phase clocking scheme. A period in this schedule, which is t time units long, is referred to as a half period. This is due to the fact that one clock period is lasting 2τ time units. One can also see that the input signal X_{in} is stable over clock phase 1 and 2 and this is due to the fact that integrator 1 samples the input signal at time t and integrator 2 samples the input signal at time $t+\tau$. These two samples are supposed to be the same according to the model and if they are not, an error will be introduced. The drawback of this is that an external Sample & Hold circuit will be required to be able to hold the input signal stable during the time when the integrators sample the signal.

Another thing that is worth mentioning is that the times when the signals X_1 and X_2 appear in the schedule is when the output signal is stable at the output of the corresponding integrator. This can be seen by, for example, if we look at the signal $x_{in}(n)$ which can be seen at time t and then look at the delay until $x_1(n)$ is produced. $x_1(n)$ is the output of the first integrator in Fig. 4.5 and it seems to be outputted at the time $t+\tau$. This means that there is half a delay unit between the input X_{in} and the output of X_1, which it also is supposed to be according to the transformed SFG in Fig. 4.5. For example if there was a whole delay unit between the input X_{in} and the corresponding output X_1, the signal X_1 would appear in the schedule at time $t+2\tau$ if the input X_{in} where stable at time t.

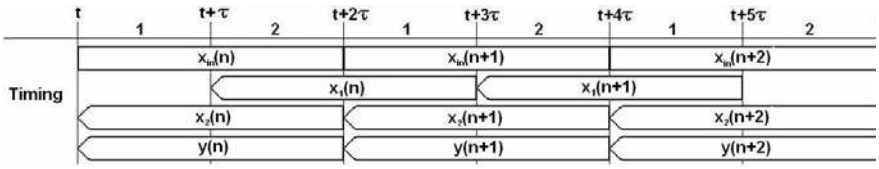

Figure 4.6: Schedule of the second-order sigma-delta modulator.

When it comes to the correct numbering of the samples, everything is related to the initial convention, that one needs to set up before one starts the scheduling. For example, if $x_{in}(n)$ is stable between time t and $t+2\tau$, the convention might be that every signal that starts either at time t or $t+\tau$, will be indexed as n and the signals that starts either at time $t+2\tau$ or $t+3\tau$ will be indexed $n+1$ and so on. The rule here is that the area where to index the signals n should be

two half periods, and the following two half periods should be indexed *n+1*.

The last thing to notice about the schedule is that the signals are drawn as blocks were the left edge is rounded. This is due to the fact that the output signals are not stable before the active blocks have settled, and this will be considered when building the circuit.

4.3.2 METHOD FOR SCHEDULING OF AN SFG

The methodology of scheduling is to start with the input signal which can be inputted at any time in the schedule. A good start is preferably to let $x_{in}(n)$ last between time t and $t+2\tau$, since this might be necessary if the integrators sample the input signal at different times. If it turns out that they do not, this requirement can be subscribed and it is then not necessary to have a Sample & Hold circuit in front of the sigma-delta modulator.

The next thing to do is to check the delay between X_{in} and X_1. If there is half a unit delay between these signals the correct thing is to schedule the X_1 signal to time $t+\tau$, which is one half of a clock period after X_{in} appears and index it as $x_1(n)$, since the signal starts at time $t+\tau$. If there is a whole unit delay between X_{in} and X_1 one shall schedule X_1 to start at time $t+2\tau$, which is one clock period after X_{in} appears. Due to the fact that the signal X_1 is scheduled one clock period later than X_{in}, it here should be indexed as $x_1(n+1)$. If we have several cascaded integrators the next step is to continue to schedule X_2, which is the output of the second integrator, from X_1 or X_{in} in the same manner as the first integrator. When the scheduling is done all the way from the input signal, through all of the integrators, to the quantizer the feedback paths are ready to be verified in the same way as when the signals were scheduled. The only difference is that the signals are already plotted in the schedule and one only needs to verify that the delay between the signals is correct.

4.3.3 EXAMPLE: SCHEDULING OF SDM2

The assignment here is to schedule the the second-order sigma-delta modulator shown in Fig. 4.5, transformed from the original SFG shown in Fig. 4.4.

The first thing to do is to schedule $x_{in}(n)$ to be stable between time t and $t+2\tau$. This means that $x_1(n)$ should be scheduled to appear one half of a clock period after $x_{in}(n)$ since there is half of a delay unit between X_{in} and X_1. This can be seen in Fig. 4.7.

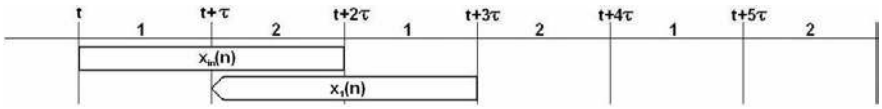

Figure 4.7: Start of the schedule of the second-order sigma-delta modulator.

The next thing to do is to is to schedule the X_2 signal. As we can see in Fig. 4.5 X_2 is delayed with one unit delay compared to X_{in} and with half of a unit delay compared to X_1. This means that we shall schedule X_2 to appear one clock cycle after X_{in} and a half clock cycle after X_1. This can be seen in the Fig. 4.8 and X_2 will here be indexed as $x_2(n+1)$ due to the fact that it appears at time $t+2\tau$, which is one whole clock cycle after $x_{in}(n)$ appears.

To finish this schedule we continue with the quantizer output. Since there is no delay between X_2 and the quantizer output we just schedule it at the same time as X_2. More thought will be put into the quantizer timing during the circuit design chapter. The last two operations of scheduling can be seen in Fig. 4.8.

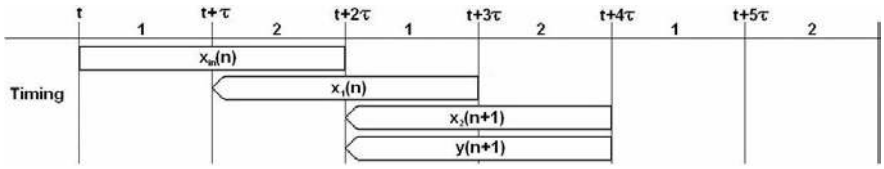

Figure 4.8: Allmost complete schedule of the second-order SDM.

The final step is to fill out the schedule with all of the samples and to check that the feedback paths are correct. The finished schedule can be seen in Fig. 4.9, where the arrows show which signals that have been used to produce a particular signal.

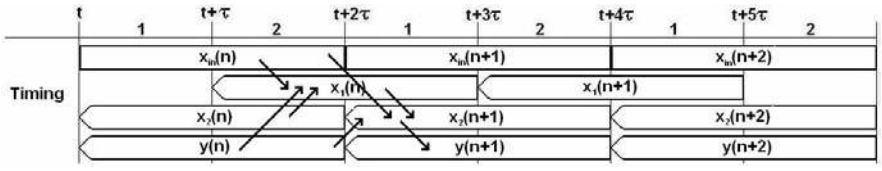

Figure 4.9: Complete schedule with arrows indicating were the signals are used.

4.4 SWITCHED-CAPACITOR CIRCUITS

To be able to build a circuit out of the schedule, one needs some knowledge about how to construct an SC-integrator with a specified number of inputs and outputs.

There are mainly two types of SC-circuits that are used when building sigma-delta modulators and both of these two standard realizations are insensitive to parasitic capacitors [2]. The first model is called non-inverting connection and the second one is called inverting connection.

These circuits are two-phase clocked, which means that two different, non-overlapping, trigger signals will be constructed out of the master clock. The first trigger signal will be high during the period were the master clock is high and the second trigger signal will be high during the period were the master clock is low. These two trigger-signals are called *P1a* and *P2a* and they can be seen in Fig. 4.10.

It is also needed to construct two additional trigger signals which are basicly the same as the two signals described above, but with the difference that they go low a little earlier than the previous trigger signals. These two signals will be called *P1a* and *P2a* and is used to end the integration phase before the input signal is removed from the input of the integrator. They can be seen in Fig. 4.10.

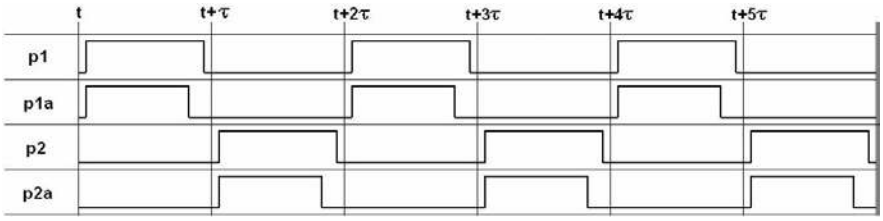

Figure 4.10: Timing diagram of trigger signals.

4.4.1 THE NON-INVERTING INTEGRATOR

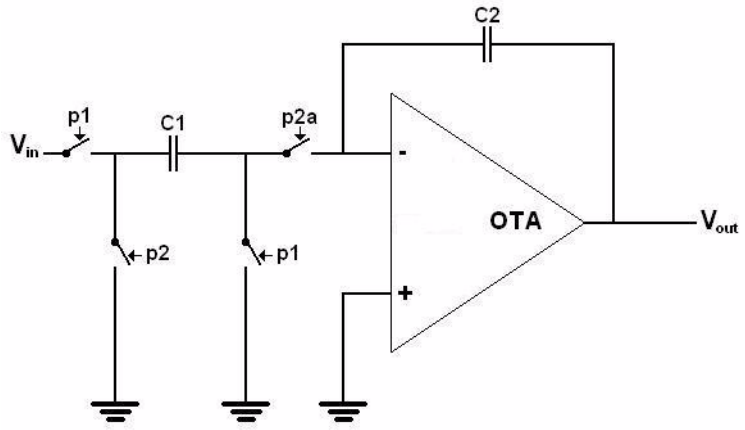

Figure 4.11: Integrator with one non-inverting input.

The non-inverting integrator as can be seen in Fig. 4.11 realizes an integration with a positive input and a unit delay. The switches that have *p1* as trigger are conducting in phase 1 and the switches triggered by *p2* is conducting in phase 2. The transfer function can be calculated from the following equations:

$$q_1(t) = -C_1 \cdot V_{in}(t) \tag{4.6}$$

$$q_2(t) = -C_2 \cdot V_{out}(t) \tag{4.7}$$

$$q_1(t+\tau) = 0 \tag{4.8}$$

$$q_2(t+\tau) = -C_2 \cdot V_{out}(t+\tau) \tag{4.9}$$

$$q_1(t+2\tau) = -C_1 \cdot V_{in}(t+2\tau) \tag{4.10}$$

$$q_2(t+2\tau) = -C_2 \cdot V_{out}(t+2\tau) \tag{4.11}$$

Charge conservation, which is due to the fact that we have an ideal OP-amp with no input current, gives:

$$q_1(t+\tau) + q_2(t+\tau) = q_1(t) + q_2(t) \tag{4.12}$$

$$q_2(t+2\tau) = q_2(t+\tau) \tag{4.13}$$

Equations (4.6), (4.7) (4.8), (4.11), (4.12) and (4.13) give

$$C_2 \cdot V_{out}(t+2\tau) - C_2 \cdot V_{out}(t) = C_1 \cdot V_{in}(t) \tag{4.14}$$

Since 2τ corresponds to one clock period, we can rewrite equation (4.14) as:

$$C_2 \cdot V_{out}(n+1) - C_2 \cdot V_{out}(n) = C_1 \cdot V_{in}(n) \tag{4.15}$$

The last step of this is to use the Z-transfrom on equation (4.15), which gives:

$$V_{out}(z) = \frac{C_1}{C_2} \cdot \frac{1}{z-1} \cdot V_{in}(z) = \frac{C_1}{C_2} \cdot \frac{z^{-1}}{1-z^{-1}} \cdot V_{in}(z) \tag{4.16}$$

Equation (4.16) corresponds to an integrator of the same type as the picture above shows, with one positive input which is scaled by C_1/C_2. The most important thing to remember about the non-inverting integrator is that the input signal is collected during the first phase of the integrator which often is referred to as the sampling phase. This integrator is not sensitive to an input signal which is unstable, as long as all of the integrators that use the same signal sample it at the same time.

4.4.2 THE INVERTING INTEGRATOR

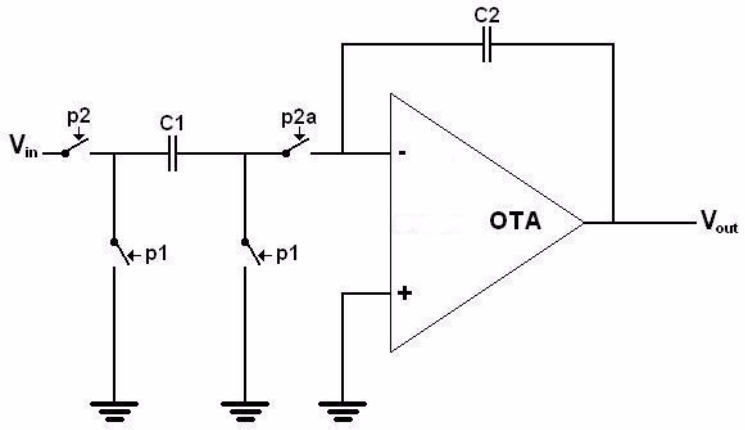

Figure 4.12: Integrator with one inverting input.

The inverting integrator realizes an integration with a half unit delay with a negative input and the circuit realization can be seen in Fig. 4.12. The transfer function is calculated below:

$$q_1(t) = 0 \tag{4.17}$$

$$q_2(t) = -C_2 \cdot V_{out}(t) \tag{4.18}$$

$$q_1(t+\tau) = -C_1 \cdot V_{in}(t+\tau) \tag{4.19}$$

$$q_2(t+\tau) = -C_2 \cdot V_{out}(t+\tau) \tag{4.20}$$

$$q_1(t+2\tau) = 0 \tag{4.21}$$

$$q_2(t+2\tau) = -C_2 \cdot V_{out}(t+2\tau) \tag{4.22}$$

$$q_1(t+\tau) + q_2(t+\tau) = q_1(t) + q_2(t) \tag{4.23}$$

$$q_2(t+2\tau) = q_2(t+\tau) \tag{4.24}$$

Equations (4.17), (4.18), (4.19), (4.22), (4.23) and (4.24) give

$$C_2 \cdot V_{out}(t+2\tau) - C_2 \cdot V_{out}(t) = -C_1 \cdot V_{in}(t+\tau) \tag{4.25}$$

$$C_2 \cdot V_{out}(n+1) - C_2 \cdot V_{out}(n) = -C_1 \cdot V_{in}\left(n+\frac{1}{2}\right) \tag{4.26}$$

$$V_{out}(z) = -\frac{C_1}{C_2} \cdot \frac{z^{1/2}}{z-1} \cdot V_{in}(z) = -\frac{C_1}{C_2} \cdot \frac{z^{-1/2}}{1-z^{-1}} \cdot V_{in}(z) \tag{4.27}$$

Equation (4.27) corresponds in this case to an integrator which is delayed by half of a unit delay with a negative input. The important thing to think about when using an inverting input to your integrator is that the input signal have to be as stable as possible to get a good result. An unstable input signal will greatly affect the settling time of the circuit.

4.4.3 DESIGN OF A DESIRED SC-INTEGRATOR

As shown in this chapter, one can design with both inverting integrators and non-inverting integrators. The next step now is to learn how to combine these two types of integrators to a new integrator with a number of non-inverting inputs and another number of inverting inputs. At first one must look at the difference between the two different types of integrators described in the text above.

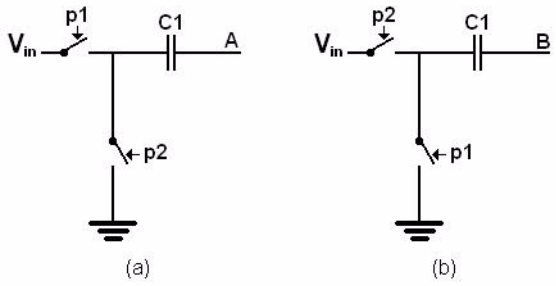

Figure 4.13: a) Non-inverting input. b) Inverting input.

If we compare the two figures that describe the circuit realizations of the non-

inverting (Fig. 4.11) and inverting (Fig. 4.12) integrators, one can see that the only thing that differs between them is the two switches to the left of capacitor C_1. This means that we can start with a standard non-input integrator as the one presented in Fig. 4.14 and connect either non-inverting or inverting inputs to it. This is done by connecting one or more of the input circuits shown in Fig. 4.13 to node C in the circuit shown in Fig. 4.14.

For example if we connect node A and node B of the circuits in Fig. 4.13 to node C of the circuit of Fig. 4.14 we will achieve an integrator with one inverting input and one non-inverting input. This example is studied in section 4.4.5. If we later want to expand this integrator with even more inputs, it is just a matter of connecting another circuit of the ones shown in Fig. 4.13 to node C of the integrator.

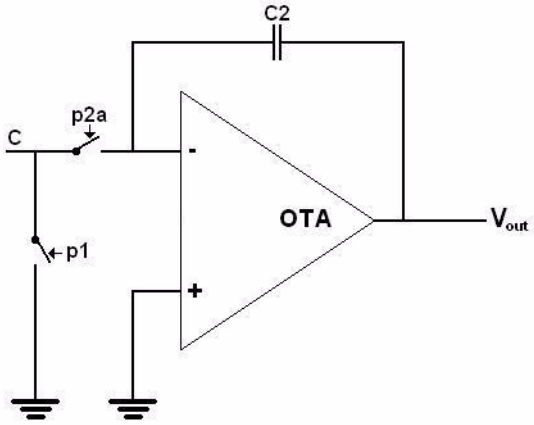

Figure 4.14: The general SC-integrator structure.

4.4.4 EXAMPLE: SWITCH CONFIGURATION FOR AN SC-INTEGRATOR WITH TWO INPUTS

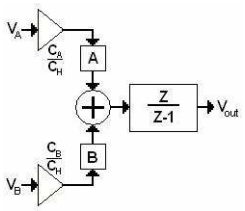

Figure 4.15: Two-input integrator SFG.

An integrator with two inputs, as the one in Fig. 4.16, with the SFG of Fig. 4.15, can be clocked in four ways making the inputs either delayed a full period or delayed half a period with negative sign.

Table 4.1 shows the proper switching for each case. '1' means that the switch is conducting during the phase of interest. Option 3 gives for example the transfer function $V_{out}(z) = \frac{1}{1-z^{-1}} \cdot \left(z^{-1} \frac{C_a}{C_H} V_a(z) - z^{-1/2} \frac{C_B}{C_H} V_B(z) \right)$.

	A	B	Phase	S_{A1}	S_{A2}	S_{B1}	S_{B2}	S_{samp}	S_{int}
1	z^{-1}	z^{-1}	Sample	1	0	1	0	1	0
			Integration	0	1	0	1	0	1
2	$-z^{-1/2}$	z^{-1}	Sample	0	1	1	0	1	0
			Integration	1	0	0	1	0	1
3	z^{-1}	$-z^{-1/2}$	Sample	1	0	0	1	1	0
			Integration	0	1	1	0	0	1
4	$-z^{-1/2}$	$-z^{-1/2}$	Sample	0	1	0	1	1	0
			Integration	1	0	1	0	0	1

Table 4.1. Different SC-integrator realizations.

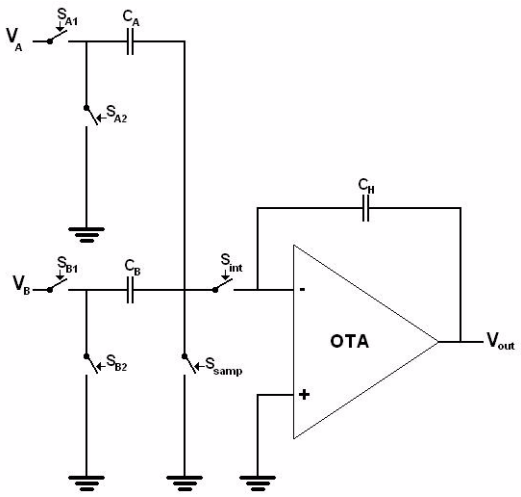

Figure 4.16: Two-input SC-integrator.

The discussion in this chapter has concerned single-ended SC-circuits. However, it is not difficult to realize a fully differential implementation of the same integrators. Fig. 4.22 shows an example of a fully differential SDM implementation.

In a differential implementation of the SC-integrators, an inverting input can be flipped to non-inverted by swiching place of the positive and negative input signal terminals. Similarly a non-inverting input can be flipped to an inverting. This makes it possible to change the sign of the input signal if it is required.

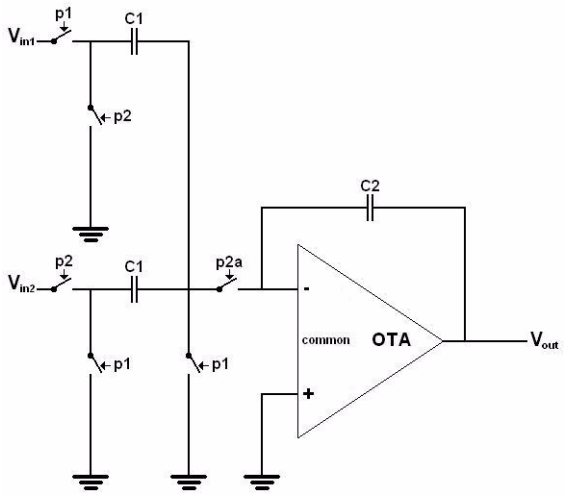

Figure 4.17: Integrator with one non-inverting and one inverting input.

4.4.5 EXAMPLE: SC-INTEGRATOR WITH ONE NON-INVERTING AND ONE INVERTING INPUT

The assignment here is to calculate the transfer function for a switched capacitor integrator with one inverting input and one non-inverting input according to Fig. 4.17. The first thing to do is to calculate the charge equations.

$$q_1(t) = -C_1 \cdot V_1(t) \tag{4.28}$$

$$q_2(t) = 0 \tag{4.29}$$

$$q_3(t) = -C_3 \cdot V_{out}(t) \tag{4.30}$$

$$q_1(t+\tau) = 0 \tag{4.31}$$

$$q_2(t+\tau) = -C_2 \cdot V_2(t+\tau) \tag{4.32}$$

$$q_3(t+\tau) = -C_3 \cdot V_{out}(t+\tau) \tag{4.33}$$

$$q_1(t+2\tau) = -C_1 \cdot V_1(t+2\tau) \tag{4.34}$$

$$q_2(t+2\tau) = 0 \tag{4.35}$$

$$q_3(t+2\tau) = -C_3 \cdot V_{out}(t+2\tau) \tag{4.36}$$

Charge conservation, due to the ideal OP-amp which means that no charge can be transported anywhere else than between the capacitors, gives

$$q_1(t+\tau) + q_2(t+\tau) + q_3(t+\tau) = q_1(t) + q_2(t) + q_3(t) \tag{4.37}$$

$$q_3(t+2\tau) = q_3(t+\tau) \tag{4.38}$$

Equations (4.28), (4.29), (4.30), (4.31), (4.32), (4.37) and (4.38) give

$$C_3 \cdot (V_{out}(t+2\tau) - V_{out}(t)) = C_1 \cdot V_1(t) - C_2 \cdot V_2(t+\tau) \tag{4.39}$$

Using the Z-transform on equation (4.39) gives

$$V_{out}(z) = \frac{C_1}{C_3} \cdot \frac{z^{-1}}{1-z^{-1}} \cdot V_1(z) - \frac{C_2}{C_3} \cdot \frac{z^{-1/2}}{1-z^{-1}} \cdot V_2(z) \tag{4.40}$$

As one can see, the resulting transfer function for this circuit corresponds to the added result of one non-inverting integrator (4.16) and one inverting integrator (4.27).

4.4.6 SWITCHED-CAPACITOR ADDERS USING COMPARATORS

When designing sigma-delta modulators, many structures require an addition just before the quantizer. This situation could appear as an addition of a reference level, which has to be subtracted in multibit sigma-deltas, or as a structural addition according to the design of the modulator. To be able to realize this addition, one could either choose to build an addition using one extra OTA or to use the comparator to realize the function. The later one can be realized since the fact that comparators have high input impedance, which means that nearly no charge dissapears into the input of the comparator and thereby that the equations of charge conservation is a good approximation of the real situation.

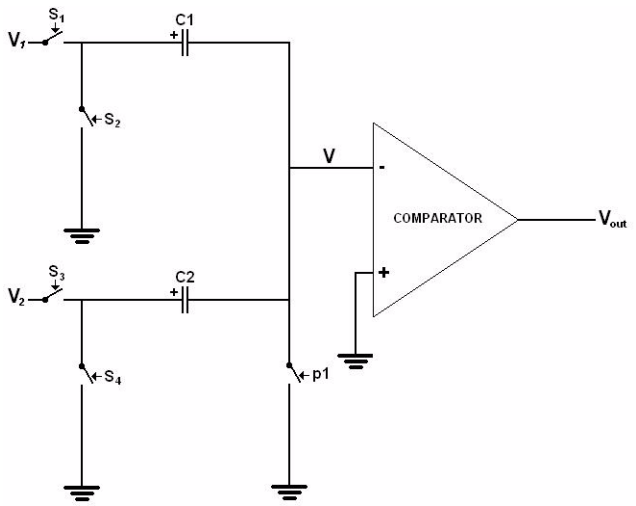

Figure 4.18: Implementation of two-input adder.

The first circuit is showed in Fig. 4.18 and the transfer function is calculated according to the equations below. The following example is calculated when S_1 is P1, S_2 is P2, S_3 is P2 and S_4 is P1. q_1 is the charge on capacitor C_1 and q_2 is the charge on capacitor C_2. The signs of q_1 and q_2 are defined according to Fig. 4.18.

$$q_1(t) = V_1(t)C_1 \tag{4.41}$$

$$q_2(t) = 0 \tag{4.42}$$

$$q_1(t+\tau) = -V(t+\tau)C_1 \tag{4.43}$$

$$q_2(t+\tau) = V_2(t+\tau)C_2 - V(t+\tau)C_2 \tag{4.44}$$

Charge conservation, due to the fact that the comparator is ideal and have infinitely high input impedance, gives equation (4.45)

$$-q_1(t) - q_2(t) = -q_1(t+\tau) - q_2(t+\tau) \tag{4.45}$$

Equation (4.41), (4.42), (4.43), (4.44) and (4.45) give:

$$-V_1(t)C_1 = -V_2(t+\tau)C_2 + V(t+\tau)(C_1 + C_2) \tag{4.46}$$

Since 2τ corresponds to one whole clock period, one can rewrite equation (4.45) and use the z-transform, which gives equation (4.47).

$$V(z) = V_2(z)\frac{C_2}{C_1+C_2} - V_1(z)z^{-1/2}\frac{C_1}{C_1+C_2} \tag{4.47}$$

This means that this particular circuit implements a SC-adder where input V_2 is not delayed and input V_1 is delayed by half a clock period. Worth noticing here is that the output of this adder will be scaled and this has to be considered when designing the forthcoming analog-to-digital converter.

S_1	S_2	S_3	S_4	**TRANSFER FUNCTION**
P1	P2	P1	P2	$V(z) = -V_1(z)z^{-1/2}\frac{C_1}{C_1+C_2} - V_2(z)z^{-1/2}\frac{C_2}{C_1+C_2}$
P2	P1	P2	P1	$V(z) = V_1(z)\frac{C_1}{C_1+C_2} + V_2(z)\frac{C_2}{C_1+C_2}$
P2	P1	P1	P2	$V(z) = V_1(z)\frac{C_1}{C_1+C_2} - V_2(z)z^{-1/2}\frac{C_2}{C_1+C_2}$

Table 4.2. Transfer functions given by trigger signals.

Table 4.2 shows the transfer functions according to the trigger signals inserted to the switches triggered by S_1, S_2, S_3 and S_4 in Fig. 4.18. According to this one can choose to implement this adder with either two half-delaying inputs, two non-delaying inputs or one delaying input and one non-delaying input. Worth mentioning here is that when building a sigma-delta modulator, there must be a half of a delay where the input signal to the modulator is fed into this adder, since this is the only way of sampling the signal. If there is not, one will need a separate Sample & Hold circuit before the modulator to hold the signal steady.

What needs to be understood when using this circuit is that it will scale the input and this is because of the way that the coefficients are realized. The input coefficients *a'* and *b'* are realized according to equation (4.48) and equation (4.49).

$$a' = \frac{C_1}{C_1+C_2} \tag{4.48}$$

$$b' = \frac{C_2}{C_1 + C_2} \tag{4.49}$$

Equation (4.48) and equation (4.49) give equation (4.50).

$$a' + b' = 1 \tag{4.50}$$

In order to estimate the scale constant k, one has to set a' and b' in relation to the wanted coefficients a and b. This can be seen in equation (4.51) and equation (4.52).

$$a' = k \cdot a \tag{4.51}$$

$$b' = k \cdot b \tag{4.52}$$

The value of the scale constant k is given according to equation (4.54).

$$k \cdot (a + b) = 1 \tag{4.53}$$

$$k = \frac{1}{a + b} \tag{4.54}$$

So in order to use this circuit, the quantizer must have a gain of k. Since the capacitor C_1 is known, the capacitor C_2 can be calculated according to equation (4.55).

$$C_2 = \frac{C_1 kb}{1 - kb} \tag{4.55}$$

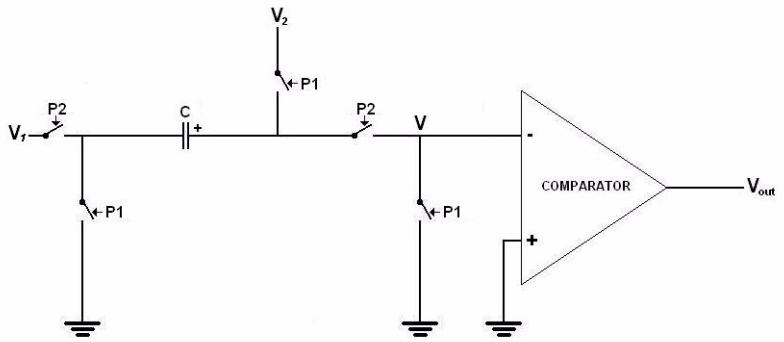

Figure 4.19: Implementation of two-input adder.

The next circuit which is proposed is described in Fig. 4.19 and the transfer function is calculated according to the equations below. q is the charge on capacitor C and the sign of q is defined by Fig. 4.19.

$$q(t) = CV_2(t) \tag{4.56}$$

$$q(t+\tau) = (V(t+\tau) - V_1(t+\tau))C \tag{4.57}$$

The rule of charge conservation gives:

$$q(t+\tau) = q(t) \tag{4.58}$$

Equation (4.56), (4.57) and (4.58) gives:

$$(V(t+\tau) - V_1(t+\tau))C = V_2(t)C \tag{4.59}$$

$$V(z) = V_1(z) + V_2(z)z^{-1/2} \tag{4.60}$$

This stucture implements an SC-adder with two inputs, where one of them is delayed by half of a clock period and the other one is non-delayed. The advantage of this structure, compared to the one presented in Fig. 4.18, is that we will save a capacitor. The disadvantage is that both of the inputs is just multiplied with factor one and added, which means that this structure is most suitable for subtracting already constructed reference levels when dealing with multibit ADC's.

To be able to use these two structures to its limit, one should implement them as fully differential implementations. This makes it possible to multiply any of the inputs to these adders with a factor of minus one which gives you full flexibility to construct any adder or subtractor with no or half of a clock cycle delay at the inputs.

4.5 FROM SCHEDULE TO CIRCUIT

4.5.1 METHOD TO CONSTRUCT A CIRCUIT FROM A SCHEDULE

We are now going to present the method to transform a schedule to a circuit realization. The most important thing during this activity is to have a full understanding for the notation in the schedule.

The first thing to know about the schedule, for example in Fig. 4.6, is that only the outputs from the active blocks in the SFG are printed. For example, if X_1 is the output of the first integrator, the time when the output appear in the schedule is when the integrator enters its integration phase. The integration phase then lasts for the whole half period from time $t+n\tau$ until $t+(n+1)\tau$. The output signal will remain stable for the following half period $t+(n+1)\tau$ until $t+(n+2)\tau$ and this is during the sample period of the integrator.

This means that in the cases when there is only one half of a unit delay between two signals in the schedule, one is able to decide which period to clock the signal into the next stage. For example, if there is one half unit delay between signal X_1 and X_2, we can choose either to input X_1 to the integrator which creates X_2 in integrator 2's sample phase or integration phase since the signal X_1 ideally is stable in both of these phases. The only difference is that if we input the signal X_1 in the integration phase of integrator 2 the signal X_1 will be inverted, and in the same way not inverted if one choose to input the signal in integrator 2's sample period. This particular issue will be discussed further later in this report.

The second thing to consider when using this method is that it does not fulfill the signs of the original SFG. Since most sigma-delta modulators designs are fully differential this is not a big issue. The solution is then to change the positive input signal for the negative input signal and the other way around. This

corresponds to multiplying the specific signal with -1. Another solution, especially when dealing with single-ended designs, is to adjust the circuit so that all of the inputs to the integrators which are supposed to be negative is taken in the integrators integration phase. This is not always possible, which means that one may have to choose another modulator structure which differs from the first design by a few unit delays.

The third thing to consider is the quantizer. If some kind of latched ADC is going to be used, one needs to be very careful when designing the clocking scheme for the circuit since the output of the quantizer is not stable during a whole clock period. This has to be taken in account when setting the trigger signals for the addtion which is before the quantizer.

To illustrate the method in a good way, we are going to use the second-order sigma-delta modulator, which have been used throughout this chapter to illustrate the different design steps.

4.5.2 EXAMPLE: SDM2 SC REALIZATION

The schedule in Fig. 4.6 is the schedule corresponding to the second-order SDM which SFG is shown in Fig. 4.5, transformed from the original SFG in Fig. 4.4.

The first thing to observe in the schedule is that the input signal X_{in} is stable between time t and time $t+2\tau$. This is an initial assumption which can be revised if it turns out that all of the integrators sample the input signal at the same time, which means that an external S&H circuit before the sigma-delta modulator will not be needed. One can also see that the integrator which produces X_1 starts its integration phase at time $t+\tau$, which means that we can choose to connect X_{in} to the integrator in the sample phase or the integration phase. The one to prefer is to connect X_{in} into the sample phase because this way does not require the signal to be stable. This is also the only way if one would like to avoid a Sample & Hold circuit at the input of the modulator.

The first step is then accomplished by connecting X_{in} into the first integrators sampling phase and let integrator 1 have its integration phase during phase 2 in the schedule.

The next step is to set the right clocks to the right switches in the second inte-

grator, which produces X_2. This is delayed one half clock cycle compared to X_1, which means that it shall be clocked on the opposite phase of the integrator which produces X_1. This is done to fulfill the requirement that X_2 should appear at the output of integrator 2 one half clock cycle after X_1 appears. It means that this integrator shall have its integration phase during phase 1 in the schedule.

When it comes to deciding in which period of integrator 2 X_1 shall be inputted, one can choose either to input the signal in the sample phase or the integration phase of integrator 2. In this case we choose, for purposes of the example, to input the signal in the integrating period of the integrator. It is here necessary to interchange the input wires to get the correct sign according to the SFG, since an inverting input produces the input multiplied by -1, and this has been illustrated in Fig. 4.21 as a mutiplication with the factor -1.

When it then comes to the input X_{in} to integrator 2, one can see that X_{in} is delayed with a whole clock period compared to X_2. This means that the way to realize this connection is by inputting it into the sample phase of integrator 2. One can now realize that integrator 2 samples X_{in} t time units later than integrator 1 and a Sample & Hold circuit at the input of the modulator is therefore required.

Now it is time to realize the addition between integrator 2 and the quantizer and since there are no delay elements at the input of this addition it would be good to use the first model with no delays which is described in chapter 4.4.6. The way to choose the trigger signals for this circuit is to perform the addition during the first phase were X_2 is stable, since there is no delay between X_2 and Y, which means that Y has to be stable at least during the later phase when X_2 is stable. This can been seen in Fig. 4.20 where the output of the this addition has been called X_3.

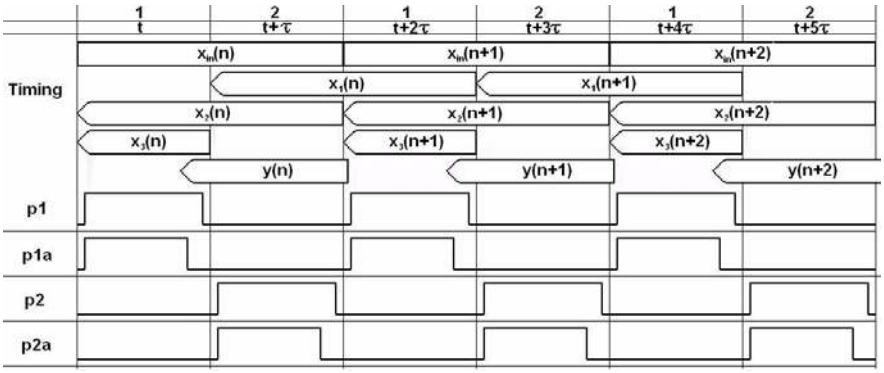

Figure 4.20: Modified schedule with trigger signals and signal X_3.

The next step, before we construct the feedback paths, is to connect the quantizer to the circuit. The way of constructing the circuit can differ a little bit depending on the choice of quantizer, but here it is assumed that the quantizer is a latched comparator were the output signal appears on the negative edge of the trigger signal P1a. This is because of the fact that signal X_3 needs to be stable when latching the quantizer and this can be seen in Fig. 4.20, as signal *y(n)* appears when signal $x_3(n)$ is stable.

It is now time to check the feedback paths and it is proper to start by checking integrator 1. One can see in Fig. 4.9 that the quantizer output *y(n)* has to be inputted to produce $x_1(n)$ in the integration phase of integrator 1 since the output of the latched quantizer is then stable. This also means that the sign of the input will be correct.

For signal $x_2(n)$ which is used to create $x_1(n)$ one can choose to either input the signal in the integration phase or in the sampling phase of integrator 1. Here it is proper to input the signal $x_2(n)$ into integrator 1 in the integration phase due to the fact that this will mean that integrator 2 will experience a smaller load during its integration phase. This connection also fulfills the sign conventions of the SFG.

The last step is to connect *y(n)*, which is the delayed and quantized version of X_2, to integrator 2. Here we can see that the only solution is to connect it into integrator 2's sampling phase. The sign specified of this input according to the

SFG is in this case not fulfilled and it is therefore needed to interchange the differential input wires.

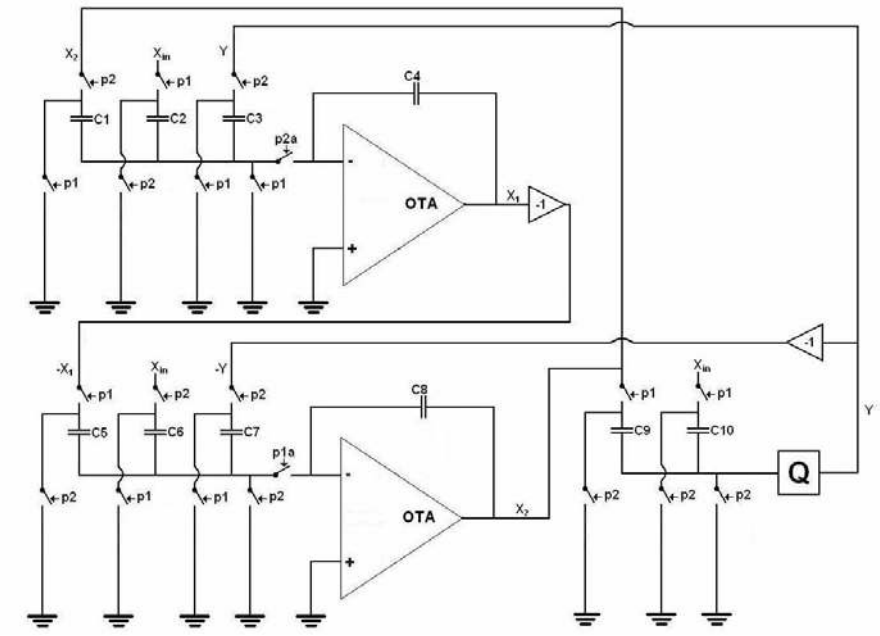

Figure 4.21: Single-ended version of the sigma-delta modulator.

The fully differential version of the circuit presented in Fig. 4.21 is presented in Fig. 4.22.

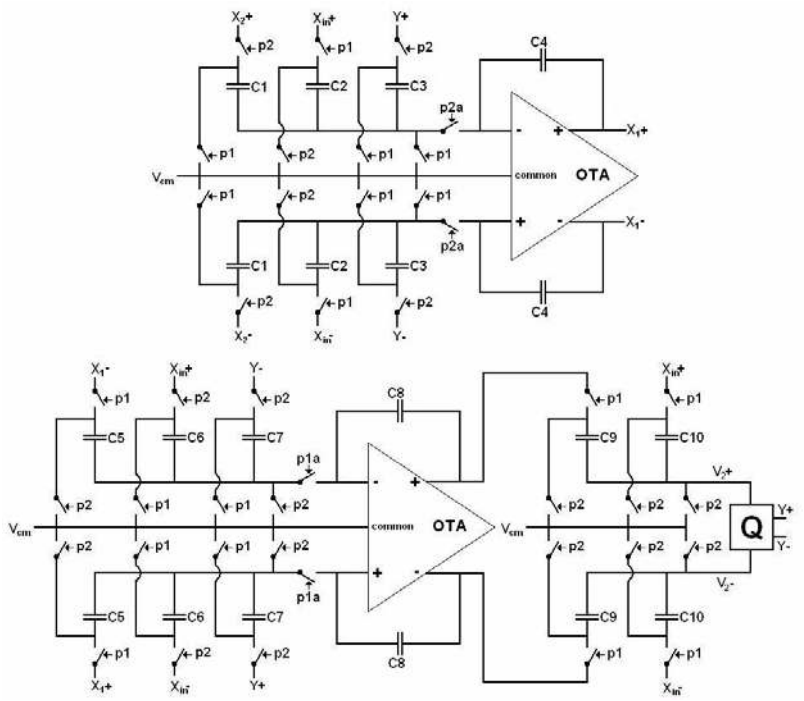

Figure 4.22: Circuit implementation of the second-order sigma-delta modulator.

4.5.3 FURTHER DISCUSSION OF ALTERNATIVES IN CASE OF HALF UNIT DELAYS

In the case when there is a half unit delay between two output signals there are, as stated in the text above, two possible choices of realization. The first one is to sample the signal in the sample phase of the integrator and the second one is to connect the signal into the integration phase of the integrator. Here we will try to explain the difference between the use of these two ways of interconnection by setting up a one pole model of each settling senario.

The model of the integrator with a non-inverting input is shown in Fig. 4.23 and the model of the integrator with one inverting input is shown in Fig. 4.24.

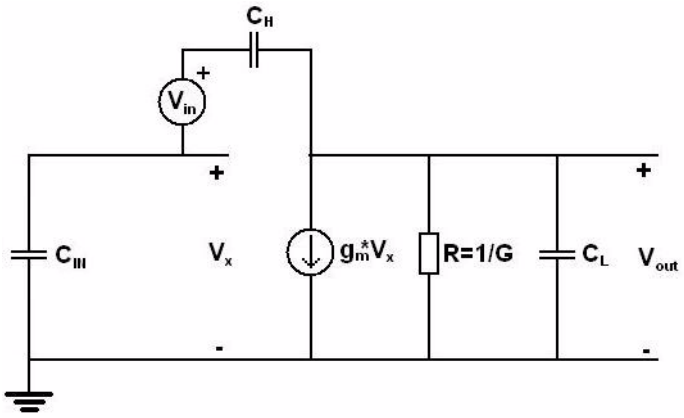

Figure 4.23: Model of the settling scenario for the non-inverting integrator.

To be able to fully analyze the two given situations, we need to calculate the step responses of the two circuits. This is done according to the calculations below.

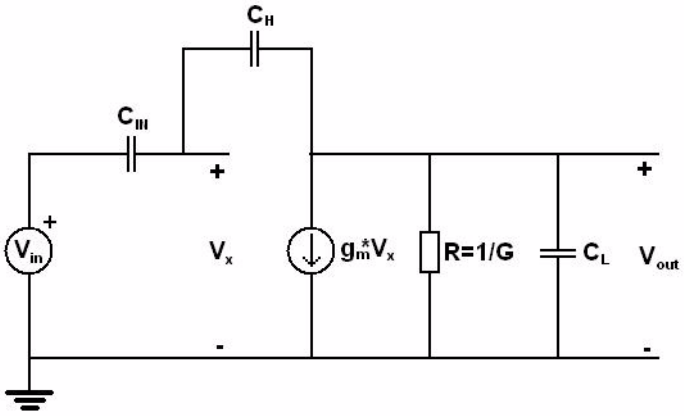

Figure 4.24: Model of the settling scenario for the inverting integrator.

4.5.4 STEP RESPONSE FOR THE INTEGRATOR WITH ONE INVERTING INPUT

$$V_x(s) = \frac{sC_{in} \cdot V_{in}(s) + sC_h \cdot V_{out}(s)}{sC_{in} + sC_h} \tag{4.61}$$

$$sC_h \cdot (V_x(s) - V_{out}(s)) = g_m \cdot V_{out}(s) + (G + sC_l) \cdot V_{out}(s) \tag{4.62}$$

$$V_{out}(s) = -\frac{(g_m - sC_h)C_{in}}{(C_{in} + C_h)G + g_m C_h + s(C_{in}C_h + C_{in}C_l + C_h C_l)} \cdot V_{in}(s) \tag{4.63}$$

It is assumed here that the term $(C_{in} + C_h)G$ is negligible, since *G=1/R*, where *R* is the output resistance of the OTA and are supposed to be large. If $V_{in}(t)$ is a step, the corresponding $V_{in}(s) = \frac{1}{s}$, which gives equation (4.64).

$$V_{out}(s) = -\frac{(g_m - sC_h)C_{in}}{g_m C_h + s(C_{in}C_h + C_{in}C_l + C_h C_l)} \cdot \frac{1}{s} \tag{4.64}$$

$$= -\frac{C_{in}C_h}{C_{in}C_h + C_{in}C_l + C_h C_l} \cdot \frac{s - \frac{g_m}{C_h}}{s + \frac{g_m C_h}{C_{in}C_h + C_{in}C_l + C_h C_l}}$$

The expression can be rewritten for convenient inverse Laplace transformation by the following rule:

$$\frac{1}{s} \cdot \frac{s+a}{s+b} = \frac{a/b}{s} + \frac{1 - a/b}{s+b} = \frac{a}{b} \cdot \left(\frac{1}{s} + \frac{b/a - 1}{s+b}\right) \tag{4.65}$$

$$V_{out}(s) = -\frac{C_{in}}{C_h} \cdot \left(\frac{1}{s} - \left(\frac{C_h^2}{C_{in}C_h + C_{in}C_l + C_h C_l} + 1 \right) \cdot \frac{1}{s + \frac{g_m C_h}{C_{in}C_h + C_{in}C_l + C_h C_l}} \right) \tag{4.66}$$

Inverse Laplace transformation gives

$$g_{inv}(t) = -\frac{C_{in}}{C_h} \cdot \left(1 - \left(\frac{C_h^2}{C_{in}C_h + C_{in}C_l + C_h C_l} + 1 \right) \cdot e^{-\frac{g_m C_h}{C_{in}C_h + C_{in}C_l + C_h C_l} \cdot t} \right), \; t \geq 0 \tag{4.67}$$

4.5.5 STEP RESPONSE FOR THE INTEGRATOR WITH ONE NON-INVERTING INPUT

$$sC_{in} \cdot V_x(s) = sC_h \cdot (V_{out}(s) - V_{in}(s) - V_x(s)) \tag{4.68}$$

$$sC_h \cdot (V_{in}(s) - V_x(s) - V_{out}(s)) = g_m V_x(s) + (G + sC_l) \cdot V_{out}(s) \tag{4.69}$$

$$V_{out}(s) = \frac{(g_m - sC_{in})C_h}{(C_{in} + C_h)G + g_m C_h + s(C_{in}C_h + C_{in}C_l + C_h C_l)} \cdot V_{in}(s) \tag{4.70}$$

As before we neglect $(C_{in} + C_h)G$. $V_{in}(t)$ is in this model equal to a step of the ratio between the input and hold capacitances, we insert $V_{in}(s) = \frac{C_{in}}{C_h} \cdot \frac{1}{s}$, and with similar approach as in the inverting case, the step response can be found.

$$V_{out}(s) = \frac{(g_m - sC_{in})C_h}{g_m C_h + s(C_{in}C_h + C_{in}C_l + C_h C_l)} \cdot \frac{C_{in}}{C_h} \cdot \frac{1}{s} \tag{4.71}$$

$$= \frac{C_{in}}{C_h} \cdot \left(\frac{1}{s} - \left(1 - \frac{C_{in}C_h}{C_{in}C_h + C_{in}C_l + C_h C_l}\right) \cdot \frac{1}{s + \frac{g_m C_h}{C_{in}C_h + C_{in}C_l + C_h C_l}} \right)$$

$$g_{inv}(t) = \frac{C_{in}}{C_h} \cdot \left(1 - \left(1 - \frac{C_h^2}{C_{in}C_h + C_{in}C_l + C_h C_l}\right) \cdot e^{-\frac{g_m C_h}{C_{in}C_h + C_{in}C_l + C_h C_l} \cdot t} \right), \; t \geq 0 \tag{4.72}$$

4.5.6 SIMULATION OF SETTLING WITH TWO CASCADED OTA'S

This simulation is done to be able to show that it is better to have at least half of a delay at every integrator input than to have no delay in between two integrators. The later case will lead to a situation where two cascaded OTA's have to settle in one half period. The simulation model is built of the one-pole OTA model shown in Fig. 4.24, here two of those have been cascaded. This means that the input voltage source of the second OTA has been replaced by the output of the first OTA. Two other simulations with the circuit shown in Fig. 4.24 and in Fig. 4.23 have also been done, with the exact same parameter values to show the differences between these three cases.

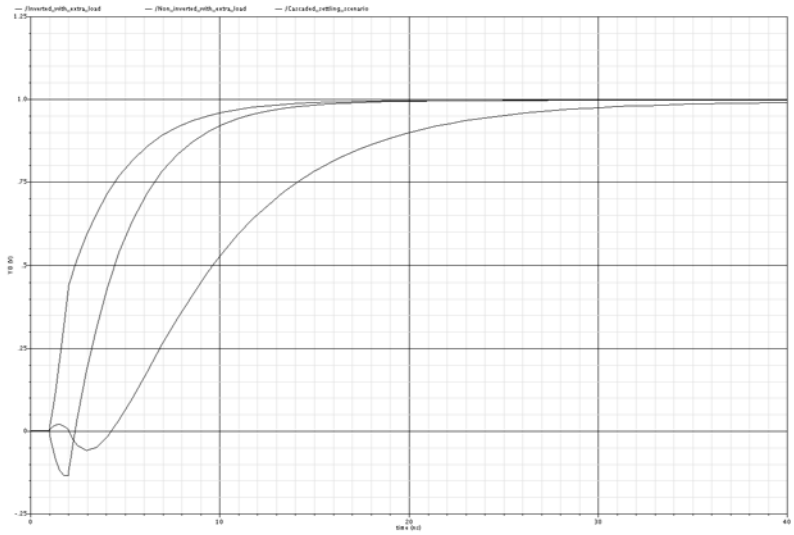

Figure 4.25: Simulated step response for non-inverted, inverted and cascaded SC-integrators.

The one of the three simulations that has the fastest settling time is the non-inverting integrator and it is followed by the inverting integrator, which settles nearly as fast if one is looking for a small settling error. The slowest settling time by far, is the system with the two cascaded OTA's, and that is why this case has been neglected in this report. Worth mentioning here is that, for the inverting integrator, the input step voltage has been adjusted to a negative step voltage for a better plot.

4.5.7 CONCLUSIONS

According to the the analytic expressions for the step responses of the settling scenarios for the inverting and non-inverting integrator, there is no clear answer to the question which circuit settles fastest. After analyzing some simulations with the same values of the constants, one could say that if the input and hold capacitances have the same value and the input capacitance of the second integrator is significantly bigger than the load capacitor of the first stage, it would be better to have an inverting input. Though, if there is no extra load capacitor at the output of the first integrator, it is much better to use a non-inverting input which samples the signal. This input is faster without any load and can accept an input signal which is not stable.

So finally the conclusion is to take the design issues of the OTA into account when choosing how to implement the circuit. If, for example, one knows that an uncompensated or lightly compensated OTA will manage to meet the requirements of the circuit, the capacitive load will be rather small and it would then in most cases be better to use the non-inverting input.

5

NOISE SOURCES IN SC SDM'S

The dominating noise sources of a differential SC-realization of a sigma-delta ADC are quantization noise, thermal noise and flicker noise. Quantization noise can be reduced by high oversampling ratio or modulator order, while thermal noise effects are reduced if large capacitor values are used or the signal power is strong. This gives a trade-off between speed, power consumtion and accuracy. Flicker noise can be prevented by special techniques.
The problem with clock-feedthrough and charge injection, that can occur in transistor switches, should be prevented by proper swich configuration. These and other noise sources, such as power supply noise and substrate noise, are well suppressed by differential design and can be included in a noise margin in estimations.

5.1 NOISE BUDGET

The obvious noise source of every ADC is the quantization noise. However, with the noise-shaping sigma-delta modulation this noise source is well controlled, and a proposal is that the thermal noise will be allowed to degrade SNR the most. The less one has to suppress thermal noise, the smaller capacitor values are needed. One wants to avoid unneccesarily large capacitor values, which otherwise would mean unneccesarily large chip area and slow circuits, or high power consumtion.

A proposed noise budget from[1] allows the thermal noise power to be 75% of the whole degradation of SNR, the quantization noise power to be only

5%, and then a good 20% margin for various additional noise sources. Aiming for this budget, given a SDM and a required SNR one can consider noise proportions as follows.

SNR is the signal-to-noise ratio, where the noise power sums up from its three sources, quantization noise, thermal noise and a noise margin.

$$SNR = \frac{P_S}{P_{N_{tot}}} \tag{5.1}$$

$$P_{N_{tot}} = P_{N_Q} + P_{N_T} + P_{N_M} \tag{5.2}$$

By simulating a mathematical model of the circuit one can get an SNR unaffected by everything but the quantization noise, i.e. the signal-to-quantization-noise ratio, SQNR. Now, the quantization noise power for the simulated circuit is given by

$$P_{N_Q} = \frac{P_S}{SQNR} \tag{5.3}$$

With the quantization noise being 5% of the noise budget, the total noise power will be 20 times the quantzation noise. If this holds to get the wanted SNR, thermal noise power can be allowed to a quantity of 15 times the quantization noise.

With the quantization noise part of the total noise fixed to 5%, the SNR will be propotional to the SQNR, as

$$SNR = \frac{P_S}{20 \cdot P_{N_Q}} = \frac{SQNR}{20} \tag{5.4}$$

Since $10 \cdot {}^{10}log\frac{1}{20} = -13.0103$, the SNR in dB becomes

$$SNR_{dB} = SQNR_{dB} - 13 \tag{5.5}$$

The conclusion is that a margin of 13 dB has to be achieved when simulating the ideal circuit, if one wants to follow the proposed noise budget, where quantization noise is 5% of total noise. Otherwise the budget has to be modified in order to make the specific circuit reach the required SNR.

If the noise margin is supposed to be 20% of the total noise, the following expression for thermal noise power received from (5.2) will enable the proper

SNR:

$$P_{N_T} = P_{N_{tot}} - P_M - P_{N_Q} = 0.8P_{N_{tot}} - P_{N_Q} \tag{5.6}$$

EXAMPLE

Assume that the required SNR is 60 dB, i.e. 10^6 times more powerful signal than noise. The signal swing of the circuit is 0 to 3.3 V but differential, which gives a full-swing signal of -3.3 to 3.3 V, i.e. maximum amplitude of 3.3 V. The system is fed with a sinusoidal input with 61% of full-swing. The signal power is

$$P_S = \frac{(3.3 \cdot 0.61)^2}{2} \approx 2 \ [\mathrm{V}^2] \tag{5.7}$$

Desired SNR is reached if total noise is no more than

$$P_{N_{tot}} = \frac{P_S}{SNR} = 2 \cdot 10^{-6} \tag{5.8}$$

Now, say the simulated SQNR reaches 70 dB. We know that this can not fulfill the budget where quantization noise is 5% of total noise, since SNR then would be $70 - 13 = 57$ dB. Still, a close enough distribution of noise sources can be made.

Power of the quantization noise is

$$P_{N_Q} = \frac{P_S}{SQNR} = 2 \cdot 10^{-7} \tag{5.9}$$

From (5.6), the maximum allowed thermal noise power will be

$$P_{N_T} = 0.8P_{N_{tot}} - P_{N_Q} = 0.8 \cdot 2 \cdot 10^{-6} - 2 \cdot 10^{-7} \approx 1.4 \cdot 10^{-6} \tag{5.10}$$

This results in a noise budget of 10% quantization noise, 70% thermal noise and 20% noise margin.

5.2 THERMAL NOISE

Thermal noise in MOS transistors causes a small variation in the drain current of the transistor, and can be modeled as a voltage source in series with the transistor, with power spectral density evenly spread over all frequencies, i.e., white noise. [2]

When analyzing transistor switches as in SC-integrators, one common assumtion is that the transistor can be replaced by a resistance during its conducting time period and open circuit during its non-conducting period. The resistance is called the on-resistance R_{on} and has the thermal noise voltage source in series. [5]

Thermal noise voltage of the on-resistance is white and have the power magnitude $4kTR_{on}$ $[V^2/Hz]$, where $k \approx 1.38 \cdot 10^{-23}$ $[J/K]$ is the Bolzmann constant and T is the absolute temperature of the device. This means that its power spectral density (PSD) is

$$S(f) = 4kTR_{on}\left[\frac{V^2}{Hz}\right] \tag{5.11}$$

5.2.1 EXAMPLE: THERMAL NOISE IN AN SC-INTEGRATOR [5]

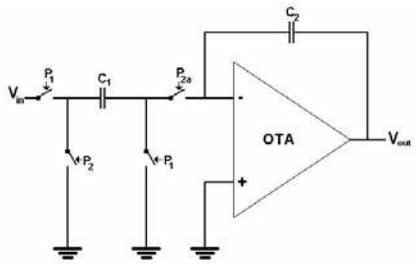

Figure 5.1: Non-inverting SC-integrator.

To study the noise effects in a SC-integrator, we shall follow calculations made in [5], for a single-ended integrator with one non-inverting input.

INPUT-REFERRED NOISE

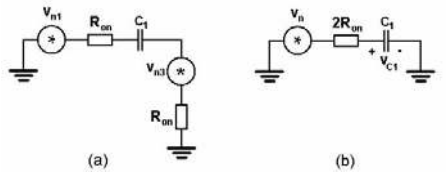

Figure 5.2: Noise analysis for the sample phase of a non-inverting integrator.

The thermal switch noise over the capacitor C_1 in Fig. 5.2:a has contributions from v_{n1} and v_{n3}, which are uncorrelated and thus may be added together to the equivalent noise voltage source v_n in Fig. 5.2:b. Assuming R_{on1} and R_{on2} are equal, the noise voltage across C_1 for the integrator's sample phase will be

$$V_{C1} = V_n \cdot \frac{1}{1 + j\omega \cdot 2R_{on}C_1}, \tag{5.12}$$

$$V_n = V_{n1} + V_{n3} = 2V_{n1} \tag{5.13}$$

If $S_{n,i}(f)$ is the PSD of noise voltage source i, and $H_i(f)$ is the expression for voltage over a certain capacitor originated from noise source i, the PSD across the capacitor is given as

$$S_C(f) = \sum_i S_{n,i}(f) \cdot |H_i(f)|^2 \tag{5.14}$$

Thus, the PSD of thermal noise over C_1 for the sample phase is found by the PSD of the equivalent noise voltage source v_n, multiplied by the magnitude response from source to C_1 in square.

$$S_{C1}(f) = 2 \cdot 4kTR_{on} \cdot \frac{1}{1 + (2\pi f \cdot 2R_{on}C_1)^2} \tag{5.15}$$

Integrating S_{C1} over all frequencies gives a mean-square value of the thermal noise over C_1, also referred to as the total noise power, for half the clock period.

$$\overline{v_{C1}^2} = 8kTR_{on}\int_0^\infty \frac{1}{1+(f\cdot 4\pi R_{on}C_1)^2}df \tag{5.16}$$
$$= 8kTR_{on}\cdot\left[\frac{\operatorname{atan}(f\cdot 4\pi R_{on}C_1)}{4\pi R_{on}C_1}\right]_{f=0}^{\infty} = \frac{2kT}{\pi C_1}\cdot\left(\frac{\pi}{2}-0\right)$$
$$= \frac{kT}{C_1}$$

The thermal noise over C_1 of the sample phase is thus independent on the switch resistances. The possible ways to suppress the noise are to keep temperature low, and foremost to chose a high value for the capacitance.

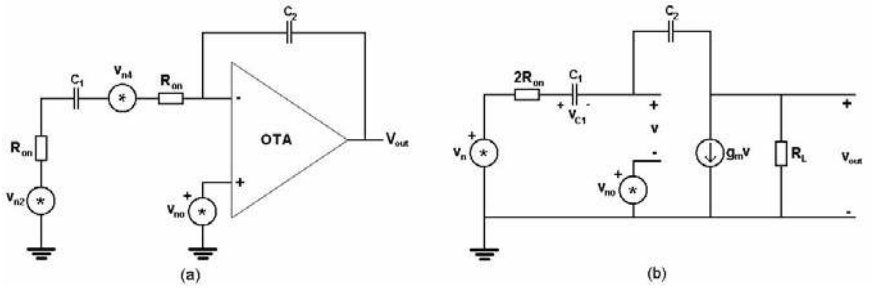

Figure 5.3: Noise analysis for the integration phase of a non-inverting integrator, with one-pole model of the OTA.

For the integrating phase, Fig. 5.3:a, the noise over C_1 depends also on thermal noise of transistors in the OTA. The switch thermal noise can again be combined to a common noise voltage source as in Fig. 5.3:b. One should know that the one-pole model of the OTA is a heavily simplified scenario, and even more simplification is now done by assuming $1/R_L = 0$. This is true for an ideal OTA, where R_L is infinitely large. R_L is supposed to be large, but to say it can be infinite is a rough approximation. With this assumption the current $g_m v$ flows through the switch-resistance and C_1.

$$g_m V = \frac{V_n - (V_{no} + V + V_{C1})}{2R_{on}} \tag{5.17}$$

$$g_m V = sC_1 \cdot V_{C1} \tag{5.18}$$

Elimination of V in (5.17) and (5.18) will give an expression for the noise voltage across C_1 for the integrating phase of the integrator:

$$V_{C1} = (V_n - V_{no}) \cdot \frac{1}{1 + s \cdot (2R_{on} + 1/g_m)C_1} \tag{5.19}$$

With this, the PSD of thermal noise over C_1 for the integration phase is given by

$$S_{C1}(f) = (8kTR_{on} + S_{no}) \cdot \frac{1}{1 + (2\pi f \cdot (2R_{on} + 1/g_m)C_1)^2} \tag{5.20}$$

Missing here is the PSD of the OTA thermal noise. This depends on the input stage of the OTA. The line of reasoning in [5] reaches the result that this noise mainly contributes from two transistors, if the input stage of the OTA is a differential pair. These are modelled with noise voltage sources with PSD $S = \frac{8}{3}kT/g_m$ at the gates. The PSD of the OTA thermal noise is then supposed to be

$$S_{no} = \frac{16kT}{3g_m} \tag{5.21}$$

Total noise power over C_1 for the integrating period is given by integrating (5.20) for frequencies zero to infinity:

$$\overline{v_{C1}^2} = \left(8kTR_{on} + \frac{16kT}{3g_m}\right) \cdot \frac{1}{4(2R_{on} + 1/g_m)C_1} = \frac{kT}{C_1} \cdot \left(\frac{1}{1 + \frac{1}{2R_{on}g_m}} + \frac{4/3}{1 + 2R_{on}g_m} \right) \tag{5.22}$$

One can see that if $2R_{on}g_m$ is large, that is, if $g_m \gg 1/R_{on}$, then the switch noise become kT/C_1, and the OTA noise can be neglected. But if it is the other way round, if $2R_{on}g_m$ is small, the OTA noise will be most significant. In later calculations, $g_m \gg 1/R_{on}$ will often be assumed. This gives the least thermal noise for a given capacitor size, but requires sufficient large current throw the OTA.

Total thermal noise power of the whole clock period over C_1 adds together from the two phases:

$$\overline{v_{C1}^2} = \frac{kT}{C_1} \cdot \left(1 + \frac{1}{1 + \frac{1}{2R_{on}g_m}} + \frac{4/3}{1 + 2R_{on}g_m} \right) \rightarrow \frac{2kT}{C_1}, \; g_m \gg 1/R_{on} \tag{5.23}$$

What is done here, is that the input-referred thermal noise power in a circuit has been determined by the following procedure:

Define noise voltage sources, set other signals to zero and calculate expressions for noise voltages over a specific capacitance. From this PSD over the capacitance is found as the square of the absolute value of the voltage across the capacitance, where every noise voltage source in square corresponds to the PSD of that specific source. Integrating the PSD over frequencies from zero to infinity gives the total noise power.

When the circuit works in several phases, this derivation is done for each phase, and in the above case of a two-phase SC-integrator the contributions from each phase adds to each other, because the affected node right to the capacitor senses all noise of both phases.

OUTPUT-REFERRED NOISE

If we chose to determine total noise voltage on capacitor C_2 instead of C_1, the result would have been the output-referred noise voltage, determined by both capacitor C_1 and C_2. In [5], this result instead comes from the following discussion.

The mean-square thermal noise voltage from (5.23) corresponds to a mean-square noise charge in C_1 of

$$\overline{q_{C1}^2} = \overline{v_{C1}^2} \cdot C_1^2 \rightarrow 2kTC_1, \; g_m \gg 1/R_{on} \tag{5.24}$$

All noise charge also reaches C_2. The two capacitors senses same noise in the integration phase, where they are connected in series, and also the contribution from the sample phase is then transferred from C_1 to C_2. Thus, if the assumtion $g_m \gg 1/R_{on}$ is made:

$$\overline{q_{C2}^2} = 2kTC_1 \tag{5.25}$$

$$\overline{v_{C2}^2} = \frac{2kTC_1}{C_2^2} \tag{5.26}$$

Equation (5.26) shows the output-referred thermal noise power from one integrator input.

The gain of the integrator is determined by the quotient $a = C_1/C_2$, as shown in Chapter 4.4. If the output-referred noise power is divided by the gain in square, the input-referred noise power is again given. Equation (5.27) gives the same expression as (5.23).

$$\overline{v_{C1}^2} = \frac{2kTC_1}{a^2C_2^2} = \frac{2kT}{C_1} \tag{5.27}$$

MORE THAN ONE INTEGRATOR INPUT

If there are several inputs to the integrator, they all contribute with the approximate mean-square noise charge $2kTC_{1,i}$ for one whole period. The mean-square noise charge in the output capacitor becomes

$$\overline{q_{C2}^2} = \sum_i 2kTC_{1,i} \tag{5.28}$$

This means that the output-referred thermal noise power, assuming $g_m \gg 1/R_{on}$, will be

$$\overline{v_{C2}^2} = \frac{2kT}{C_2^2} \cdot \sum_i C_{1,i} \tag{5.29}$$

To instead refer this thermal noise power to one input, one have to divide it by the gain from that input to the output, $a_i = C_{1,i}/C_2$, in square. Equation (5.30) gives that the input-referred thermal noise voltage is only depending on temperature, the chosen input capacitor and the integrator's gain coefficients.

$$\overline{v_{C1,i}^2} = \frac{2kT}{a_i^2C_2^2} \cdot \sum_j C_{1,j} = \frac{2kT}{C_{1,i}} \cdot \sum_j \frac{C_{1,j}}{C_{1,i}} = \frac{2kT}{C_{1,i}} \cdot \sum_j \frac{C_{1,j}/C_2}{C_{1,i}/C_2} = \frac{2kT}{C_{1,i}} \cdot \sum_j \frac{a_j}{a_i} \tag{5.30}$$

It is possible to chose $C_{1,i}$ so that the maximum thermal noise power is not higher than allowed, and then fixed values for C_2 and other input capacitors are given. The higher the ratio $a_i = C_{1,i}/C_2$ is, the lower value for C_2 will be required for the circuit, given a value of C_1. Now, if it is possible to scale up the coefficient a_i, that will be desirable to minimize total capacitor size of the SC-integrator.

If the coefficient a_i is scaled up with S, it is the same as scale down C_2 by S.

$$a_{i,S} = a_i \cdot S = \frac{C_{1,i}}{C_2 \cdot \frac{1}{S}} \tag{5.31}$$

In sigma-delta modulators of order higher than one, the first integrator is the most critical one in aspect of thermal noise. This is due to the noise-shaping nature of the modulator, and will require the input capacitors of the first integrator to have larger value than any other capacitors, from noise view. Therefore, if one can scale up the capacitor ratios in the first integrator, and then scale down the capacitor ratios in the next integrator, one get smaller value for the capacitor C_2 in the first integrator, and thus save chip area. One instead will get larger values for the capacitor ratios in the second integrator, but here the input capacitors can be much smaller than in the first integrator, and the total capacitance quantity will be smaller.

5.2.2 GENERAL METHOD FOR THERMAL NOISE ESTIMATION

The procedure described for calculating noise in an SC-circuit is a general method, that can be as accurate as needed, depending on how many noise sources one includes.

For each phase of the period, the circuit is drawn with on-resistances instead of conducting switches, and open circuits instead of non-conducting switches. The operational amplifier has to be replaced by, for example, a one-pole model. Of course, more sophisticated is the two-pole model, but also harder to work with. Equivalent noise voltage sources are inserted in the circuit, other input signals are set to zero.

Now an expression for the voltage over the desired capacitor is determined. If the chosen capacitor is the hold capacitor, the final result will be output-referred, and if the chosen capacitor is one input capacitor, the result will be referred to that input.

The expression of the noise voltage across the capacitor will consist of noise voltage sources multiplied by transfer functions. Noise PSD over the capacitor will be given by PSD of each noise voltage source times the magnitude of the corresponding transfer function squared.

Mean-square noise voltage over the capacitor is found by integrating its noise PSD over all frequencies. This is the total noise power of the present phase. Total noise power of the whole clock period adds up from every phase.

The noise calculations in this chapter have concerned thermal noise in a single-ended SC-circuit. With a fully differential implementation, the number of transistor switches as well as capancitances are doubled, and so are the power of the thermal noise. One has to multiply the single-ended noise power by two, to get the noise power of the corresonding fully differential circuit.

One should remember that differential implementation also means that the signal swing can be doubled, giving that the signal power becomes four times the case of single-ended implementation. Thus, a differential design is preferable because it will reduce thermal noise compared to signal power.

5.3 FLICKER NOISE

Intrinsic noise in CMOS devices caused by trapping and release of charge carriers is called flicker noise or *1/f*-noise. This brings low-pass shaped noise into the drain current. Its power spectral density is approximately propotional to $1/f^a$, where f is the frequency and $a \in [0.8, 1.3]$ [2].

Flicker noise power is also proportional to *1/(WL)*, i.e. inversely proportional to the channel widht and length of the MOS transistor. Large transistors causes less flicker noise.

[1] clames that flicker noise in SC-switches are negligible, since the current flow in short pulses, and flicker noise occurrs at long intervals. Problems should only occur in active blocks. Therefore, it is good to have large sized transistors at OTA inputs. By the difference in PN-junctions, for some technologies PMOS transistors are less distorted by flicker noise than NMOS. [3] If it is the case for the technology one is going to use, the OTA should preferably be designed with PMOS transistor at its input.

If required, there are some known techniques to further reduce the flicker noise effect in operational amplifiers. Foremost, correlated double-sampling (CDS) can be used to reduce effects of not only of flicker noise, but also effects of offset voltage and sensitivity to finite DC-gain in the amplifier [7].

6

SIZING OF CAPACITORS IN SC SDM'S

The sizing of the capacitors is the first step to be able to realize a fully functional circuit realization of a SDM. This step is relevant due to the fact that too small capacitors will introduce unwanted thermal noise at the output of the SDM, which might decrease the SNR, and too large capacitors will result in increased requirements on the OTA's due to the larger load. The goal is to choose the capacitors to be as small as possible in order to let the OTA's drive the smallest load possible, and to still make the capacitors large enough so that the desired SNR is still fulfilled.

The method here is to start by inserting equivalent noise sources at one of the inputs of each integrator and to calculate the input-referred spectral density of the noise generated inside of the integrator. The next step is to calculate the transfer function from each noise source to the output. The last step is to mulitiply each input-referred noise spectral density with the corresponding transfer function and to integrate this over the frequency band of interest. The frequency band of interest is the passband of the modulators STF and the result of these calculations will be the noise power at the output of the SDM. This resulting expression will depend on the capacitors of each integrator and the capacitor sizes will here be adjusted so that the output power is smaller or equal to our calculated noise budget.

6.1 EQUIVALENT NOISE MODEL

The first step when trying to estimate the thermal noise at the output of the SDM, is to insert equivalent noise sources at one of the inputs of every integrator. Which actual input that is chosen does not really matter since the transfer function from the noise source of interest to the output of the modula-

tor is used to calculate the noise power at the output of the modulator. To be able to illustrate this operation the second-order SDM used earlier in the report have been used. The SFG describing the modulator can be seen in Fig. 6.1 and the result of the operation can be seen in Fig. 6.2.

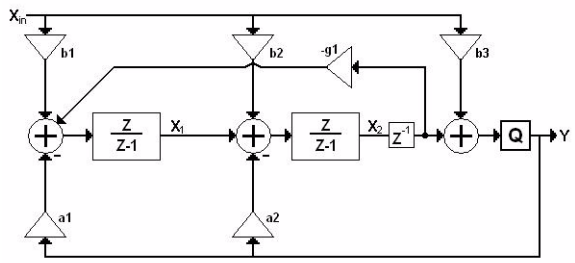

Figure 6.1: A second-order SDM.

The method used in this chapter when calculating the input-referred noise powers of the integrators is assuming that $R_{on} \cdot g_m \gg 1$. This means that the noise due to the switches is dominating the noise due to the OTA, and that this method calculates the input-referred noise power as a noise generated by the switches. However, in most cases it is important to optimize the power dissipation of the modulator and then one should use the general method to estimate the input-referred noise power, presented in Chapter 5. This general method does not assume anything, which means that the noise will also depend on the design of the OTA, and an iterative design flow will therefore be required in order to obtain the minimum power dissipation.

The total mean-square noise charge generated by a SC-integrator with one input is $q_e^2 = 2kT \cdot C_s$, where C_s is the sampling capacitor of the integrator. It is common that integrators have several inputs, which often result in several sampling capacitors. This can for example be seen in Fig. 6.3. Since the thermal noise generated at the different capacitors can be seen as uncorrelated noise sources, it is possible to add the different mean-square noise charges generated by each capacitor according to equation (6.1). The index i is the index of all the sampling capacitors of the circuit.

$$q_e^2 = 2kT \cdot \sum_i C_i \tag{6.1}$$

In order to calculate the input-referred noise power, one needs to start with calculating the output-referred noise power. This is done by transfering the mean-square noise charge to a noise power over the output capacitor C_h. The expression for doing this is shown in equation (6.2).

$$v_{out}^2 = \frac{q_e^2}{C_h^2} \tag{6.2}$$

Finally, the input-referred noise power is obtained if one divides the input-referred noise power with the gain, from the noise source to the output of the modulator, to the power of two. The resulting input-referred noise power is shown in equation (6.3), where the input capacitor is assumed to be C_k and k is the index of the sampling capacitor where the equivalent noise source is added.

$$v_{in}^2 = \frac{v_{out}^2}{\left(\frac{C_k}{C_h}\right)^2} = \frac{2kT}{C_k^2}\sum_i C_i \tag{6.3}$$

6.2 TRANSFER FUNCTION FOR THERMAL NOISE

To be able to estimate the noise power at the output of the modulator, one needs to calculate the transfer functions from the different noise sources to the output. This is done by creating a linear model of the SFG where the quantizer is removed due to the fact that the quantization error and the input signal is considered to be zero when calculating the transfer function from the different error sources. The second-order SDM, which has been used as an example troughout this report, has been used to illustrate this. The simplified version of the SFG which is used when calculating these transfer functions can be seen in Fig. 6.2.

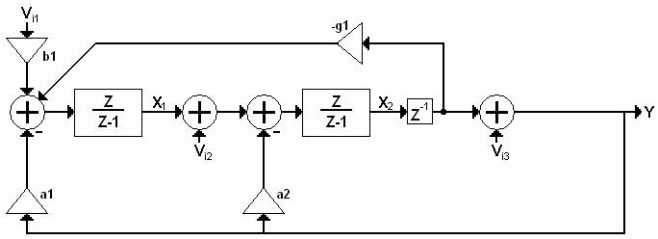

Figure 6.2: Simplified SFG representing the second-order SDM.

Equations (6.4), (6.5) and (6.6) are given from the SFG shown in Fig. 6.2. All three noise sources are included in these equations.

$$x_1 = (v_{i1}b_1 - ya_1 - x_2g_1z^{-1}) \cdot \frac{z}{z-1} \tag{6.4}$$

$$x_2 = (x_1 - v_{i2} - ya_2) \cdot \frac{z}{z-1} \tag{6.5}$$

$$y = x_2z^{-1} + v_{i3} \tag{6.6}$$

Equations (6.4), (6.5) and (6.6) give:

$$y = \frac{v_{i1}b_1 \cdot z + v_{i2} \cdot (z-1) + v_{i3} \cdot (z^2 + (g_1 - 2)z + 1)}{z^2 + (g_1 + a_1 + a_2 - 2) \cdot z + 1 - a_2} \tag{6.7}$$

The last step is to set $v_{n2} = 0$ and $v_{n3} = 0$ in order to get $H_1(z)$, $v_{n1} = 0$ and $v_{n3} = 0$ to get $H_2(z)$ and $v_{n1} = 0$ and $v_{n2} = 0$ in order to get $H_3(z)$. $H_1(z)$ is the transfer function from the error source v_{n1} to the output of the modulator, $H_2(z)$ and is the transfer function from the error source v_{n2} to the output of the modulator and $H_3(z)$ and is the transfer function from the error source v_{n3} to the output of the modulator.

$$H_1(z) = \frac{y}{v_{i1}} = \frac{b_1 \cdot z}{z^2 + (g_1 + a_1 + a_2 - 2) \cdot z + 1 - a_2} \tag{6.8}$$

$$H_2(z) = \frac{y}{v_{i2}} = \frac{z-1}{z^2 + (g_1 + a_1 + a_2 - 2) \cdot z + 1 - a_2} \tag{6.9}$$

$$H_3(z) = \frac{y}{v_{i3}} = \frac{z^2 + (g_1 - 2)z + 1}{z^2 + (g_1 + a_1 + a_2 - 2) \cdot z + 1 - a_2} \tag{6.10}$$

The three equations (6.8), (6.9) and (6.10) are the transfer functions from the three noise sources inserted in the SFG in Fig. 6.2 and these equations are going to be used to calculate the total noise power due to thermal noise at the output of the modulator in section 6.4.

6.3 NOISE AT THE OUTPUT OF THE SDM

Up to this, the input-referred noise power at the input of the integrators and their respective transfer functions to the output of the modulator have been calculated. The only thing that remains is to integrate each noise power spectral density in the band of interest. The band of interest is the passband of the SDM's STF and the resulting output noise powers can then be added to achieve the total output noise power. In this specific case we are dealing with a lowpass SDM which means that the integration is specified by the expressions below.

The expression for calculating the output noise power resulting from one noise source is done according to equation (6.11). H_i is the transfer function from the noise source, which generates the noise power v_i^2, to the output of the modulator and f_s is the sampling frequency of the modulator and M is the oversampling factor. In order to get the frequency spectra of $H_i(z)$ one needs to substitute $z = e^{j2\pi fT}$.

$$\overline{N}_i^2 = \frac{v_i^2}{\left(\frac{f_s}{2}\right)} \int_0^{f_s/(2M)} \left|H_i(e^{j2\pi fT})\right|^2 df \tag{6.11}$$

The resulting total noise power at the output is then calculated according to equation (6.12).

$$\overline{N}_{tot}^2 = \sum_i \overline{N}_i^2 \tag{6.12}$$

6.4 EXAMPLE: SECOND-ORDER SDM

In this section the noise power at the output of the second-order SDM, which can be seen in Fig. 6.1, is going to be calculated.

6.4.1 THE FIRST INTEGRATOR OF THE SECOND-ORDER SDM

The first step in this example is to insert equivalent noise sources at the input of every integrator. This has already been done in section 6.1 and the result of this is shown in Fig. 6.2. To be able to calculate the output noise power of the modulator one also needs to have knowledge about how the circuit is implemented. The single-ended circuit implementation can be seen in Fig. 6.3. The multiplications with factor *-1* in this schematic is not going to be considered in these calculations since they are easily implemented when dealing with a fully differential circuit.

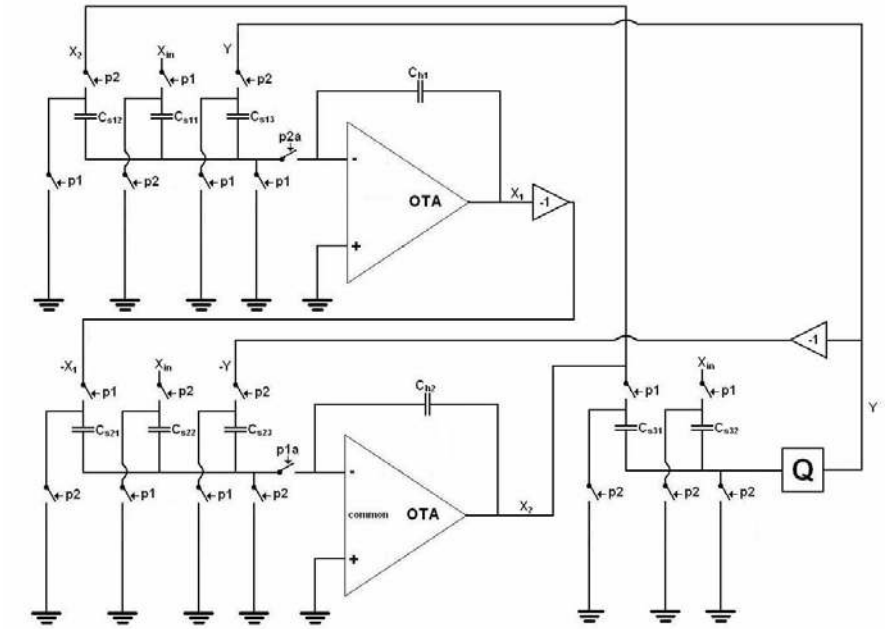

Figure 6.3: Circuit implementation of the second-order SDM.

The noise charge generated by the two sampling capacitors is calculated by using equation (6.1) and the result is shown in equation (6.13).

$$q_{e1}^2 = 2kT \cdot (C_{s11} + C_{s12} + C_{s13}) \tag{6.13}$$

When the noise power generated by the sampling capacitors in integrator 1 is calculated, the output-referred noise power is obtained using equation (6.2). The result of this operation can be seen in equation (6.14).

$$v_{o1}^2 = 2kT \cdot \frac{(C_{s11} + C_{s12} + C_{s13})}{C_{h1}^2} \tag{6.14}$$

Finally the input-referred noise power is obtained using equation (6.3) and input capacitor were the equivalent noise source is inserted is capacitor C_{s11}. The result is presented in equation (6.15).

$$v_{i1}^2 = \frac{2kT}{C_{s11}} \cdot \left(1 + \frac{C_{s12}}{C_{s11}} + \frac{C_{s13}}{C_{s11}}\right) \tag{6.15}$$

6.4.2 THE SECOND INTEGRATOR OF THE SECOND-ORDER SDM

A faster approach is going to be used when calculating the input-referred noise power of the second integrator since the calculations are almost the identical. The first step is then to calculate the mean-square noise charge which is generated by these three capacitors according to equation (6.1) and the result is shown in equation (6.16).

$$q_{e2}^2 = 2kT \cdot (C_{s21} + C_{s22} + C_{s23}) \tag{6.16}$$

Equation (6.3) and (6.16) gives:

$$v_{i2}^2 = \frac{2kT}{C_{s21}} \cdot \left(1 + \frac{C_{s22}}{C_{s21}} + \frac{C_{s23}}{C_{s21}}\right) \tag{6.17}$$

Equation (6.17) now represents the input-referred noise power at the input of integrator 2.

6.4.3 THE QUANTIZER ADDITION

The last noise power which is supposed to be calculated is the one in front of the quantizer where the equivalent noise source v_{i3} is inserted. The only dif-

ference here is that once the mean-square noise charge is declared, the only thing that is left is to look at the total noise power which the mean-square noise charge causes on the input capacitor C_{s31} where the noise is added. This is done by first calculate the total mean-square noise charge, according to equation (6.1). The result is shown in equation (6.18).

$$q_{e3}^2 = 2kT \cdot (C_{s31} + C_{s32}) \tag{6.18}$$

The input-referred noise power $v_{i3}{}^2$ is then obtained according to equation (6.19).

$$v_{i3}^2 = \frac{2kT}{C_{s31}} \cdot \left(1 + \frac{C_{s32}}{C_{s31}}\right) \tag{6.19}$$

6.4.4 CALCULATION OF THE OUTPUT NOISE POWER

The last thing to do in this example is to integrate each noise power spectral density in order to get the noise power at the output of the SDM. The noise transfer functions from the noise sources have already been calculated and they are presented in section 6.2. The transfer function according to the first noise source v_{i1} is shown in equation (6.8), the transfer function according to the second noise source v_{i2} is shown in equation (6.9) and the transfer function according to the third noise source v_{i3} is shown in equation (6.10). The output noise power generated by each noise source is then calculated according to equation (6.11).

$$\overline{N}_1^2 = \frac{v_{i1}^2}{\left(\frac{f_s}{2}\right)} \int_0^{f_s/(2M)} \left|H_1(e^{j2\pi fT})\right|^2 df \tag{6.20}$$

$$\overline{N}_2^2 = \frac{v_{i2}^2}{\left(\frac{f_s}{2}\right)} \int_0^{f_s/(2M)} \left|H_2(e^{j2\pi fT})\right|^2 df \tag{6.21}$$

$$\overline{N}_3^2 = \frac{v_{i3}^2}{\left(\frac{f_s}{2}\right)} \int_0^{f_s/(2M)} \left|H_3(e^{j2\pi fT})\right|^2 df \tag{6.22}$$

The parameter values used to calculate the output presented in Table 6.1.

Cefficient	**Realization**	**Value**
b0	C_{s11}/C_{h1}	0.30788
a0	C_{s12}/C_{h1}	0.29557
g1	C_{s13}/C_{h1}	0.01545
v1	C_{s21}/C_{h2}	0.32370
b1	C_{s22}/C_{h2}	0.11162
a1	C_{s23}/C_{h2}	0.21128
v2	-	2.50850
b2	-	0.47000
M	-	32

Table 6.1. Parameter values for the SDM.

These parameter values together with equation (6.20), (6.21) and (6.22) gives:

$$\overline{N}_1^2 = \frac{kT}{C_{s11}} \cdot 0.13156 \tag{6.23}$$

$$\overline{N}_2^2 = \frac{kT}{C_{s21}} \cdot 0.00444 \tag{6.24}$$

$$\overline{N}_3^2 = \frac{kT}{C_{s31}} \cdot 8.9578 \cdot 10^{-5} \tag{6.25}$$

Finally, the total output power is computed using equation (6.12), (6.23), (6.24) and (6.25).

$$\overline{N}_{tot}^2 = \left(\frac{kT}{C_{s11}} \cdot 0.13156 + \frac{kT}{C_{s21}} \cdot 0.00444 + \frac{kT}{C_{s31}} \cdot 8.9578 \cdot 10^{-5}\right)c \tag{6.26}$$

6.4.5 CAPACITOR SIZES

Before calculating the different capacitor sizes, one needs to estimate the total amount of noise power which is allowed at the output of the modulator due to thermal noise. This can be determined according to the model described in

chapter 6. In this calculation the noise power due to thermal noise is $P_{n_T} = 4,686 \cdot 10^{-6}[V^2]$.

The next step is to decide how large parts of the total noise power allowed each term shall contribute with. This can easily be seen as an optimization problem where several iterations can be needed. The parts of the noise is defined according to equation (6.27).

$$\sum_i k_i = 1 \tag{6.27}$$

The index i is the index of the different noise sources and in this example the indexes are 1, 2 and 3. The equation which then needs to be solved to find the capacitor sizes is equation (6.28).

$$\overline{N}_i^2 = k_i P_{n_T} \tag{6.28}$$

In the current example with three different noise powers according to equation (6.23), (6.24) and (6.25), equation (6.28) gives:

$$C_{s11} = \frac{kT}{k_1 P_{n_T}} \cdot 0.13115 \tag{6.29}$$

$$C_{s21} = \frac{kT}{k_2 P_{n_T}} \cdot 0.00335 \tag{6.30}$$

$$C_{s31} = \frac{kT}{k_3 P_{n_T}} \cdot 6.0722 \cdot 10^{-5} \tag{6.31}$$

In this example k_1, k_2 and k_3 are chosen to be:

$$k_1 = 0.9 \tag{6.32}$$

$$k_2 = 0.05 \tag{6.33}$$

$$k_3 = 0.05 \tag{6.34}$$

The values of k_i can be changed to allocate different amounts of the noise budget to different noise sources. This problem can be seen as an optimization problem where one migth be able to find a optimal solution for the smallest power dissipation or area. The coefficient k_i together with equation (6.29)

, (6.30) and (6.31) and $kT = 4.8 \cdot 10^{-21}$ gives the capacitor values:

$$C_{s11} = 1.498 \cdot 10^{-16}[F] \tag{6.35}$$

$$C_{s21} = 5.050 \cdot 10^{-17}[F] \tag{6.36}$$

$$C_{s31} = 9.177 \cdot 10^{-18}[F] \tag{6.37}$$

With the capacitor relations showed in table 6.1 and equations (6.35), (6.36) and (6.37) the rest of the capacitor values can be calculated.

$$C_{h1} = 4.864 \cdot 10^{-16}[F] \tag{6.38}$$

$$C_{s12} = 1.438 \cdot 10^{-16}[F] \tag{6.39}$$

$$C_{s13} = 7.513 \cdot 10^{-18}[F] \tag{6.40}$$

$$C_{h2} = 1.560 \cdot 10^{-16}[F] \tag{6.41}$$

$$C_{s22} = 1.741 \cdot 10^{-17}[F] \tag{6.42}$$

$$C_{s23} = 3.296 \cdot 10^{-17}[F] \tag{6.43}$$

$$C_{s32} = 1.719 \cdot 10^{-18}[F] \tag{6.44}$$

6.4.6 CAPACITOR AREA DEPENDING ON ALLOWED NOISE

Another way of choosing the capacitor sizes is by defining an optimization problem where the summation of all the capacitor values in the circuit is assumed to be proportional to the area of the circuit. The assignment is then to choose the capacitor values to fulfill equation (6.46) and to minimize the summation of the capacitors according to equation (6.45). One also need to consider that the noise due to thermal noise is not too large and the criteria for this is given by equation (6.46), where N_k^2 is the noise power at the output of the modulator generated by a specific noise source and N_{t0}^2 is the total amount of noise power due to thermal noise allowed at the output of the mod-

ulator.

$$\min \sum_i C_i \tag{6.45}$$

$$\sum_k \overline{N}_k^2(C_k) < \overline{N}_{T_0}^2 \tag{6.46}$$

The last thing that limits this optimization problem is that the capacitors cannot be to small since the fact that the switches in the modulator have a limited off-resistance. This means that leakage current will occur which will mean that charge will be lost from the sampling capacitors in between the sampling and integration phase when all of the switches are non-conducting. This parameter have to be chosen individually for each capacitor, since they in most designs have different amount of switches connected to each capacitor.

The optimization problem corresponding to the second-order sigma-delta modulator presented in this report can be formulated according to the equations below. The minimum size of the capacitors have here been chosen to be the same for all of the capacitors and the value is C_{min}.

$$\min C_{tot} = 2.01017 \cdot C_{s11} + 1.99754 \cdot C_{s21} + 1.18736 \cdot C_{s31} \tag{6.47}$$

$$\frac{6.3151 \cdot 10^{-22}}{C_{s11}} + \frac{2.1294 \cdot 10^{-23}}{C_{s21}} + \frac{4.2997 \cdot 10^{-25}}{C_{s31}} \leq 4.6855 \cdot 10^{-6} \tag{6.48}$$

$$C_i \geq C_{min} \tag{6.49}$$

6.4.7 CONCLUSION

One can see by looking at equation (6.26), that the noise power at the output of the modulator in this example is dominated by the noise produced in integrator 1. This is beacuse of the fact that every noise source is damped by the gain of the integrators before the noise source and it means that the capacitors in integrator 1 will be the largest ones. Worth mentioning here is that the result presented in equation (6.26) is when dealing with a single-ended circuit. If one want to expand this theory to apply to differential circuits, one only need to multiply the resulting noise power in the single-ended case by a factor 2 since differential design have twice as many capacitors and switches.

7

OTA SPECIFICATIONS FOR SC SIGMA-DELTA MODULATORS

7.1 OTA SPECIFICATION

This chapter is supposed to explain a method to in a structured way set the requirements on a OTA which should be used in a SC-integrator. The purpose of setting the requirements as precise as possible is to optimize the power dissipation of the OTA. The parameters which are supposed to be set is unity-gain bandwitdh w_u, Slewrate SR, phase margin ϕ_m, DC-gain a_0, and output range.

The actual SC-design of the integrator, were the OTA is used, has to be specified since the startpoint of this analysis is the load of the OTA. Lets look at the integrator in Fig. 7.1. It is possible to represent this integrator as a model with the parameters gain and feedback factor β, as showed in Fig. 7.3.

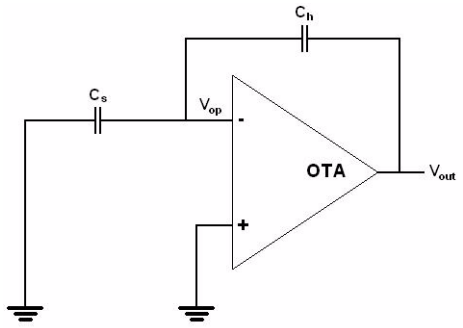

Figure 7.1: Equivalent circuit of SC-integrator for calculation of β.

To be able to calculate the feedback factor β, one needs to look at the at the schematic representation of the integrator in Fig. 7.1. The feedback factor for this particular configuration is defined as:

$$\beta = \frac{V_{op}}{V_{out}} = \frac{C_h}{C_s + C_h} \tag{7.1}$$

A more general expression for β for a SC-integrator with *n* inputs can be seen in equation (7.2) and the corresponding modulator can be seen in .

$$\beta = \frac{V_{op}}{V_{out}} = \frac{C_h}{\sum_n C_n + C_h} \tag{7.2}$$

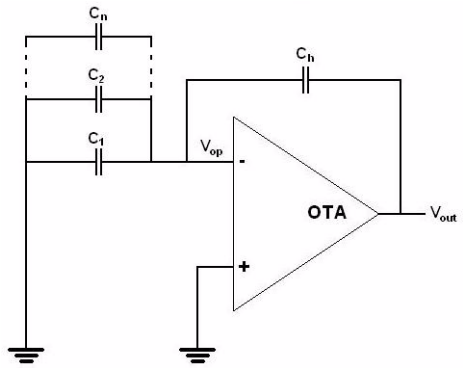

Figure 7.2: Equivalent SC-integrator with *n* inputs for calculation of β.

The feedback factor β will later be used to estimate the the phase margin for optimal settling according to the method suggested by [9].

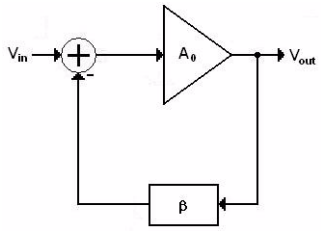

Figure 7.3: Model of a SC-integrator.

7.1.1 DC-GAIN REQUIREMENTS ON AN OTA

The first parameter which is to be decided is the DC-gain of the OTA. This can be done by setting up a model of how the DC-gain affects the output of a SC- integrator. The first thing that needs to be done is to specify the function of an OTA with limited DC-gain and this is shown according to equation (7.3). A_0 is the DC-gain, V_{in}^+ and V_{in}^- is the inputs and V_{out} is the output of the OTA.

$$V_{out} = (V_{in}^+ + V_{in}^-) \cdot A_0 \tag{7.3}$$

The obtained transfer function of a SC-integrator with n inputs using equation (7.3) is presented in equation (7.4), with α and β according to equation (7.5) and equation (7.6). k_n is a variable which decides if input is an inverting input($k_n = 0$) or a non-inverting input($k_n = 1$).

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \left(\sum_n C_n z^{\frac{1}{2}(1-k_n)} \right) \frac{1}{C_H} \frac{1}{\alpha z - \beta} \tag{7.4}$$

$$\alpha = \frac{1}{C_H A_0} \sum_n C_n + \frac{(A_0 + 1)}{A_0} \tag{7.5}$$

$$\beta = \frac{(A_0 + 1)}{A_0} \tag{7.6}$$

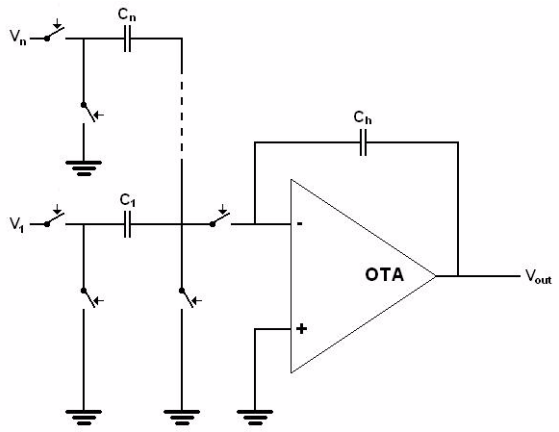

Figure 7.4: SC-integrator with n inputs.

The resulting model of the integrator can be seen in Fig. 7.5 and the idea is that this model shall be used to simulate the modulator in matlab with different values on the DC-gain A_0 in order to determine the requried DC-gain of the different OTA's used to implement the modulator.

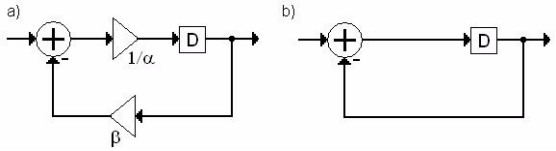

Figure 7.5: SFG describing the integrator. a) Variable DC-gain A_0.b) Ideal model.

7.1.2 REQUIREMENT OF SETTLING ERROR

To be able to estimate the phase margin for optimal settling one needs to know the maximum settling error which is tolerated in order to fulfill the requirements on the SNR. This is done by simulating a model of the system with variable DC-gain, for example in Matlab, where the maximum settling error is specified and the output error is measured by observing the SNR. The output of such a simulation can look something like in Fig. 7.6.

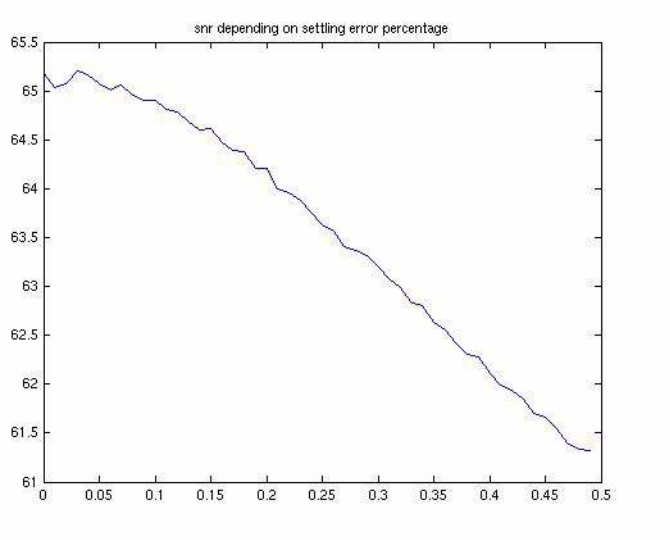

Figure 7.6: SNR depending on settling error.

In Fig. 7.6 one can see that the settling error cannot be larger than 0.2% if the system is supposed to perform over 64 dB SNR. This design parameter is called error bound and is later used to obtain the phase margin for optimal settling.

7.1.3 PHASE MARGIN FOR OPTIMAL SETTLING

The method for finding the phase margin for optimal settling is based upon a time-domain analysis of an under-damped system decribed in [9]. The result of this analysis is the optimal phase margin for a SC-integrator with specified feedback factor β and a specified error bound *D*. The expression for the optimal phase margin is defined by equation (7.7).

$$\phi_m(MST) = 90° - \text{atan}\left(\frac{1+\left(\frac{\pi}{\ln(D)}\right)^2}{4\beta}\right) \tag{7.7}$$

The pole separation factor is defined by the two poles w_1 and w_2 according to equation (7.8).

$$\Upsilon_0 = \frac{\omega_2}{\omega_1} \tag{7.8}$$

What is also given out of this theory is that one can also obtain the pole separation factor from the phase margin and this is done according to equation (7.9).

$$\Upsilon_0 = 4\frac{(1 + a_0\beta)}{1 + (\pi/\ln(D))^2} \tag{7.9}$$

7.1.4 SLEWRATE AND OUTPUT RANGE

When it comes to specifying slewrate, there are several different methods of doing this. The method suggested by [1] is just to allocate 25% of the total settling time, which is half the time of a clock period, for slewing. What is left is only to divide the worst case step with the allocated time. This gives the expression:

$$SR = \frac{V_{max} - V_{min}}{t_{slew}} \tag{7.10}$$

Worth mentioning about slewrate is that the chance of that an integrator's output has to go from V_{min} to V_{max} or the other way at one time period is most unlikely, which basicly means that the slewrate according to equation (7.10) is too large. The needed slewrate seems to be dependent on the modulator design and the number of quantization steps in the modulator and until a more precise theory is developed the suggested way of deciding the correct slewrate is to simulate and iterate.

When it comes to specifying the output range, the most important thing is that one have taken this in account when designing the ADC and setting the scale constants. The scaling compensates for non-ideal input- and output ranges and almost any ranges are acceptable if the scaling is done well, although a good output range is preferable in order to be able to scale the first integrator in the modulator as much as possible to be able to minimize the total area of the capacitors.

7.2 SIMULATION OF TWO-POLE MODEL OF OTA

In order to specify the last parameter, which is the unity-gain bandwith w_u, one has to set up a model which simulates a two-pole OTA. The pole separation factor is accessable according to equation (7.9), and this will be used to decide the second pole of the system, when the first one is specified.

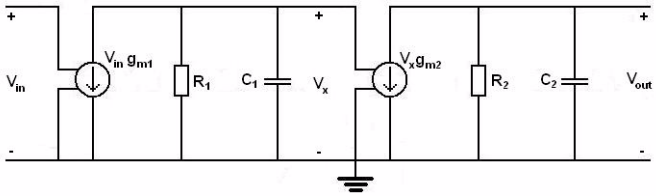

Figure 7.7: Two-pole model of an OTA.

The two-pole model presented in Fig. 7.7 has the following transfer function:

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{R_1 g_{m1} \cdot R_2 g_{m2}}{(1 + R_1 C_1 s)(1 + R_2 C_2 s)} \tag{7.11}$$

In equation (7.11) one can start by identifying the DC-gain A_0 and the two poles ω_1 and ω_2.

$$A_0 = R_1 g_{m1} \cdot R_2 g_{m2} \tag{7.12}$$

$$\omega_1 = \frac{1}{R_1 C_1} \tag{7.13}$$

$$\omega_2 = \frac{1}{R_2 C_2} \tag{7.14}$$

One can also use equation (7.8), which together with equation (7.11), equation (7.12), equation (7.13) and equation (7.14) gives:

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{A_0}{\left(1 + \frac{s}{\omega_1}\right)\left(1 + \frac{s}{\Upsilon \cdot \omega_1}\right)} \tag{7.15}$$

Equation (7.15) gives an expression which only depends on the dominating

pole w_1. The pole-separation factor γ is a constant which is calculated according to equation (7.9). The parameteters needed to simulate the two-pole model of the OTA is given by table 7.1.

Parameter	**Value**
g_{m1}	1
R_1	1
C_1	$\frac{1}{\omega_1}$
g_{m2}	$\frac{A_0}{R_2}$
R_2	R_{out}
C_2	$\frac{1}{\Upsilon\omega_1 R_2}$

Table 7.1. Parameter values of the two-pole OTA model.

7.3 EXAMPLE OF OTA SPECIFICATIONS

This example is going to illustrate how to obtain the specifications of the OTA which is used to realize the first integrator in the second-order SDM used as an example troughout this report. The circuit realization of the first integrator can be seen in Fig. 7.8. It is here assumed that the signal X_1 is connected into the next integrators sampling period, which basicly means that the only load which the OTA experiences is the capacitor C4.

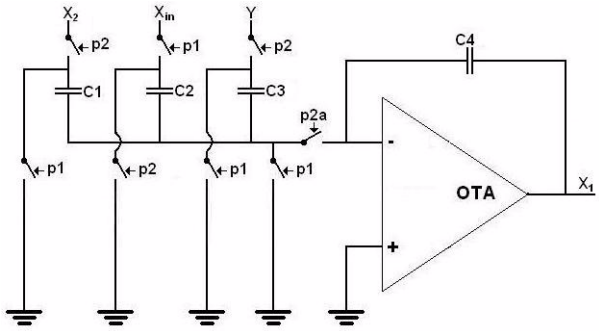

Figure 7.8: Circuit realization of the first integrator of the second-order SDM.

The first thing to do is to simulate the differential equations describing the modulator with limited DC-gain in order to find the required DC-gain. The same DC-gain has been used for both of the integrators in the second order SDM and the result of this simulation can be seen in Fig. 7.9.

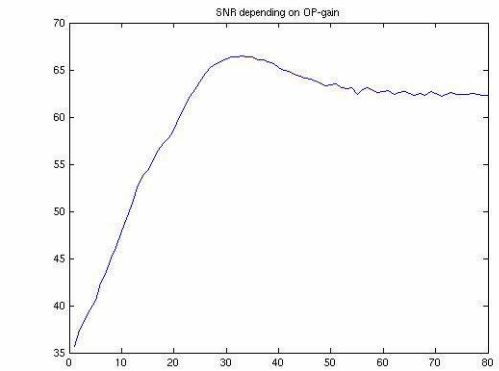

Figure 7.9: SNR plotted against DC-gain of the OTA's.

As one can see, it would be enough to choose a DC-gain of 30 dB, but to have some design margin left when the settling fault is added the DC-gain is chosen to be 50 dB for both of the integrators in the second order SDM.

In order to be able to find the optimal phase margin and pole-separation factor, one needs to start by finding out the feedback factor β for the SDM showed in Fig. 7.8. The expression for this can be seen in equation (7.16).

$$\beta = \frac{C_h}{C_h + C_{s11} + C_{s12} + C_{s13}} = \frac{1}{1 + \frac{C_{s11}}{C_h} + \frac{C_{s12}}{C_h} + \frac{C_{s13}}{C_h}} \tag{7.16}$$

The modulator coefficients have been calculated earlier in this report and they are realized by the following capacitor relations:

$$a_0 = \frac{C_{s11}}{C_h} = 0.29557 \tag{7.17}$$

$$b_0 = \frac{C_{s12}}{C_h} = 0.30788 \tag{7.18}$$

$$g_1 = \frac{C_{s13}}{C_h} = 0.01545 \tag{7.19}$$

Equation (7.16), (7.17), (7.18) and (7.19) gives:

$$\beta = \frac{1}{1 + b_1 + a_1 + g_1} = 0.61771 \tag{7.20}$$

The next thing to be done is to simulate the system in order to obtain the allowed settling error of the circuit. This has been done with a DC-gain of 50 dB and the result can be seen in Fig. 7.10. Lets say that 62 dB of SNR is enough to be able to fulfill the specifications of the modulator and this means that $D = 0.004$ is the allowed settling error.

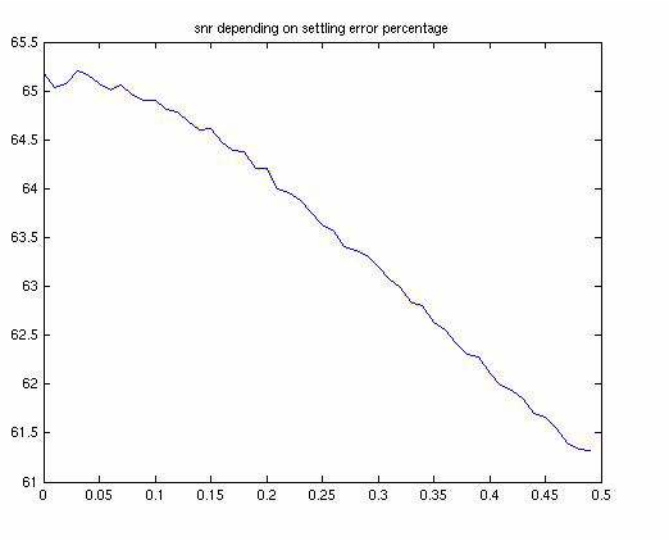

Figure 7.10: SNR depending on the settling-error in percent.

The error bound D and feedback factor β is now specified so the phase margin and pole-separation factor can now be calculated according to equation (7.7) and (7.9).

$$\phi_m = 61.8° \tag{7.21}$$

$$\Upsilon_0 = 592.9 \tag{7.22}$$

The thing that is left to do now is to set up the two-pole model of the integrator and to simulate it with the calculated values of A_0, γ_0 and R_{out} which here is chosen to be $10k\Omega$. The parameters of the two-pole model is set according to Table 7.1. and the only parameter which is left to variate now is the value of the first pole, which is supposed to be changed until one can see that the first peak of the settling signal just goes exactly as far as the tolerated limit. This is needed due to the theory of perfect settling suggested by [10]. After achieving a good settling behaviour the model of the OTA can be disconnected and simulated in order to find the unity-gain bandwith ω_u. The achieved parameters can be seen below.

$$A_0 = 50\text{dB} \tag{7.23}$$

$$\omega_u = 3.13 \text{ MHz} \tag{7.24}$$

$$\varphi_m = 60° \tag{7.25}$$

The output range has to be chosen during the scaling of the integrator and if it cannot be fullfilled with the chosen OTA-structure the scaling has to be done again with another output range in mind. The scaling for this model has been done according to the following output range.

$$OR = 0.4 \text{ to } 2.9\text{V} \tag{7.26}$$

7.4 OTA TEST

In order to test our OTA-specifications an OTA was constructed. The only problem was that we were not, due to lack of time, able find an OTA-structure with the rules of freedom that was requested. The chosen OTA-structure was therefore taken from [1], which is an fully-differential folded cascode single-stage OTA. The advantages with this structure is that it has low power dissipation due to the single-stage design. The drawback is though, that the phase margin will always be good and this means that there is not really a point in trying to find the optimal phase margin. Instead the main goal of the unity-gain bandwith simulation was to let the bandwith be low enough to let the signal settle within the allowed settling error *D* during a time of *330 ns,* which was our allowed settling time when running with *44.1k Samples/second* and an OSR of 32. This gave us a bandwith of *3.16 MHz* with a capacative load of *2 pF.*

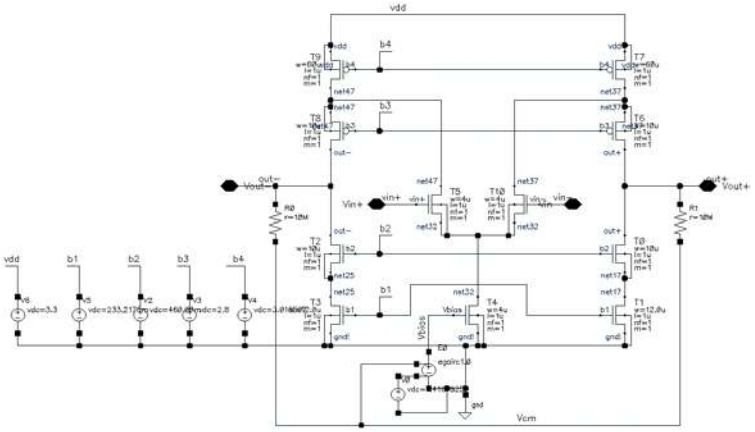

Figure 7.11: Schematic of the folded-cascode OTA.

After several simulations with the constructed OTA, which can be seen in Fig. 7.11, one could see that the SNR of the system was well within range of the desired SNR which shows that our estimation of the OTA- specifications was correct. The bias current in each branch of this OTA was 16 uA, which probably could have been made even lower. Some measured values of the SNR at the output of the modulator can be seen in table 7.2. The maximum bandwitch according the Nyquist Sampling Theorem is then $\frac{(44.1 \cdot 10^3)}{2} = 22.05$ kHz , because the fact that our eample modulator is an low-pass SDM.

Frequency	**SNR**
1 kHz	67.31 dB
5 kHz	70.80 dB
10 kHz	69.77 dB
15 kHz	69.67 dB
20 kHz	67.72 dB
25 kHz	

Table 7.2. Measured SNR at the output of the modulator.

As one can see, the SNR of the simulations is a few dB better than expected and this is explained due to the fact that the matlab simulations are pessimis-

tic, which means that the resulting SNR always is the worst one that could be found.

8

CONCLUSIONS

8.1 CONCLUSIONS & RESULTS

8.1.1 SCALING

Scaling is a very important activity when building a SDM and in this chapter we suggest a method that is supposed to scale the inputs of the integrators so that the chance of clipping at the output of the OTA is reduced. Our simulations showed that clipping at the output of the integrators reduced the SNR significantly, so we thought that a scaling method which allowed as little clipping as possible should be best. This particular issue could easily be simulated even further to find out how much clipping an integrator can have before it starts to reduce the SNR significantly. This might mean that the first integrators inputs could be scaled up even further which would mean that the capacitor sizes, due to the thermal noise, could be reduced and power might be saved.

The most important discovery in this chapter is that chip area and power can be saved if the scaling is done properly.

8.1.2 METHOD TO REALIZE AN SDM USING SC-NETS

Even though the theory of sigma-delta noise shaping filters are well-known since allmost two decades, there are very little litterature with structured methology for top-down design. The many trade-offs makes it hard to go

right from a mathematical modulator structure down to a realization on circuit level.

What is presented in this thesis, is a suggested design flow from a given signal flow graph down to a switched-capacitor circuit realization. We have not seen anything similar in any litterature we have read.

With this design flow, the final realization are known allready at SFG level. When chosing the modulator structure, aspects as capacitive load at OTA outputs, requirement for external S&H, time given for quantization and DAC can be considered. Once understood, the approach is intuitive and straight-forward.

Some conclusions concerning the possibility of using inverting or non-inverting input to a differential SC-integrator are made. One can be able to avoid driving extra load at an integrators integration phase by using the best-suited coupling (inverting or non-inverting) into the following integrator. The best choice depends of the size of the capazitors, which is depending of coefficients, scaling and thermal noise. The research and simulations on this subject has to be continued to get accurate results.

8.1.3 NOISE ANALYSIS AND CAPACITOR SIZING

Oppertunities for formulation of optimization is what characterizes the investigations of capacitor sizing depending of thermal noise. The first oppertunity is when dealing with the noise budgets for thermal noise, quantization noise and the noise margin for other noise sources. It would be very interesting here to see if we would be able to save power by choosing to construct a better modulator, which produces a smaller amount quantization noise, and to have a larger budget for thermal noise.

The second opportunity to formulate an optimization problem is a variation of the one that is already formulated in Chapter 6. The only difference is that it would be interesting to formulate some kind of cost function which describes the power estimation of the different OTA's depending on the capacitor sizes.

A thing that we can feel is missing here is a detailed analysis of the switches in the design that specificly focusing on the leakage currents.

8.1.4 OTA SPECIFICATIONS

The OTA-specifications seems like an area where over-estimation of the requirements are very common. Since the OTA's is the main power consumers of a SDM it is also very important to optimize the requirements to be able to have as low power disspation as possible.

We feel that more extensive testing of the constructed OTA would have been needed to really prove our point and we think that even our estimation of the demands are a little bit over the top. Still, the methodology suggested in this chapter is something that we have not seen anywhere else and it proves that the requirements of the OTA's in SDM's can be turned down a few notches.

Another thing that has to be taking into account into this analysis is the noise of the OTA, for example the flicker noise.

8.2 FURTHER WORK AND DEVELOPMENT

The main thing of further work is to look at the other parts of the SDM which is the ADC and DAC. The only thing that reamins in order to build a complete SDM is to analyze at the switches in the design. Another component, which is not needed in all structures, is the S&H and this component would also have to be analyzed in order to build a SDM, especially when it comes to bandpass versions of the system.

Other things that would be interesting to evaluate further is the different optimization problems described in section 8.1 and to really investigate the different OTA structures to find out the benefits and drawbacks of them.

Finally, the hardest problem is not to build SDM's which can produce good results, but to make them power efficient and this is also the main problem when building sigma-delta ADC's and the main focus of further research.

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