On the Testing Quality of Random and Pseudo-random Sequences for Permanent and Intermittent Faults

Jin Ding
Dept. of Telecommunications
Beijing Univ. of Posts & Telecom.
Beijing 100088, P.R.China

Yu-Liang Wu
Dept. of Computer Science and Engineering
The Chinese University of Hong Kong
Shatin, Hong Kong

Abstract—In this paper, the natures of random and pseudo-random input sequences and their influence on permanent and intermittent fault detecting are analyzed. The aliasing fault coverage between the pseudo-random and random sequences is estimated. The activity probability features of the intermittent faults are considered. The self-test circuits of the intermittent faults are illustrated. The experimental results based on real circuits are obtained through simulation. The mathematical analysis and experimental results show that the quality of the pseudo-random testing is better than that of the random testing for the permanent and intermittent faults. The Markov chain models are used in obtaining the input sequence length needed for determining if a circuit fault is intermittent or permanent.

I Introduction

The continually growing complexity of VLSI circuits makes the built-in self-test (BIST) techniques especially attractive [1~3]. In the techniques, two modules: the pseudo-random sequence generator and the output responses compactor, have to be integrated into a VLSI chip. The pseudo-random sequences generated by the generator is applied to the inputs of the circuit under test (CUT) and at the same time, the compactor compresses the CUT responses set into a signature.

In most BIST techniques, the linear feedback shift register (LFSR) [4,5] is commonly used in generating the pseudo-random sequences. The responses compaction can be implemented by using the multiple input shift register (MISR) [6], the multiplexed parity trees [7], the transition count [8], the state-difference count [9], and so on. When the pseudo-random input sequences are applied to the CUT, the compactor compresses the CUT output responses simultaneously. After finishing the testing, the compressed signature will be compared with the expectant reference value produced by a corresponding fault-free circuit. If the two values are the same, the CUT testing will be considered pass; otherwise, the CUT will be considered faulty.

However, the pseudo-random sequences generated by the LFSR used in the BIST techniques are not completely random. Therefore, the natures of the pseudo-random input sequences and the effectiveness of the compact approaches need to be analyzed.

Some efforts have analyzed the pseudo-random testing [10-13]. These efforts used the combinatorial analysis and the differential solution to obtain the detection probability, the input sequence length, the fault coverage, the test confidence, and so on. The results of these efforts showed that the random test model is not a better approximation to the pseudo-random testing. However, the relationship among the input sequence length, the testability, and the fault coverage was not described in these efforts. Especially, the aliasing fault coverage between the random and pseudo-random sequences was not discussed.

In this paper, we will analyze the relationship among the input sequence length, the testability, and the fault coverage for the random and pseudo-random testing, and estimate the aliasing fault coverage between the random and pseudo-random sequences. Moreover, we will derive the expression of the aliasing fault coverage between the random and pseudo-random input sequences for the intermittent faults. We will obtain the activity probability of the intermittent faults by using the retry policy, and design the self-test circuits for the intermittent faults. Finally, we will give the input sequence length used to determine the intermittent or permanent fault in a circuit according to the Markov chains.

The paper is organized as follows. Section 1 introduces the problems to be resolved in this paper. Section 2 builds the analytical models of the aliasing fault coverage between the random and pseudo-random input sequences. Section 3 analyzes the influence of the random and pseudo-random testing on the intermittent faults. Section 4 demonstrates the self-test circuits for the intermittent faults. Section 5 concludes this paper.

II Aliasing coverage

Paper [14] has proposed a relationship between the mean fault coverage and the circuit testability. However, the relationship is only suitable for the pseudo-random sequences according to the analysis in [14], though it said the relationship is for the random vectors. Because it is known that the pseudo-random sequences are not completely random. In the pseudo-random sequences generated by the LFSR, any two vectors before the (2^n-1)th vector are not the same (n is the bit number of the LFSR). Namely, the vector applied to the CUT will not be the same as any previous vector. Here we assume that the primary input number of the CUT is equal to n, because in this case, the pseudo-random sequences have the best effectiveness for single stuck-at faults. However, for the random sequences, the next vector applied to the CUT will, possibly, be the same as the previous vectors with a certain probability. Then, what is the dissimilarity between the random and pseudo-random sequences? Firstly, we define the aliasing fault coverage between the random and pseudo-random input sequences as follows.

Definition 1: Aliasing fault coverage: The aliasing fault coverage between the random and pseudo-random input sequences used in testing the logic circuits is the fault coverage difference between the random and the pseudo-random sequences, given the input sequence length m.

Supposed that the fault coverage for the random sequences is denoted as C_r, while the fault coverage for the pseudo-random sequences is denoted as C_p. Then, the aliasing fault coverage C_a is represented as

$$C_a = C_r - C_p . \quad (1)$$

Formula (1) shows if C_a is larger than 0, the testing quality of the random sequences is better than that of the pseudo-random

sequences; otherwise, the testing quality of the random sequences is worse than that of the pseudo-random sequences.

For the pseudo-random sequences, the mean fault coverage of the first vector is

$$C_{p1} = \int_0^1 xp(x)dx\,, \tag{2}$$

where x is the testability of the detectable faults, and p(x) is the distribution of the testabilities of the detectable faults in a circuit [14]. Then, the fault coverage of two vectors is

$$C_{p2} = C_{p1} + \int_0^1 x(1-x)\,p(x)dx = \int_0^1 x[1+(1-x)]p(x)dx\,. \tag{3}$$

Similarly, the fault coverage of m vectors is

$$C_{pm} = \int_0^1 x[1+(1-x)+\cdots+(1-x)^{m-1}]p(x)dx\,. \tag{4}$$

For the random sequences, the mean fault coverage of the first vector is the same as that of the pseudo-random sequences, i.e., formula (2). However, the fault coverage of two vectors is not the same as that of the pseudo-random sequences. It is because that the second vector is possibly the same as the first vector in the random sequences. Therefore, the fault coverage of two vectors is

$$C_{r2} = C_{p1} + \frac{2^n-1}{2^n}\int_0^1 x(1-x)\,p(x)dx\,, \tag{5}$$

where $(2^n-1)/2^n$ denotes the probability of disappearing the first vector in this random sequence. Possibly, the second vector is just the same as the first vector.

Thus, the aliasing fault coverage of two vectors is

$$C_{a2} = C_{r2} - C_{p2} = -\frac{1}{2^n-1}\int_0^1 x(1-x)\,p(x)dx\,. \tag{6}$$

For the random sequences, the fault coverage of 3 vectors has two cases. The first case is that the third vector repeats the first or the second vector (if the second vector is different from the first). The other is the best case where a different vector appears with the probability $(2^n-2)/2^n$. Therefore, the mean fault coverage of three vectors in the best case is

$$C_{r3} = C_{p1} + C_{p2} + \frac{2^n-2}{2^n}\int_0^1 x(1-x)^2\,p(x)dx\,. \tag{7}$$

Similarly, the fault coverage of m vectors in the best case for the random sequences is

$$C_{rm} = C_{p1}+\cdots+C_{p(m-1)} + \frac{2^n-(m-1)}{2^n}\int_0^1 x(1-x)^{m-1}\,p(x)dx\,. \tag{8}$$

For the random sequences, the fault coverage of m vectors in the worst case is

$$C_{rm} = C_{r2}\,. \tag{9}$$

Then, the aliasing fault coverage of m vectors is estimated as

$$C_{r2} - C_{pm} \le C_{am} \le -\frac{m-1}{2^n}\int_0^1 x(1-x)^{m-1}\,p(x)dx\,. \tag{10}$$

Theorem 1: The testing quality of the random sequences is worse than that of the pseudo-random sequences.

***Proof*:** In inequality (10), we can see that C_{am} is less than or equal to 0; namely, the mean fault coverage of the random input sequences is less than or equal to that of the pseudo-random sequences. Thus, the testing quality of the random sequences is worse than that of the pseudo-random sequences.□

In inequality (10), we can also see that, in the worst case, the absolute value of the aliasing fault coverage will increase with the increase of the input sequence length m. This implies the testing quality of the random sequences becomes worse than that of the pseudo-random sequences with the increase of m.

Fig. 1 shows the relationship of the aliasing fault coverage against the input vector number in the simplest case where p(x)=1 and n=6. The shadow part in Fig. 1 is the area between the best and worst aliasing fault coverage curves.

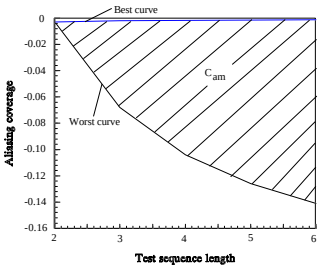

Fig.1. The aliasing fault coverage vs the input vector number

Table 1 shows the simulation results for circuit c17, one of the ISCAS-85 benchmark circuits [15], where SL is the input sequence length. In table 1, it is clear that the testing quality of the pseudo-random sequences is really better than that of the random sequences. That is because, in the random sequences, many future vectors are the same as the previous vectors. For example, in the independent random experiment, the 11th and 12th vectors repeat the eighth and sixth vectors, respectively.

In Table 1, when SL is 1 and 2, the coverages of the pseudo-random testing are less than that of the random testing. This is because that the actual coverage of a random vector may differ from the mean coverage. However, the variance will be small for almost all circuits [14]. Meanwhile, the variance will decrease with the increase of the input sequence length.

Table 1. The fault coverage for the circuit c17

SL	Pseudo-random	Random	SL	Pseudo-random	Random
1	0.294118	0.323529	8	0.911765	0.794118
2	0.323529	0.352941	9	0.911765	0.823529
3	0.588235	0.441176	10	1.000000	0.823529
4	0.735294	0.470588	11		0.863043
5	0.764706	0.735294	12		0.863043
6	0.852941	0.735294	13		0.970588
7	0.882353	0.764706	14		1.000000

Fig. 2 shows a combinational circuit for a 4-bit comparator that has 9 inputs and 3 outputs [16]. Fig. 3 shows the curves of the mean fault coverage vs. the input sequence length for the pseudo-random testing and the random testing, respectively. In Fig. 3, we can also obtain the same conclusion as theorem 1.

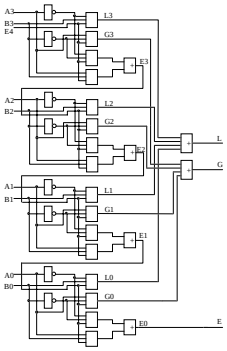

Fig.2 A 4-bit comparator circuit

The natures of the pseudo-random and random sequences for the permanent faults has been analyzed. Then, what is their influence on the intermittent faults of logic circuits? In the next section, we will discuss this problem.

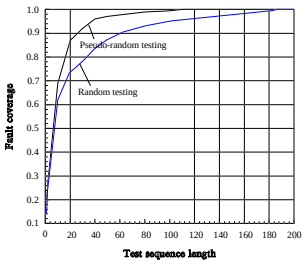

Fig.3 Fault coverage vs. input sequence length

III Intermittent fault testing

Papers [16,17] proposed the retry policy on the intermittent fault detecting. The testing process of the retry policy is divided into 2 phases.

In phase 1, the random input vectors are applied until a fault is detected. In phase 2 (retry phase), the same input vector is applied for some times to determine the fault type (permanent or intermittent).

However, in this scheme, the influence of the random and pseudo-random sequences on the intermittent faults is not considered, and the mean intermittent fault coverage and the self-test circuit design are not discussed.

In fact, inequality (10) is also suitable for the intermittent faults after considering the activity probabilities of the intermittent faults, due to the usage of the retry policy in detecting the intermittent faults. For the intermittent faults, inequality (10) is slightly modified as follows

$$\alpha(C_{r2} - C_{pm}) \le C_{am} \le \alpha(-\frac{m-1}{2^n}\int_0^1 x(1-x)^{m-1} p(x)dx), \qquad (11)$$

where α is the mean activity probability of the considered intermittent faults in a circuit.

Theorem 2: The testing quality of the random sequences is worse than that of the pseudo-random sequences for the intermittent faults in a circuit.

Proof: Because α is greater than 0 in inequality (11), C_{am} is less than or equal to 0. Therefore, theorem 2 is correct in terms of theorem 1. □

We made the simulation for the intermittent faults for the c17 circuit and the circuit shown in Fig. 2. Fig. 4 shows the simulation results, which represent the relationship between the input sequence length and the mean fault activity probability for reaching the fault coverage 1.0 for the circuit c17. Fig. 5 shows the simulation results of the mean fault coverage against the input sequence length in the condition where the mean fault activity probability is equal to 0.60 for the circuit shown in Fig 2. In this paper, we only consider the first time appearance of the intermittent faults in the circuit, because the retry policy to be described in the next section is used in detecting the intermittent faults. In Figs. 4 and 5, we can also see that the testing quality of the pseudo-random sequences is better than that of the random sequences for the intermittent fault testing.

IV Self-test design for the intermittent faults

Since the testing quality of the pseudo-random sequences is better than that of the random sequences for the intermittent fault testing, we use the BIST techniques to design self-test circuits for a 5-input CUT, which possibly contains the intermittent faults. Fig. 6 is the generator of the pseudo-random sequences and the same test vector repetition, and Fig. 7 is a self-test circuit of the intermittent faults.

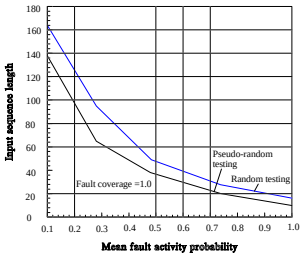

Fig.4. The input sequence length vs. the fault activity probability for fault coverage 1.0

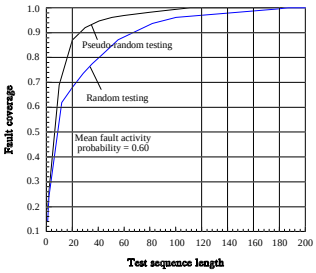

Fig.5. The fault coverage vs. the input length under α =0.6

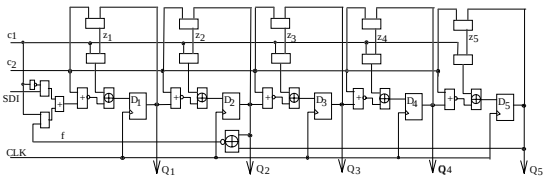

Fig.6. The generator of the pseudo-random sequence and of the same vector repetition

In Fig. 6, SDI is the scan input; CLK is the clock; c1 and c2 are the control inputs; Q_i is the output, which is connected to the input of the CUT correspondingly.

The operation modes of the generator are shown below.

(1) Set state, if c1=0, c2=1. The input value of each D flip-flop is equal to 0.

(2) Scan state, if c1=0, c2=0. $D_i = Q_{i-1}$, $D_1 = \overline{SDI}$.

(3) Generator state, if c1=1, c2=0. The pseudo-random sequences are generated in this state.

(4) Repetition state, if c1=1, c2=1. $Q_i^t = Q_i^{t-1}$, where t denotes the time. In this state, the generator can be used to repeat the same test vector.

In Fig. 7, CM is the comparator, subtracter is a counter that decreases by 1, the gold value is the reference value obtained from a corresponding fault-free circuit.

The testing process is shown below.

(1) When c1=1, c2=0, and c3=1, the LFSR generates the pseudo-random sequences that are applied to the input of the CUT. CM is used to compare the CUT output responses with the gold value. If the two values are the same, CM output is 0, which makes LED green. If the two values are different, CM output is 1, which makes LED red. In the red case, the CUT is considered as faulty. Meanwhile, the signal S puts the number L of the repetition of the same test vector into the subtracter and lets c2 become 1. At this time, the self-test circuit is in the mode of the same test vector repetition.

(2) The same test vector continues to be applied to the CUT. As soon as LED becomes green, i.e., the CUT output response is the same as the gold value. The fault in the CUT disappears. Then, the fault in the CUT is considered an intermittent fault. At the same time, the signal S locks the CLK. On the other hand, if the number L of the repetition of the same test vector in the subtracter is decreased to 0, the output signal F produced by the subtracter also locks the CLK. Then, the fault in the CUT is considered a permanent fault.

Note that c2 and c3 will be controlled by the internal signals in the self-test circuit after starting self-testing.

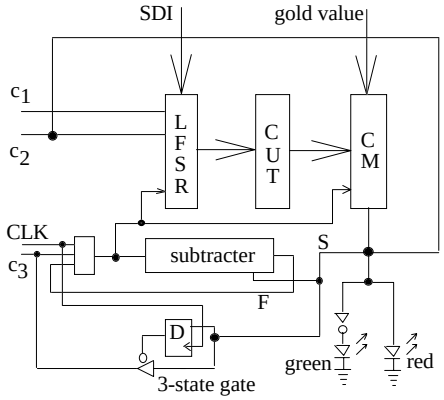

Fig.7. Self-test circuit

In the retry policy, two problems have to be resolved. The first is to determine the input sequence length used to tell whether the circuit is faulty. The other is to determine the number of the repetition of the same test vector to decide whether the circuit fault is intermittent. The first problem has been resolved in paper [18]. The second depends on the confidence.

Definition 2: Confidence of fault type: The confidence of fault type is the trustful degree to consider a fault in a circuit as the permanent or the intermittent fault.

In order to resolve the second problem, the Markov chains [16] are used to describe the testing process. In the chains, we can derive the following formula.

$$P_c = 1 - P_f^{L-1}(1 - P_f), \qquad (12)$$

where P_c is the confidence to consider the fault f as a permanent fault, P_f is the activity probability of the fault f, and L is the number of the repetition of the same test vector. The fault activity probability can be obtained from the number L.

For example, If the confidence is 0.999999999 and the fault activity probability P_f is greater than 0.9999999, the number L of the repetition of the same test vector is greater than 4.6×10^7. In this case, the fault f is considered as a permanent fault; otherwise, the fault f is considered as an intermittent fault.

V Conclusions

In this paper, we analyzed the testing quality of the pseudo-random and random input sequences. The theoretical and simulation results show that the testing quality of the pseudo-random sequences is better than that of the random sequences, and the aliasing fault coverage between the random and pseudo-random sequences will increase with the increase of the input sequence length in the worst case. We also discussed the influence of the mean activity probability of the intermittent faults on the mean fault coverage. Given an input sequence length, the fault coverage will decrease with the decrease of the fault activity probability. We designed the functional circuits of the pseudo-random self-testing of the intermittent faults. Moreover, the test sequence length used to classify the intermittent and permanent faults was estimated. The experiments based on real circuits containing the permanent and intermittent faults show that the simulation results agree with the analytical models.

Acknowledgment

This paper is partially supported by the Hong Kong RGC Earmarked Grant No. CUHK4163/97E.

References

[1] Sanjay Gupta and et. al., Arithmetic additive generators of pseudo-exhaustive test patterns. *IEEE Trans. Computers*, Vol.45, No.8, pp.939~949, 1996.

[2] Keiho Akiyama and Kewal K. Saluja, A method of reducing aliasing in a built-in self-test environment. *IEEE Trans. Computer-aided design*, Vol.10, No.4, pp.548~553, 1991.

[3] Chih-Ang Chen and Sandeep K. Gupta, BIST test pattern generators for two-pattern testing--theory and design algorithms. *IEEE Trans. Computers*, Vol.45, No.3, pp.257~269, 1996.

[4] R.G.Bennetts, Design of testable logic circuits. *Addison-Wesley Publishing Company*, 1984.

[5] Patrick P. Gelsinger, Design and test of the 80386. *IEEE Design & Test*, pp.42~50, June, 1987.

[6] Maurizio Damiani and et. al., Aliasing in signature analysis testing with multiple input shift registers. *IEEE Trans. Computer-aided Design*, Vol.9, No.12, pp.1344~1353, 1990.

[7] Krishnendu Chakrabarty and John P.Hayes, Test response compaction using multiplexed parity trees. *IEEE Trans. Computer-aided Design*, Vol.15, No.11, pp.1399~1996, 1996.

[8] Konstantinos I. Diamantaras and Niraj K. Jha, A new transition count method for testing of logic circuits. *IEEE Trans. Computer-aided Design*, Vol.10, No.3, pp.407~410, 1991.

[9] Ding Jin and Hu Jian-dong, State-difference count and its confidence estimation. *Acta Electronica Sinica*, Vol.23, No.7, pp.41~45, 1995.

[10] Dan Li and Wen-Ben Jone, Pseudorandom test-length analysis using differential solutions. *IEEE Trans. Computer-aided Design*, Vol.15, No.7, pp.815~825, 1996.

[11] E.J.McCluskey and et. al., Probability models for pseudorandom test sequences. *IEEE Trans. Computer-aided Design*, Vol.7, No.1, pp.68~74, 1988.

[12] K.D.Wagner and et. al., Pseudorandom testing, *IEEE Trans. Computers*. Vol.C-36, No.3, pp.332~343, 1987.

[13] Cary K.Chin and Edward J.McCluskey, Test length for pseudorandom testing. *IEEE Trans. Computers*, Vol.C-36, No.2, pp.252~256, 1987.

[14] Sharad C.Seth and et. al., A statistical theory of digital circuit testability. *IEEE Trans. Computers*, Vol.39, No.4, pp.582~585, 1990.

[15] F.Brglez and H.Fujiwara, A neutral netlist of 10 combinational benchmark designs and a special translator in Fortran. *In Proc. International Symposium on Circuits and Systems*, June 1985.

[16] Asad A. Ismaeel and Rakesh Bhatnagar, Test for detection & location of intermittent faults in combinational circuits. *IEEE Trans. Reliability*, Vol.46, No.2, pp.269~274, 1997.

[17] T-H Lin and K.G.Shin, An optimal retry policy based on fault classification. *IEEE Trans. Computers*, Vol.43, No.9, pp.1014~1025, 1994.

[18] Ding Jin and Hu Jiandong, On Shortening of Test Sequence Length for Signature Analyzer. *Journal of Electronics (China)*, Vol.12, No.2, pp.151~159, 1995.