On the Trap Assisted Stress Induced Safe Operating Area Limits of AlGaN/GaN HEMTs

Bhawani Shankar[1], Ankit Soni[1], Sayak Dutta Gupta[1], R. Sengupta[1], H. Khand[1], N. Mohan[2], Srinivasan Raghavan[2] and Mayank Shrivastava
[1]Department of ESE, [2]Center for Nanoscience & Engineering
Indian Institute of Science, Bangalore, India, mayank@.iisc.ac.in

***Abstract*—This experimental study reports a systematic investigation of Safe Operating Area limits in AlGaN/GaN HEMT using sub-µs pulse characterization with on the fly Raman and CV characterization to probe defect and stress evolution across the device. Influence of a recess depth on SOA boundary is analyzed. Post failure analysis corroborates well with the failure physics unveiled in this work.**

***Index Terms*—GaN HEMT, Safe Operating Area, Stress, Trap**

I. Introduction

The outstanding properties of Gallium Nitride (GaN) such as wide bandgap (3.4 eV), high breakdown field (3.3 MV/cm), good thermal conductivity (1.3 W/cm^2-K) and low dielectric constant (9) have triggered the replacement of Si by GaN in power device applications. GaN based high electron mobility transistor (HEMT) have shown outstanding performance in high power and high frequency domain [1]. Despite the attractive performance/cost ratio, poor reliability of GaN HEMT is a major hurdle to its large-scale penetration in power device market. Therefore, reliability of AlGaN/GaN HEMT is now a topic of intense research. Long term reliability of these devices has been studied in greater details in the recent literature [1]-[7]. However, a clear understanding of the physical phenomena active under high electric field and high current injection conditions, which define the safe operating area (SOA) limit in GaN HEMT, is still missing in the literature [8],[9]. Therefore, a study to gain insight into possible degradation mechanisms which limit the SOA reliability in GaN HEMT is a worthwhile effort. The present experimental study aims to systematically investigate the evolution and influence of mechanical stress and defects across AlGaN/GaN system, using on the fly Raman spectroscopy during high field and current stress. Raman spectroscopy has been widely used for thermal analysis [10]-[13] and stress distribution studies [14]-[16] in GaN HEMT. For the first time, in this work, Raman spectroscopy is used to probe dynamics of trap induced stress which limits the SOA boundary in AlGaN/GaN HEMT. Impact of various technology parameters on SOA reliability is studied. TCAD simulation and post failure analysis of devices provide insight into the degradation physics.

II. Device Fabrication and Processing

AlGaN/GaN HEMTs were fabricated on the layer stack as shown in Fig. 1, which was grown on Si (111) using MOCVD, with and without carbon doping in buffer. Ti/Al/Ni/Au metal stack was deposited using e-beam evaporation and later annealed at 870°C to realize source/drain Ohmic contacts. Devices were MESA isolated on wafer using Chlorine chemistry by Inductively Coupled Plasma - Reactive Ion Etching. O_2/BCl_3 based atomic layer etching was employed to achieve controlled gate recess. D-mode and E-mode devices with varying recess depths were fabricated. Post dielectric deposition and dielectric anneal, Ni/Au gate was deposited followed by soft anneal. All the devices consist of dielectric passivation and field plate.

III. Device Characterization

Pulse I-V characterization of HEMT devices was done using pulses of 100 ns duration with 1 ns rise time to determine the SOA boundary and failure threshold. Sub-bandgap UV (365 nm) assists in carrier de-trapping in GaN. Therefore, devices were tested under dark or with UV to study the impact of trapping on SOA reliability. After each pulse, linear drain to source dc current (I_{DS}) was spot measured at small dc bias to monitor device degradation. DC I-V and capacitance-voltage (C-V) characterization was done at regular intervals between stress routine to record the change, if any, in device parameters and capture the evolution of traps in different regions of the device with stress. Raman peaks native to GaN, shift with mechanical/electrothermal strain. Therefore, 2D stress profile was recorded across source-drain region, at regular intervals during the test, using on the fly 2D Raman mapping, as depicted in Fig.1. All the experiments were conducted at room temperature.

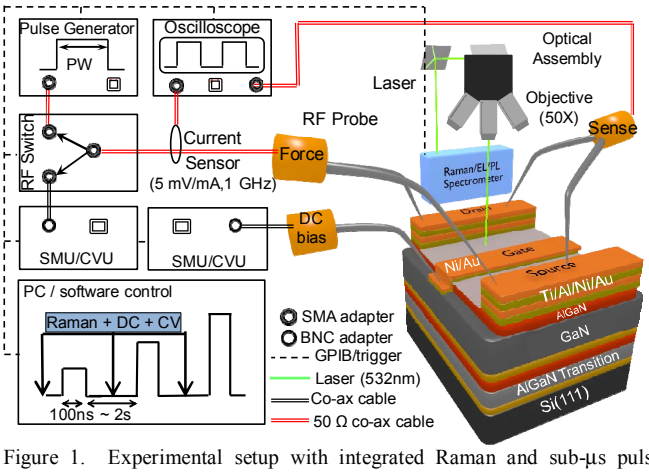


Figure 1. Experimental setup with integrated Raman and sub-µs pulse generator used for pulse IV characterization to determine SOA behavior of AlGaN/GaN HEMTs. Stress evolution in device was recorded via on the fly Raman mapping using 532nm laser.

This work was financially supported by Department of Science and Technology(DST), Govt. of India, under project grant no. DST/TSG/AMT/2015/294.

IV. Safe Operating Area

Initially, a commercial p-GaN gate E-mode HEMT was characterized to determine its SOA boundary. Figure 2(a) shows the pulse I-V characteristics with SOA. The associated degradation in spot measured drain current, under high field and high current stress conditions is depicted in Fig. 2(b). As seen, the device degraded to different extent at different gate bias, with maximum degradation in OFF-state. These results depict the importance of this study and highlight the universal nature of degradation trends presented in this work. Next, pulse I-V characterization of fabricated device was done under dark and with UV exposure, to independently determine impact of traps and self-heating on the SOA boundary as shown in Fig. 3(a). Significant improvement in SOA was observed with UV exposure, which signifies the hidden role of surface and/or buffer traps on SOA reliability. A comparison of drain current degradation trends captured in dark and UV condition, is presented in Fig. 3(b). It reveals, negligible degradation in presence of UV whereas the drain current faced significant degradation in dark. And the same observation persists at different gate bias. Possibly, UV exposure de-traps the carries trapped at different locations in the device, and mitigates the device degradation.

A. Influence of Carrier Trapping

To understand, the physics of SOA improvement with UV, in further detail, a HEMT structure was simulated in TCAD at different buffer trap concentrations. And the electric field distribution in channel was extracted in each case as shown in Fig. 3(c). It revealed that the peak electric field in the channel shifts from gate to drain edge in presence of buffer traps, which is equivalent to the case of I-V measurements done under dark. In absence of traps the electric field peaks at the gate edge which occurs when the UV exposure was present while stressing the device. Therefore, traps can modify the field distribution and hereby potentially govern the device degradation via field driven mechanisms like inverse piezoelectric effect and influence the SOA boundary of AlGaN/GaN HEMTs. Here, effect of surface states is not studied, as the devices used in this study were passivated.

B. Influence of Stress

Now, as it is clear that traps can modify the field distribution in GaN HEMT, one would be curious to study its impact, if any, on the mechanical stress introduced in the device via inverse piezoelectric effect. A device was stressed under dark and UV conditions. 2D map of the stress distribution in source to drain region was recorded using on the fly Raman spectroscopy at regular intervals during the stress. Figure 4(a) shows the Raman map recorded in the pristine device, before stress that is under zero bias condition. It unveils the presence of high compressive stress under the gate finger. Then the device is stressed in OFF-state, under dark condition and the corresponding stress map is shown in Fig. 4(b). It reveals that compressive stress builds up at the drain edge and in drift region, under the dark condition. On the other hand, with UV illumination compressive stress was missing in the drain and drift region, and it was present only under the gate as depicted in Fig. 4(c). This result corroborates well with observation of trap induced field shift in GaN HEMT. Compressive stress develops at the drain edge due to excessive trapping, which shifts the peak electric field from gate to drain edge. UV exposure de-trapped the carriers and restored the peak stress to the gate finger. When the device is stressed under ON state, Raman peaks for GaN; $E_{2\text{-}H}$ (567.5 cm^{-1}) and $A_{0\text{-}L}$ (735 cm^{-1}), shift towards left with increasing stress at the drain as depicted in Fig. 4(d). This unveils that the tensile stress at the gate edge towards drain, increases with drain voltage. The increased mechanical stress creates defects/cracks in gate/drift region when its elastic energy hits a critical value [17]. DC I-V and C-V measurement were done at regular intervals during the test. Trap density was extracted in gate, gate-source and gate-drain regions at different stress levels. Figure 5(a) shows the variation in trap density in various regions of the device. A significant increase in trap density is noticed in the gate-drain region [9] with increasing drain stress. Here gate-to-drain trap density increases at a much higher rate than in the gate-to-source region. This is attributed to the piezoelectric stress developed in gate-drain region which generates new defects as discussed above. Moreover, a positive V_{TH} shift is observed with stress, as depicted in Fig. 5(b) and it points to accumulation of negative charge underneath gate via electron trapping. Also, the increased device R_{ON} and degraded drain current, point to electron trapping in gate-drain region.

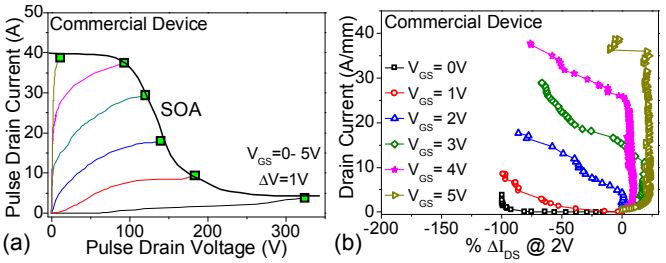


Figure 2. (a) Pulse IV characteristics of a commercial GaN device with SOA boundary marked. (b) Percentage change in linear drain current measured after each voltage pulse, at 2V dc. Severe degradation is observed at different gate bias with highest degradation (~100 %) under OFF-state.

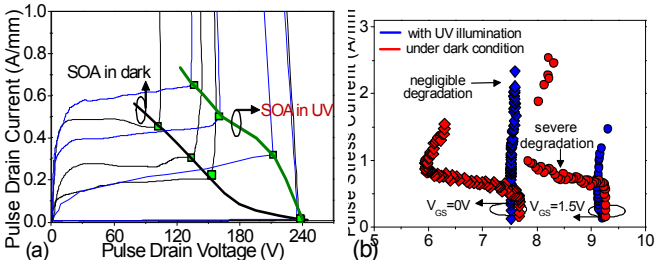
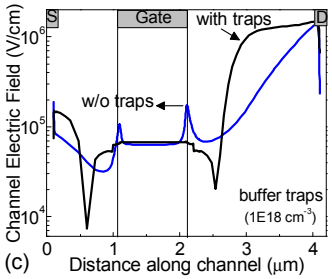


Figure 3. (a) Safe Operating Area of AlGaN/GaN HEMT under dark and UV condition. Figure highlights the trapping limits SOA boundary. (b) Comparison of degradation in linear drain current measured after each stress pulse, under dark and UV conditions. UV illumination effectively suppresses degradation by assisting in the carrier de-trapping.



(c) Simulated electric field profile in channel, with and w/o buffer traps shows peak electric field shifts from gate to drain edge in presence of traps, which is the case of test done in dark.

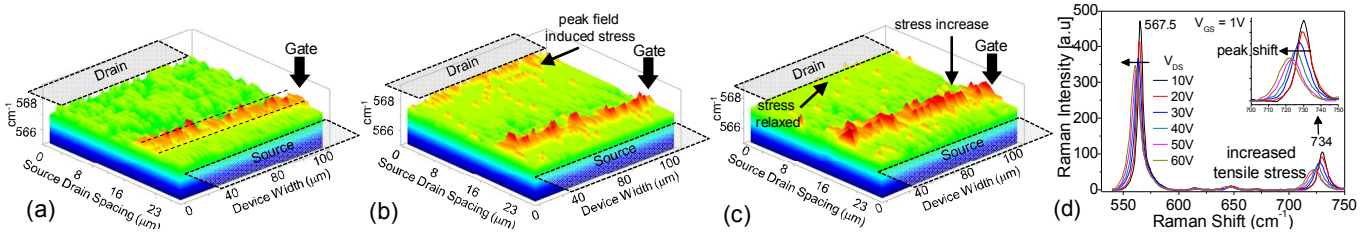


Figure 4. (a) Raman map captured in source-drain region of pristine device, before stress. Figure reveals compressive stress under gate finger possibly due to gate recess. On the fly Raman map was captured during OFF-state stress (V_{DS} 60V@ V_{GS} -6V) (b) in dark and (c) with UV illumination on device. Figure (b) shows stress accumulates at drain edge when device is tested under dark condition, while stress builds up at gate edge with UV exposure as shown in (c). In dark, trapping in buffer and barrier region, causes peak electric field to shift to drain edge as seen in simulation result (Fig. 3c). UV exposure, suppressed trapping by de-trapping carriers and restored the peak field back to gate edge as evident from increased stress at gate under UV in Fig.(c). Fig.(d) shows Raman spectra spot measured, under ON-state, at gate edge towards drain at different drain stress. Left shifting in E_2(H) (567.5 cm^{-1}) and A_1(LO) (730cm^{-1}) Raman peaks of GaN reveal increased tensile stress at gate edge with increase in drain voltage.

C. *Influence of Gate Recess*

Devices with different recess depth were characterized to determine their SOA boundary as shown in Fig. 6(a)-(d). Device without gate recess exhibited a narrower SOA as depicted in Fig. 6(a), while in devices with full recessed gate, the failure occurred at a fixed drain voltage independent of applied gate bias as seen in Fig. 6(d). This reveals field limited SOA in fully recessed structure and points to a possibility of field modulation with recess depth, as discussed later. A comparative analysis of SOA boundaries of devices with different recess depth is done as in Fig. 6(e). It reveals that SOA boundary shifts with recess depth and it can be maximized using an optimum recess depth or with a partial recessed gate. To further understand it, the linear drain current was spot measured in each case. Figure 7(a) presents a comparison of distinct degradation trends in drain current as function of gate recess depth. It unveils that the percentage degradation in the device reduces with increase in recess depth. Devices without recess undergo up-to 30% degradation in drain current, while devices with 15 nm recess depth degrades only up-to 10%. On the other hand, fully recessed devices suffered from maximum degradation of 90%. To understand the underlying physics, TCAD simulation of a device was done for different gate recess depth and variation in electric field distribution in channel, is determined for different recess depths as depicted in Fig. 7(b). It shows that in case of non-recessed or fully recessed structure, the electric field peaks at either the gate or drain edge. However, for intermediate optimum recess depth, the field redistributes such that peak field gets suppressed both on gate and drain edges.

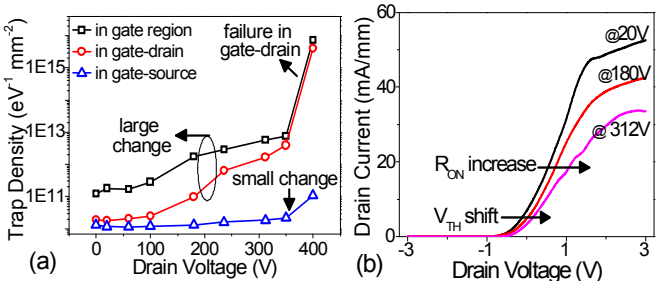


Figure 5. (a) Increase in trap density captured after each stress voltage pulse. Rapid increase in trap density in gate-drain region can be seen. (b) Transfer characteristics of HEMT recorded at regular intervals during the test shows shift in threshold voltage and increase in R_{ON} with increase in drain stress.

Field suppression at drain reduces impact ionization rate and avoids early avalanche in device. Low field at gate, slows the hotspot formation and hot electron induced degradation. Therefore, redistribution of channel field with suppressed peaks at optimum recess depth, improves device reliability and broadens the SOA. This explains the as observed dependence of SOA on recess depth. in this work.

V. Failure Analysis

After pulse characterization, the damaged regions of failed devices were analyzed using Scanning Electron Microscopy (SEM), Energy Dispersive X-Ray Spectroscopy (EDX) and Transmission Electron Microscopy (TEM) to gain physical insight into the underlying degradation mechanism. Figure 8(a) shows the post failure SEM micrograph of a device which failed in OFF-state under UV condition. It depicts a part of gate metal finger blown-off at failure without any trace of material melting. This highlights the possibility of purely field driven failure. Presence of cracks underneath gate, towards drain side, reveal that the damage occurred due to high mechanical stress at gate edge. This observation nicely corroborates with the Raman stress map shown in Fig. 4(c) where the region under gate finger was found to be always under a compressive stress. The inverse piezoelectric effect introduces mechanical strain at gate because the channel electric field peak peaks at the gate edge in absence of carrier trapping as revealed by TCAD results in Fig 3(c). SEM image of a device which failed at a stress of 10 ns pulse duration is shown in Fig. 8(b). It unveils multiple damages formed along the gate edge in the gate-drain region. MOCVD grown AlGaN/GaN stack, possess a finite defect density which can introduce non-uniformity in carrier trapping and associated peak field shift, at drain, along the device width. Enhanced impact ionization and carrier injection into the buffer, in these localized high field regions invokes avalanche instability and causes multiple damages [9] as seen in Fig. 8(b). Figure 8(c) shows post failure SEM image of a device which faced premature breakdown under ON-condition. It reveals, presence of a pit triggered device failure in gate-source region. Pits and dislocations are native to AlGaN/GaN material system and originate from lattice mismatch between different layers. Post failure SEM image of device which was

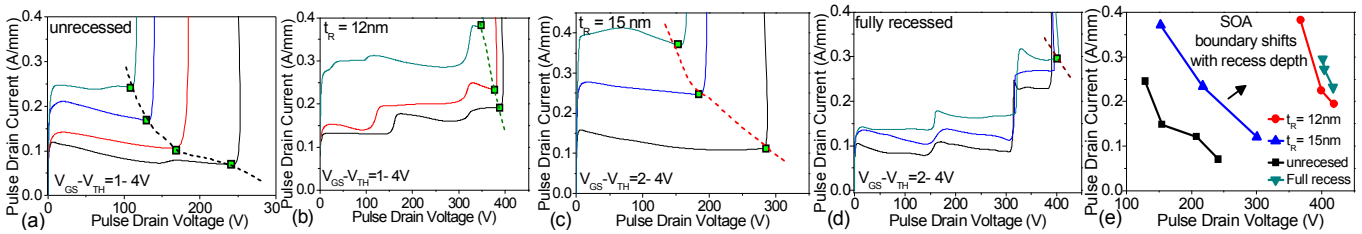


Figure 6: SOA boundary of devices with different recess depth (t_R). (a) Figures shows narrow SOA boundary in HEMT without (b)-(d) shows SOA of devices with increasing recess depth. Figure reveals that with gate recess the SOA broadens however, with fully recessed gate as in (d) device failure occurred at a fixed drain voltage independent of gate bias and reveals field limited SOA in recessed structure. (e) Shift in SOA boundary with recess depth is observed, with optimum SOA achieved with 15nm recess depth.

failed under OFF-state is shown in Fig. 8(d). It shows failure occurred with a crack in gate-drain region and gate metal folding exclusively at the drain side gate edge. Metal melting/folding reveals the thermal nature of the failure. TEM cross-section was taken along the gate edge (white dotted line in Fig. 8d). It unveils the presence of a dislocation at the gate edge, as shown in Fig. 8(d1), which caused failure. The cross-sectional image in Fig. 8(d2) also reveals that the damage occurred deep in the buffer with the newly formed crack reaching till the Si substrate. This can be explained as follows; dislocations provide parasitic path for current leakage and material diffusion. This weakens the material strength via electro-chemical reactions [18] and creates local damages.

VI. Conclusion

This work investigates influence of key technology parameters on the SOA limits of AlGaN/GaN HEMTs. SOA boundary in OFF-state was found to deteriorate due to compressive stress at drain-gate edge. Carrier trapping shifts peak electric field towards drain which results in stress accumulation at drain edge. ON-state SOA limited by tensile stress in the gate-to-drain region. Increased stress leads to defect generation and increased trap density in gate-drain region. OFF-state failure was found to be field driven while ON-state failure exhibited thermal nature. We found that electric field profile in channel and buffer can be tuned by controlling the recess depth, which directly affects device degradation and the SOA boundary in AlGaN/GaN HEMTs.

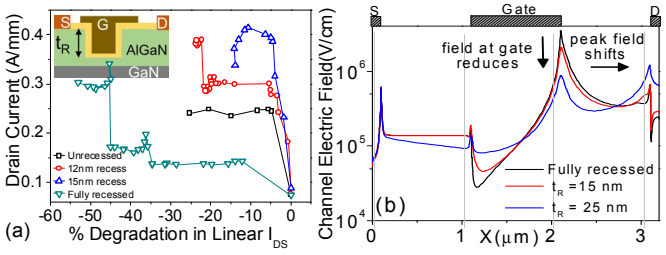


Figure 7. (a) Inset shows schematic of HEMT with recessed gate where recess depth (t_R) is varied. Percentage degradation in linear drain current for devices of different recess depth, drain stressed under ON-state (V_G-V_{TH}=2V). Maximum degradation occurs in device with full recess and least occurs in device with 15nm recess depth. (b) TCAD simulation for different recess depth shows electric field peaks at gate edge in unrecessed structure. With increase in recess depth, peak field shifts to drain edge for 25nm recess depth. 15nm partial recess, suppresses peak at both gate and drain edge and improves SOA

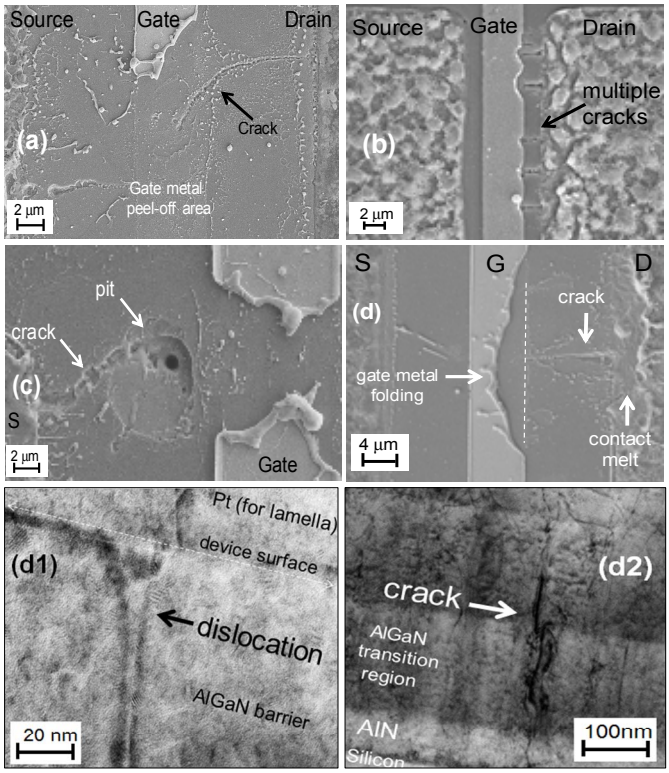


Figure 8. (a) Post failure SEM image of device failed in On-state. Figure shows cracking underneath gate blew-off the gate finger which was already under compressive stress as clear from Raman plots. (b) Multiple damages observed in gate-drain region reveal failure due to non-uniform trapping and stress distribution along device width as shown in Fig. 4a-c. Defects like pit can trigger failure as shown in (c). On-state failure in (d) occurred with crack in gate-drain region with gate metal folding. TEM cross-section taken along gate edge (white dotted line) shows presence of dislocation at gate edge, as shown in (d1) and crack in buffer reaching till Si substrate as in (d2).

Acknowledgment

Authors acknowledge IISc GaN team for fruitful discussions. This work was funded by Department of Science and Technology(DST), Govt. of India, under project grant no. DST/TSG/AMT/2015/294.

References

[1] G. Meneghesso et al., "Reliability of GaN High-Electron-Mobility Transistors: State of the Art and Perspectives," *IEEE Transactions on Device and Materials Reliability*, vol. 8, no. 2, pp. 332-343, June 2008.

[2] J.A. del Alamo, J. Joh, “GaN HEMT reliability,” *Microelectronics Reliability*, vol. 49, pp. 1200-1206, 2009.

[3] R. Vetury, N. Q. Zhang, S. Keller and U. K. Mishra, "The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs," *IEEE Transactions on Electron Devices*, vol. 48, no. 3, pp. 560-566, Mar 2001.

[4] S. C. Binari *et al*., "Trapping effects and microwave power performance in AlGaN/GaN HEMTs," *IEEE Transactions on Electron Devices*, vol. 48, no. 3, pp. 465-471, Mar 2001.

[5] G. Meneghesso, F. Rampazzo, P. Kordos, G. Verzellesi and E. Zanoni, "Current Collapse and High-Electric-Field Reliability of Unpassivated GaN/AlGaN/GaN HEMTs," *IEEE Transactions on Electron Devices*, vol. 53, no. 12, pp. 2932-2941, Dec. 2006

[6] J. Joh and J. A. del Alamo, "A Current-Transient Methodology for Trap Analysis for GaN High Electron Mobility Transistors," *IEEE Transactions on Electron Devices*, vol. 58, no. 1, pp. 132-140, 2011.

[7] J. Joh and J. A. del Alamo, "Critical Voltage for Electrical Degradation of GaN High-Electron Mobility Transistors," *IEEE Electron Device Letters,* vol. 29, no. 4, pp. 287-289, April 2008

[8] Xing Huang, Dong Young Lee, Volodymyr Bondarenko, Art Baker David C. Sheridan, Alex Q. Huang and B. Jayant Baliga, "Experimental study of 650V AlGaN/GaN HEMT short-circuit safe operating area (SCSOA)," in *Proc. 2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC's*, Waikoloa, HI, pp. 273-276.

[9] Bhawani Shankar, Ankit Soni, Manikant Singh, Rohith Soman, Hareesh Chandrasekar, Nagaboopathy Mohan, Neha Mohta, Nayana Ramesh, Shreesha Prabhu, Abhay Kulkarni, Digbijoy Nath, R. Muralidharan, K. N. Bhat, Srinivasan Raghavan, Navakant Bhat and Mayank Shrivastava, "Trap assisted avalanche instability and safe operating area concerns in AlGaN/GaN HEMTs," in *Proc. 2017 IEEE International Reliability Physics Symposium*, Monterey, CA, pp. WB-5.1-WB-5.5.

[10] Kuball, M., Riedel, G. J., Pomeroy, J. W., Sarua, A., Uren, M. J., Martin, T., Hilton, K. P., Maclean, J. O., and Wallis, D. J., “Time-Resolved Temperature Measurement of AlGaN/GaN Electronic Devices Using Micro-Raman Spectroscopy,” *Electron Devices Letters* vol. 28, no. 2, pp. 86-89, Feb. 2007.

[11] Andrei Sarua, Hangfeng Ji, Martin Kuball, Michael J. Uren, Trevor Martin, Keith P. Hilton, and Richard S. Balmer, "Integrated micro-Raman/infrared thermography probe for monitoring of self-heating in AlGaN/GaN transistor structures," *IEEE Transactions on Electron Devices*, vol. 53, no. 10, pp. 2438-2447, Oct. 2006.

[12] M. Nazari, B. L. Hancock, E. L. Piner and M. W. Holtz, "Self-Heating Profile in an AlGaN/GaN Heterojunction Field-Effect Transistor Studied by Ultraviolet and Visible Micro-Raman Spectroscopy," *IEEE Transactions on Electron Devices*, vol. 62, no. 5, pp. 1467-1472, May 2015.

[13] N. Killat, M. Montes, J. W. Pomeroy, T. Paskova, K. R. Evans, J. Leach, X. Li, Ü. Özgür, H. Morkoç, K. D. Chabak, A. Crespo, J. K. Gillespie, R. Fitch, M. Kossler, D. E. Walker, M. Trejo, G. D. Via, J. D. Blevins, and M. Kuball, "Thermal Properties of AlGaN/GaN HFETs on Bulk GaN Substrates," *IEEE Electron Device Letters*, vol. 33, no. 3, pp. 366-368, March 2012.

[14] S. Choi, E. R. Heller, D. Dorsey, R. Vetury and S. Graham, "Thermometry of AlGaN/GaN HEMTs Using Multispectral Raman Features," *IEEE Transactions on Electron Devices*, vol. 60, no. 6, pp. 1898-1904, June 2013.

[15] A. Sarua and Hangfeng Ji and M. Kuball and M. J. Uren and T. Martin and K. J. Nash and K. P. Hilton and R. S. Balmer, “Piezoelectric strain in AlGaN/ GaN hetero-structure field-effect transistors under bias,” *Applied Physics Letters*, vol. 88, no. 10, pp. 103502, 2006.

[16] M. Power and J. W. Pomeroy and I. Chatterjee and D. M. Risbud and B. Wynne and M. A. Gajda and J. Šonský and K. D. Pedrotti and M. J. Uren and M. Kuball, “Reverse-biased induced mechanical stress in AlGaN/GaN power diodes,” in *Proc. 2016 28th International Symposium on Power Semiconductor Devices and ICs,* Prague, pp. 103

[17] J. Joh, J. Del Alamo et al., “Critical voltage for electrical degradation of gan high-electron mobility transistors,” *Electron Device Letters*, *IEEE*, vol. 29, no. 4, pp. 287–289, 2008.

[18] M. Kuball, M. Tapajna, R. J. Simms, M. Faqir, and U. K. Mishra, “Algan/gan HEMT device reliability and degradation evolution: Importance of diffusion processes,” *Microelectronics Reliability*, vol. 51, no. 2, pp. 195 – 200, 2011.