On the way to large–scale and high–resolution brain–chip interfacing

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Abstract

Brain-chip-interfaces (BCHIs) are hybrid entities where chips and nerve cells establish a close physical interaction allowing the transfer of information in one or both directions. Typical examples are represented by multi-site-recording chips interfaced to cultured neurons, cultured / acute brain slices, or implanted "in vivo". This paper provides an overview on recent achievements in our laboratory in the field of BCHIs leading to enhancement of signals transmission from nerve cells to chip or from chip to nerve cells with an emphasis on in-vivo interfacing, either in terms of signal-to-noise ratio or of spatiotemporal resolution. Oxide-insulated chips featuring large-scale and high-resolution arrays of stimulation and recording elements are presented as a promising technology for high spatiotemporal resolution interfacing, as recently demonstrated by recordings obtained from hippocampal slices and brain cortex in implanted animals. Finally, we report on an automated tool for processing and analysis of acquired signals by BCHIs.

1. Introduction

1.1. Towards a definition of Brain-Chip-Interface (BCHI)

The use of on-chip microelectromechanical systems (MEMS) in the biomedical field has gained increasing attention in recent years. The continuous improvement of micromachining and microelectronics technologies and simultaneous deepening of knowledge about cellular and molecular mechanisms in life sciences are driving development of new generations of MEMS serving as scientific, diagnostic and therapeutic tools. Microchips for multi-site recording of neuronal activity

were among the first to be introduced [1] and are now representing an expanding technology [2, 3] where there is still great potential for novel applications. Since its infancy, the technology underwent a progressive development and is now widely adopted by neuroscientists for recording living neurons "in vitro". More recently, we have assisted to the increasing usage of implantable microchips as neuronal probes for investigating brain circuits "in vivo" while, in parallel, their potential for neuroprosthetics application has been successfully demonstrated in non-human primates [4] and assessed in clinical trials in paralyzed patients [5].

The multiplication of approaches and application examples that are based on chip-to-brain interaction and communication has led us to attempt the formulation of a comprehensive definition for this class of hybrid devices. BCHI is proposed as the term identifying those hybrid systems where electronics-based micromachined devices can establish communication pathways through close physical interaction with brain cells, either "in vitro" or "in vivo" (Fig. 1).

Despite the fact the most BCHIs are based on electrical signaling between neurons and microelectronics sensors, the definition is wide-range and comprehensive of other technological approaches. It includes, for example, other physical means of information exchange, such as those based on chemical or optical signals. In addition, the definition is taking into account that interfacing to brain cells can occur at different levels, either of individual cells or ensembles, and that communication can be uni- or bi-directional, allowing scientists to explore new concepts of cognitive processing and / or capabilities of the brain opening a new door to cognitive research.

1.2. Levels of brain-chip interfacing

At least three basic levels of brain-chip interfacing are identified on the basis of the dimensional scale of the biological entities involved: neurons, tissue and brain [2]. At present, neurons are most frequently interfaced to metal microelectrodes [1] or oxide-insulated electrical microtransducers (e.g. Electrolyte-Oxide-Semiconductor Field Effect Transistors, EOSFETs or Electrolyte-Oxide-Semiconductor Capacitors, EOSCs) to record or stimulate their electrical activity in dissociated cultures [2, 6–7]. This first-level of interfacing implies that single cells are contacting and signaling to cell-sized microdevices. A recent and original example of such a BCHI was proposed by Hai et al.

where a tight electrical coupling between neurons and chip was achieved through gold micro-nail shaped microelectrodes that were engulfed by neurons through a phagocytosis-like mechanism [8]. Also, large-scale high-resolution recordings from individual neurons in a network can be obtained, thanks to chips featuring large Multi Transistor Arrays (MTAs) as demonstrated with neuronal networks in vitro [9].

A second level of interfacing implements the concept of establishing an interaction with the brain tissue. This is achieved, usually, by placing a tissue slice a several hundred micrometers thick in contact with the chip. Recently, high resolution recording from brain slices of the rat hippocampus was performed this way by Fromherz and coworkers [10]. In these cases, individual microdevices sample the activity of a population of cells rather than of single neurons. Signals are in the form of local field potentials (LFPs), multi-unit or single-unit (spikes) activity. In general, even if single-units can be detected and identified, they originate from activity of several neurons distributed in the proximity of the sensor and can be reduced, therefore, to a population recording scheme.

Finally, the third level of interfacing is represented by chip implants in the brain or other parts of the nervous system, such as spinal cord, peripheral nerves or sensory organs. To this respect, recent results show that high-resolution recording from the rat brain somatosensory cortex can be performed using MTAs [11].

1.3. Existing technologies and chips for neural tissue interfacing

Aiming for (in-vitro) neural tissue interfacing simultaneously at a number of sites distributed in space [12], extracellular recording and stimulation techniques have been developed. There, the tissue is located in an electrolyte above the surface of a solid-state chip. The surface of the chip provides voltage-sensitive sites in a regular spatial arrangement. Moreover, between the tissue and the chip surface a cleft is formed, that, in the case of dissociated neurons in culture on the chip surface has been shown to be in the order of 50 nm using fluorescence interference contrast (FLIC) microscopy [2]. In Fig. 2, two different approaches are depicted to form the voltage-sensitive device: in Fig. 2 (a), the site is made by means of a noble metal electrode, which is connected to further signal-processing circuitry. Commercially available multi electrode arrays (MEAs) use this approach and separate a

number of such noble metal electrodes arranged within a 2D array from each other in the lateral direction by an insulating substrate material [13–14]. Ideally, noble metal electrode and electrolyte form a capacitor with a very thin so-called Helmholtz double layer capacitance. Whereas the capacitance per area is very high in that case, so that cleft-voltage coupling to the electrode is very efficient, the entire surface consists of a chemically non-homogeneous surface, as electrodes and insulating material between electrodes periodically alternate [15].

EOSFETs (Fig. 2 (b)) represent the second approach in this context [16]. There, the gate of the well-known Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) is replaced by the electrolyte above the transistor's gate dielectric, and cleft voltages induced by a firing nerve cell translate into a modulation of the transistor's drain current. This approach provides a homogeneous dielectric surface within the entire active neural tissue interfacing area. Also, a number of 2D arrays have been published [17].

In both cases, however, realization of large high-density 2D arrays is restricted by interconnect issues: only one interconnect layer is available in the bulk material which is used to make a connection between the active sites in the center of the chips to pads at the chip borders. Thus, aiming for a significant increase in spatiotemporal resolution, (extended) CMOS (Complimentary Metal-Oxide-Semiconductor) technology and chips with related circuitry have been proposed in recent years to circumvent such interconnect problems. Moreover, such chips allow provision of signal processing circuitry in closest proximity to the related recording/stimulation sites. CMOS-based noble metal electrode arrays have been published with up to 11k sites, and extended EOSFET arrays have been reported with up to 16 k and – very recently - 32 k sites [18–21]. Depending on the respective application, different design goals have been targeted: in [20], the 11 k chips provide 126 signal channels which can be selected from the entire array using a sophisticated signal routing algorithm. The chips presented in [20–21], on the other hand, always record entire frames or entire sub-frames so that a neural tissue imaging mode is obtained.

A number of recent developments are also aiming for in-vivo interfacing. Two examples of popular metal based electrodes for in-vivo interfacing are – the 'Utah probe' [22] and the 'Michigan probe' [23] (a detailed review on metal electrode for BCHI can be found in [3]). Whereas extracellular

recording and stimulation principles from the 'in vitro' approaches can be adopted, the chips developed in that context cannot simply be transferred as they are. Biggest concern is power: if the power is transferred wirelessly, the amount of available power is limited; if that is not the case (and the power is provided through a cable), the maximum power which can be consumed in live tissue is limited due to heat generation. Unfortunately, however, the number of sites and bandwidth of such a system increase the power consumption whereas the noise of a system shows an increase with decreasing power allowed per site [3].

The existing BCHI techniques face challenges mainly in terms of high space resolution (μm range) and bi-directional communication, i.e., simultaneous stimulation and recording with a single device. Though the recent development has seen some closed loop stimulation devices [24 – 26], yet, the integration of recording and stimulation sites at a higher – resolution still remains an open problem. Also, biocompatibility of the devices and robustness of recording has to improve for the stability of long-term implants. Also, due to the different neuronal network topology in different brain areas the in-vivo systems must always be carefully tailored depending on the related target application.

1.4. Tools for neuronal signal analysis

The existing chips for BCHI generate huge amount of data imposing a big challenge on the neuroscience and neuroengineering communities to process and analyze the acquired signals to infer meaningful conclusions [27–28]. To respond to this challenge sophisticated signal processing techniques are required to support the analysis of the function as well as the structure of individual neurons in the context of surrounding neuronal networks. Though individual tools are available to perform processing for the spike train analysis, spike detection and sorting, yet very few tools are available to date to process LFPs and integrate all the signal processing steps [29–30]. Also, commercially available tools for the analysis of such data cannot be easily adapted to newly emerging requirements for data analysis and visualization, and cross compatibility between them is limited.

There are a few software packages developed for academic and commercial purposes [29-50]. These software packages mainly deal with data visualization, spike detection and sorting, spike train analysis, EEG signal analysis, and cross–software platform. Also, a couple of open platforms are

under development to promote sharing of different laboratory–developed tools across the worldwide web [51–52]. However, there is no comprehensive standard tool / package to date incorporating analysis on spike trains, LFPs, and EEG. Moreover, when different software are used for the signal acquisition and signal analysis, file format conversion can be a nightmare. Also, as most of the available tools are developed for very specific analysis, often multiple packages / tools are required to perform different analyses on a single dataset which are time consuming and cumbersome. Thus an umbrella tool is required to perform processing and analysis regardless of the recorded signal types. The SigMate software package, developed in our lab, is a comprehensive tool, designed to perform processing and analyses of spikes, LFPs, and EEG signals [53–54].

2. Interfacing with the brain through E(OM)OSFET based chips

2.1. Chip description

We performed BCHI through three different generations of chips. The first two generations were high density flat chips based on EOSFETs and EOMOSFETs (Electrolyte–Oxide–Metal–Oxide–Semiconductor Field Effect Transistors [10]), whereas, the third one was a vertically implantable chip based on EOSFETs (needle chip). The two generations of flat chips were used in performing a series of experiments with a novel configuration, called, 'Rat-On-Chip' (ROC) where the anesthetized animal was placed up-side-down on the chip for performing a high resolution electrocorticogram. The third generation chip was impaled in the anesthetized animal's brain to record the brain activity.

2.1.1. EOSFET chips with 64 recording sites

These chips were based on two linear arrays of metal-free field-effect-transistors, each consisting of 31 insulated EOSFETs, spaced at 30 to 40 µm, and 32 EOSCs integrated in between two adjacent transistors (Fig. 3). The area covered by each FET was either 3.1 µm × 7.2 µm or 3.5 µm × 9.0 µm [55–56].

2.1.2. EOMOSFET chips with 128 × 128 recording sites

These chips had a size of 5.4 mm × 6.5 mm. They were wire bonded to a standard ceramics package. A perspex chamber was attached such that the active area of the chip was 1 mm × 1 mm with 128 × 128 transistors. The pitch between two adjacent transistors was 7.4 µm [9, 10, 18, 57] and

the sampling rate was 6 kS/s. Fig. 4 shows the chip with a magnification of the recording sites.

2.1.3. Implantable EOSFET chips with 4 recording sites

The needle chips were fabricated from silicon-on-insulator (SOI) wafers (4 in.) with 100 µm n-type silicon (1–10 Ω cm) and 2 µm SiO_2 on a 400 µm thick silicon substrate (SiMat, Landsberg, Germany). Each chip consisted of two parts: a needle (2 mm long) with an array of four transistors (gate area 10 µm × 10 µm, pitch 80 µm, Fig. 5, left) and a contact plate with the bond pads [58]. For stability reasons, the chips of the prototype series were relatively massive with a thickness of 100 µm and a width of 360 µm. A rather blunt shape of the tip was fabricated in order to place the transistors close to the tip. The contact plate was 500 µm thick, 5 mm wide and 10 mm long. Its edge was displaced with respect to the needle in order to allow a visual control of the impalement.

2.2. Animal preparation

30-40 days old Wistar rats were anesthetized with an induction mixture of Tiletamine and Xylazine (2 mg and 1.4 mg / 100 g weight, respectively). The rat's eye, hind-limbs' reflexes, respiration, and whiskers' spontaneous movements were monitored throughout the experiment to check the level of anesthesia and whenever necessary additional doses of Tiletamine (0.5 mg / 100 g weight) and Xylazine (0.5 g / 100 g weight) were provided.

Rats were positioned on a stereotaxic apparatus and fixed by teeth- and ear-bars. The body temperature was constantly monitored with a rectal probe and maintained at about 37°C using a homeotermic heating pad. Heart beat was monitored by standard ECG. Anterior-posterior opening in the skin was made in the center of the head, starting from the imaginary eye-line and ending at the neck. The connective tissue between skin and skull was removed by a bone scraper. The skull was drilled to open a window in the first somatosensory cortex, S1 (AP –1 to –4, LM +4 to +8) right cortex. In order to reduce brain edema, only a slit at coordinates AP –2.5, LM +6 was made [59].

Throughout the surgical procedure and recording, the brain was bathed through a perfusion system by a standard Krebs solution (composition in mM: NaCl 120, KCl 1.99, $NaHCO_3$ 25.56, KH_2PO_4 136.09, $CaCl_2$ 2, $MgSO_4$ 1.2, glucose 11), constantly oxygenated and warmed to 37°C.

In the ROC configuration, the anesthetized rat was carefully placed "upside-down" on the dry 64

EOSFET based chip or EOMOSFET based chip (equipped with a suitable custom-made plastic chamber) to get a better adhesion of the brain surface to the recording area. A perfusion system was realized with a peristaltic pump, so that the oxygenated and warmed Krebs solution flowed into the chamber. An elastic gel-based and heated "mattress" was put under the rat to maintain body's temperature and to reduce possible artifacts generated by movements. At the end of each experiment, the rat was carefully removed from the setup: the contact area between the cortex and the transistors was clearly visible on both the brain and the chip (Fig. 4 (b)).

While preparing the animal for the impalement, at the end of the surgery the contralateral whiskers were trimmed at about 10 mm from the snout. These whiskers were then stimulated to evoke neuronal activity at the S1.

2.3. Recording cortical surface signals in Rat-On-Chip configuration

Two kinds of stimuli were independently provided during the recording: 1: 1 mM bicuculline (a competitive $GABA_A$ receptor antagonist leading to epileptic-like activity) was incubated 5' on the brain before the positioning of the rat on the chip and then added to the recording bath solution; 2. air puff stimulations of 40 psi with duration of 50 ms were provided to the selective whiskers by means of a microinjection pneumatic picopump (PV80, WPI Inc., USA), in order to evoke a neuronal response of the S1 somatosensory cortex. The recorded signals from the 64 EOSFETs chips were compared to extracellular recordings with 1 MΩ resistance borosilicate micropipettes inserted in S1 cortex for both bicuculline and air-puff stimulation (Fig. 7).

The chips were connected to computers by custom-built amplifiers and the neuronal signals were recorded by custom-made software developed in LabView (http://www.ni.com/labview/). The signals recorded by the EOMOSFET chips were visualized through a pseudo-color plot of the x, y transistors matrix, where positive-to-negative signal amplitudes (mV) were shown by red-to-blue colors. Single transistor traces in the time domain could be selected by moving cross hairs on the matrix (Fig. 8). These chips were detecting neuronal signals as evidenced from the individual frames of the pseudo-color plot taken at 200 µs time lag (Fig. 9).

2.4. Recording cortical signals using implantable needle chips

Neuronal signals were evoked by stimulating single whiskers mechanically with a piezoelectric bender through a connected tube. The bender was driven by a waveform generator (Agilent 33250A 80 MHz, Agilent Tech.) providing square stimuli at 0.5 Hz. Each whisker, starting from the posterior group, was individually inserted into the metal tube and the corresponding response was checked in S1 cortex IV layer (at 640 μm depth). The most responsive whisker, i.e., the "principal whisker" was then chosen for the recording section, and signals were recorded by moving the chip up and down to have a complete depth profile of the cortex. At each recording depth LFPs were recorded by stimulating the whisker at different angles ranging from 0° to 315° at a step of 45° [60].

The chip was connected to the computer by custom-built amplifiers and the neuronal signals were recorded by custom-made signal acquisition software developed in LabView. The acquired signals were compared to the conventional borosilicate micropipettes with 1 MΩ resistance and were found similar (Fig. 10) [61].

3. Analysis of signals acquired by the chips

As mentioned earlier, the signals acquired by the state-of-the-art BCHIs are huge in amount and require tools for automated processing and analysis. We have developed a comprehensive tool, 'SigMate' for processing and analysis of the signals recorded using the BCHIs discussed in the previous section. This tool is more of a framework that incorporates popular open-source standard tools and our in-house tools. The following subsections will provide information about the design and existing features of the SigMate package.

3.1. SigMate design

SigMate is designed using a multi–layered approach with three layers as seen in Fig. 11.

- o   Presentation layer (top layer): This is the topmost level of the application. The presentation layer contains the GUIs of the application. It communicates with the middle layer by requesting the user commands.

- o   Application layer (business logic layer, or middle layer): The logic layer is separated from the

presentation layer and here an application's functionality is controlled by performing detailed processing and analysis.

- o Data layer (bottom layer): This layer consists of databases and/or storages. Here information is stored and retrieved. This layer keeps data neutral and independent from applications or business logic. Giving data its own layer also improves scalability and performance. In case of SigMate, no particular databases are used, rather storage devices are used to store the signals and it is expected to have the recorded signal files in a storage device.

Fig. 12 shows the use case diagram of the SigMate software package with its various features.

3.2. SigMate features

SigMate is a comprehensive package as it contains features dealing with LFPs, spikes, and EEG. Present features include:

- o Signal visualization: to visualize signals in 2D and 3D.

- o File operations: to perform file splitting, file concatenating, and file column rearranging.

- o Stimulus artifact removal: to remove slow artifacts induced by air-puff stimulation in case of cortical signal recording, and fast artifacts induced by intracortical microstimulations.

- o Noise characterization: to assess the quality of the recorded signal and provide the user with noise information of the recorded signals.

- o Spike detection, sorting and spike train analysis: we adopted a popular package "Wave_Clus" from [30].

- o Current source density calculator: calculates current source density (CSD) of the recorded LFPs using standard CSD method, step inverse CSD method, δ–source inverse CSD method, and spline inverse CSD method.

- o Latency estimator: estimates latencies through event and sink detection in LFPs and CSDs, respectively. Also calculates the cortical layer activation order using the calculated latencies, if a

depth profile of LFPs is provided.

o Contour based single LFP classifier: classifies single LFPs based on their shapes to understand the possible signal variations generated by the underlying neuronal networks under same stimulation.

o EEG analysis: we adopted a popular open-source package, "EEGLAB" from [29] for processing EEG.

Fig. 13 shows the initial GUI of the SigMate software package pointing out the various attributes present in the GUI.

4. Conclusion and perspectives

Despite first evidence has been provided that BCHIs can be employed to drive neuroprosthetic devices in humans [5], there is a long way to go before reasonable advantages can be obtained to justify a massive use in clinics of the approach. Potentially, for example, BCHIs offer the possibility of on-chip integration of neuromorphic substitutes of brain circuits. Examples of various model based neuroprosthetic devices were reported [4–5, 62–66]. The reported applications not only included neuroprosthetic devices to restore motor functions, but also devices focusing on afferent processes, i.e., sensory processes [67]. Moreover, the first level of BCHI (interfacing individual neurons and their networks with planar chips) may be used for biological specifications, like – gene functions and DNA/RNA schema. An application example of such BCHI can be found in [68] and a topical review at [69]. In conclusion, BCHIs represent a transdisciplinary approach allowing to investigate brain function with unprecedented resolution and acting as communication link between nervous system and neuroprostheses.

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Figure Captions

Fig. 1

Brain-Chip Interface. Rat neurons in culture on a silicon-oxide insulated array of field effect transistors (EOSFETs). EOSFETs detect extracellular potentials generated by ionic currents flowing through the neuronal membrane during electrical signaling, thus monitoring neuronal excitation [6].

Fig. 2

Schematic description of extracellular nerve cell interfacing approaches. a. Noble metal electrode based interfacing, b. EOSFET based interfacing.

Fig. 3

(a) A first generation chip used for "rat-on-chip" recordings, with the plastic chamber; the FETs' arrays are located in the center of the chip. (b) Magnification of the chip showing alternated EOSCs and EOSFETs arranged in two rows. Scale bar 100 µm [11].

Fig. 4

(a) A second generation chip used for a high-resolution cortical recording, with the plastic chamber. (b) Magnification of the chip showing the recording area containing the 128×128 EOMOSFET matrix after removal of the rat [11].

Fig. 5

(a) Scanning electron microscope picture of a needle chip prototype with 4 EOSFETs shown in different colors [58]. (b) Experimental setup for the needle chip. Magnification of the rat head: the opening in the skull in correspondence to the S1 cortex and the chip inserted into the cortical area are visible. The chip was carefully inserted through a small slit in the meninges. A selected whisker was inserted into a tube mounted on the piezoelectric bender for stimulation. (c) Setup for multiple implants where one chip is positioned in the S1 cortex and the second one in the M1 cortex. Sample of recordings using the needle chip is shown in Fig. 10.

Fig. 6

Placement of the rat on the chip during ROC experiment. (a) With the 64 EOSFETs chip. (b) With the 128 × 128 EOMOSFET chip.

Fig. 7

(a) Superimposition of two LFPs from S1 cortex upon chemical stimulation, one recorded by a glass pipette inserted in the first cortical layers (black) and one by a transistor (grey). (b) Superimposition of two LFPs from S1 cortex upon air puff stimulation. Color codes for pipette and transistor as on the left. The stimulus is shown at the bottom [the y-axis scale doesn't apply to the stimulus].

Fig. 8

High-resolution recording from the rat brain somatosensory cortex at 8 µm pitch. (a) Bidimensional plot of potentials measured by a 128 × 128 EOMOSFET array based chip after bicuculline stimulation. Each pixel (defined by x, y coordinates) represents a transistor record at a spatial resolution of 7.8 µm. (b) Single transistor traces corresponding to red and green cursors on the left. Time scale is in s, amplitude in mV.

Fig. 9

Electrical imaging of S1 brain cortex at 7.8 µm resolution in the living rat. These frames captured at 200 µs time lag show the propagation of LFPs across the cortical surface.

Fig. 10

Comparison of averaged (n = 50) evoked LFPs recorded in the rat S1 cortex by means of a micropipette (a) and transistor (b) at 0°. Recording depths in µm are shown at the right of each trace.

Fig. 11

Three–layered architecture of the SigMate software package.

Fig. 12

Use case diagram of the SigMate software package. The Scientist represents a generic user who directly interacts with the various features of the package. The user interacts with the GUIs of the features and the modules constituting the feature are encapsulated in the middle layer. In the use case diagram the directed line(s) represent(s) major modules of a feature.

Fig. 13

Initial GUI of the SigMate package. This GUI contains the menu bar that bundle the various features of the package together. There are some common attributes which are available in all the features' GUIs: 1) a dropdown box for selection of signal source, 2) a number of check boxes for channel selection, 3) a listbox to show the selected files, 4) a browse button to let the program select a folder whose contents can be seen in the listbox, 5) a display pane (with zoom, pan and data cursor add-ins) to visualize the selected signal file(s) from the listbox, 6) a remove file button to remove selective files from the listbox, 7) a pair of move up and move down buttons to set the order of the selected signal files, 8) a load data button to load the signal files present in the listbox for easy access, and 9) module specific buttons and fields.
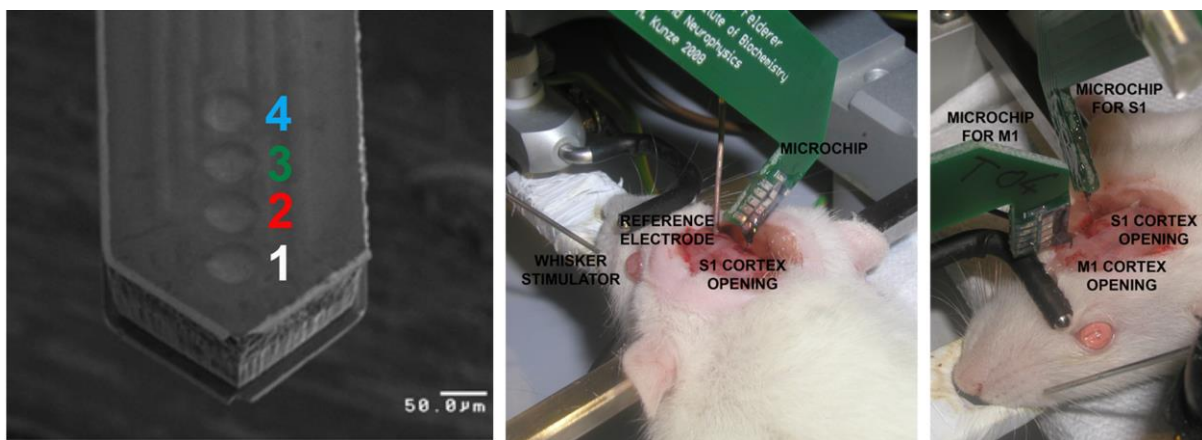
Figures:

Figure 1:
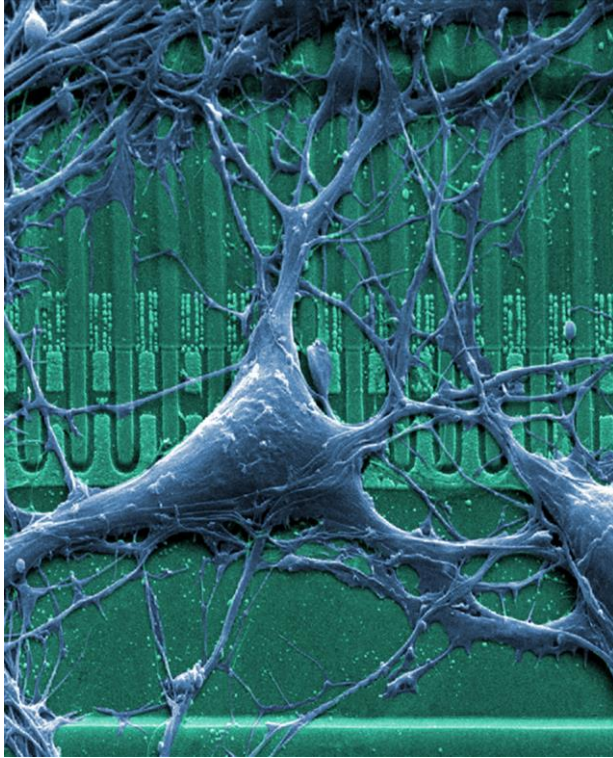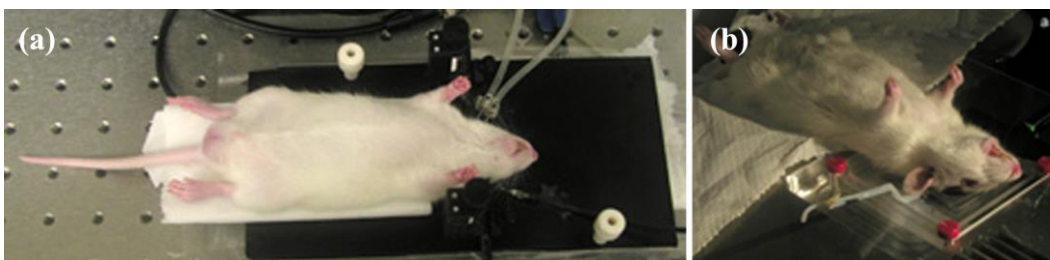

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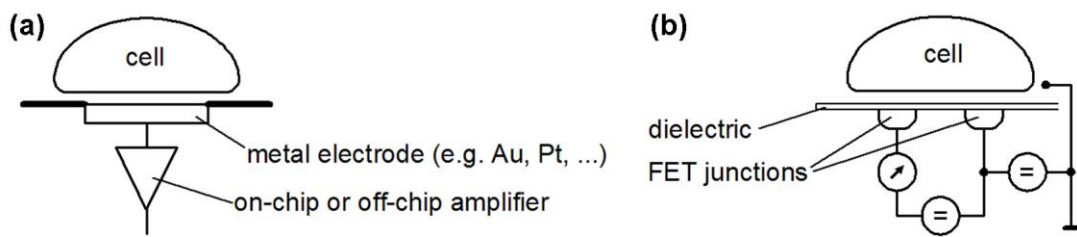
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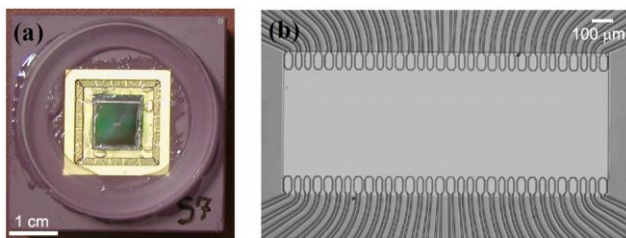
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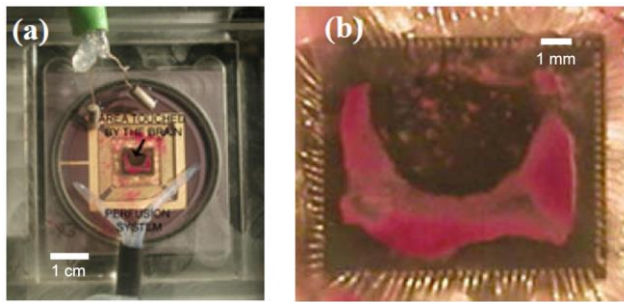
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Figure 6:

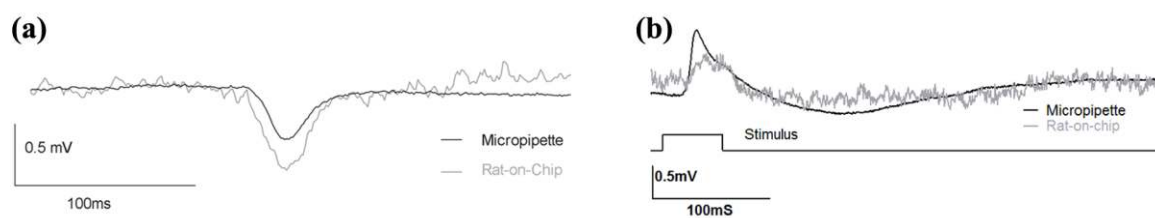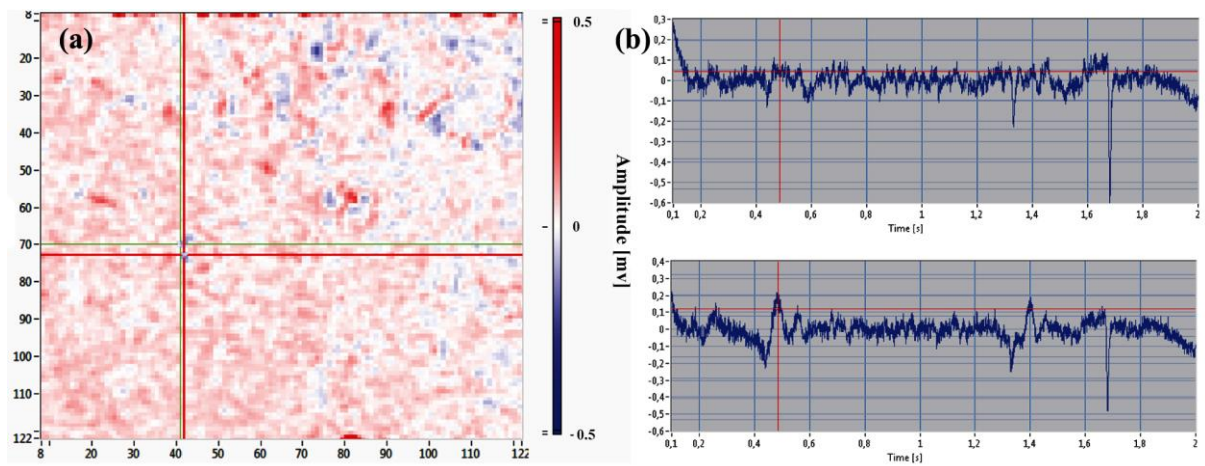Figure 7:

Figure 8:

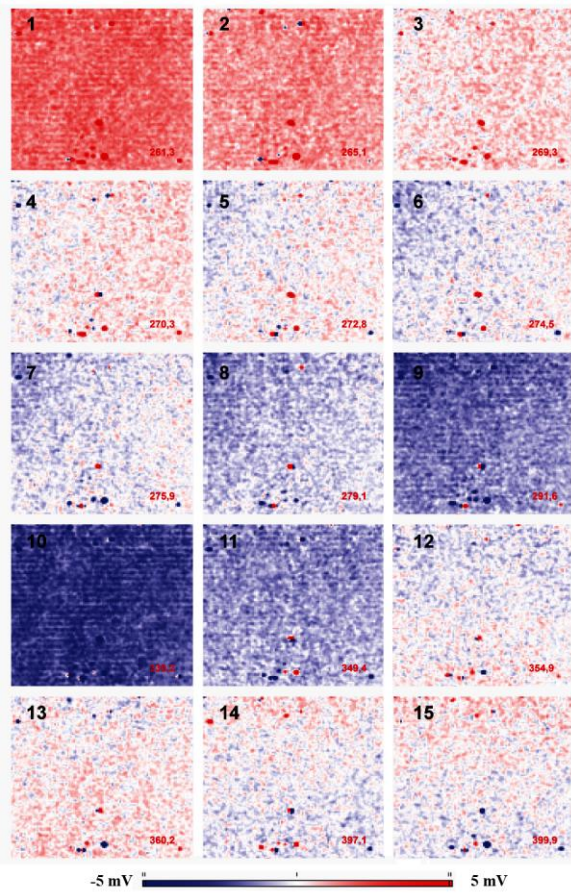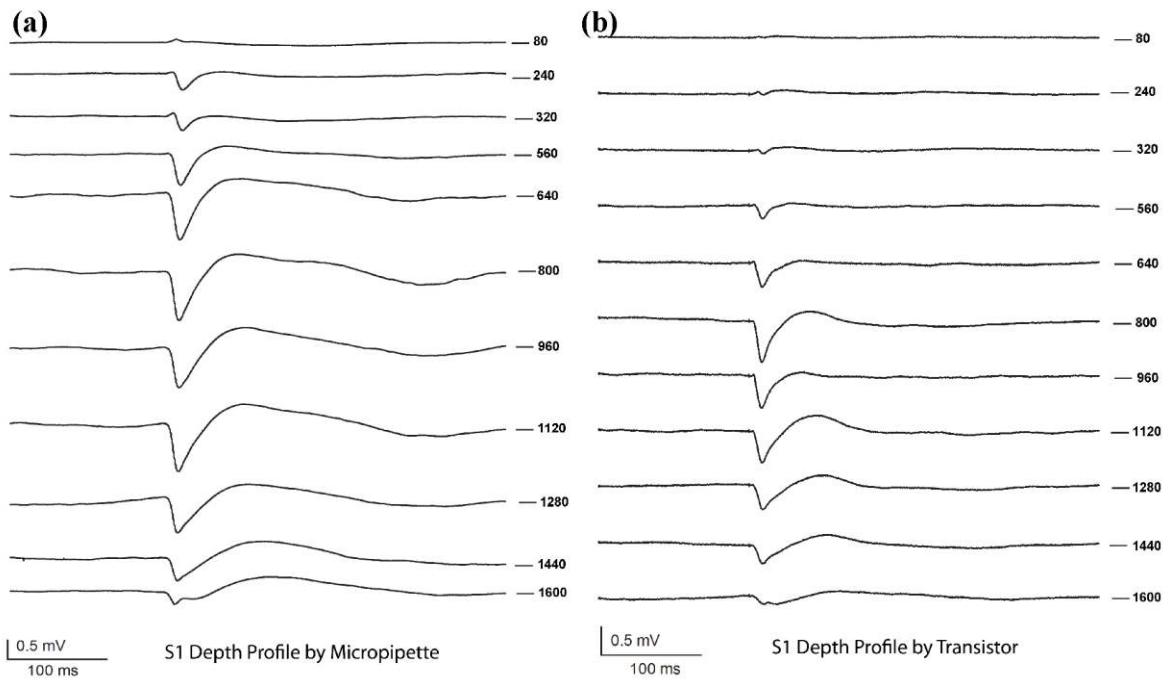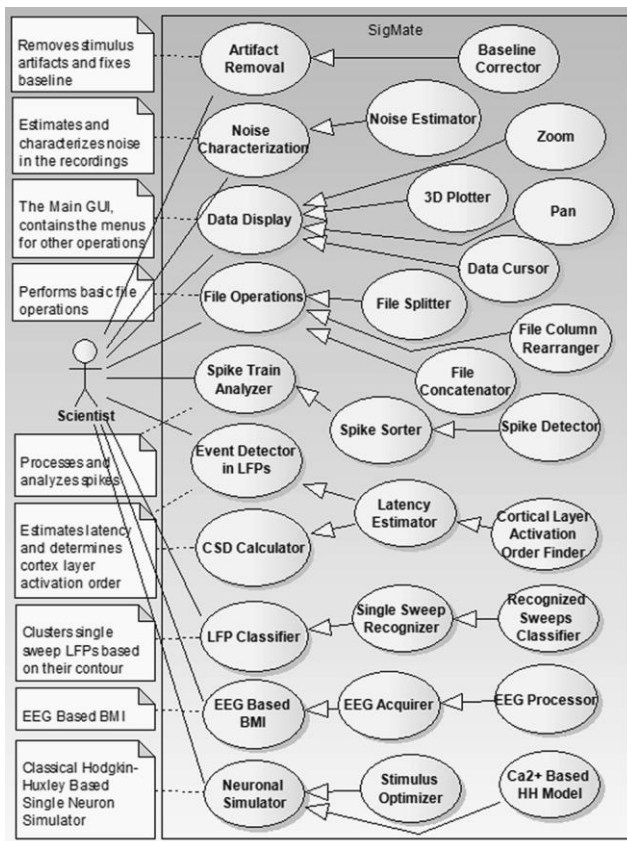Figure 9:

Figure 10:

S1 Depth Profile by Micropipette

S1 Depth Profile by Transistor

Figure 11:

Figure 12:

Figure 1: