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One Leg Control Strategy in Single-Phase Five-Level Inverter

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General Chair

One Leg Control Strategy in Single-Phase Five-Level Inverter

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***Abstract*—The use of power inverter technology with low harmonics content is rapidly growing. For decades, researchers have conducted investigations to minimize its harmonics content, leading to the creation of a five-level inverter. This new topology often deals with many power semiconductor switches, thereby making it difficult to control. Therefore, this paper studies a further simulation and hardware implementation of the one leg control strategy of the single-phase five-level inverter design with efficient control of switches operated in a line frequency to achieve a higher-level demand. The verification of this research is a simulation and prototype implementation carried out in the laboratory**

Keywords—One leg, Single-phase, Five-level inverter

I. INTRODUCTION

Renewable energy is a new trend in the electricity industry. This system (photovoltaic and wind) consist of an energy conversion device, and Maximum Power Point Tracker (MPPT) used to maximize power output in an inverter. The newly designed inverter contains low harmonic content, with the most common being the H-bridge. Furthermore, to obtain a small harmonic production of voltage or current, it must be operated at high frequencies using large filters. Due to these limitations, multi-level inverters are widely implemented

This type of inverter is similar to the conventional with the same functionalities. However, it has better voltage and current harmonic output, although they are less efficient. The basic multi-level inverter consists of three groups, namely: neutral diode-clamped [1-3], multi-cells (flying capacitor) [4], and separated DC sources (cascade H-bridge) [5]. To form a five-level, the common multi-level inverters require many power semiconductor switches. Here are examples of some five-level topology: Eight-six active switches [6-8], six active switches [9] and two passive switches [10-11], as well as five active switches and four passive switches [12, 13]. Judging from the number of switches (passive and active), this system will be more complicated with complex control circuits. Many types of five-level inverters have the same voltage and current output harmonics at the same level, but the complexities of control could be reduced. Other advantages also include the ability to suppress switching losses on the power semiconductor component and semiconductor switch device. A higher inverter level will result in a smaller output voltage and current harmonics. Although the value of the filter size decreases, this method is not efficient. Inverters with a low total harmonic distortion (THD) are in great demand because it produces high THD, thereby, leading to interference with the distribution network, such as in the case of grid tie inverters [14-17].

In this paper, a five-level inverter using five active and one passive power switch had been analyzed to develop a new one leg control strategy capable of producing higher switching frequency. This control strategy is able to achieve low switching loss than every active power switch. The five-level inverter control design is validated using computational simulation, and at the final stage, hardware implementation is carried out. Testing is conducted by comparing the simulation and implementation results obtained from the laboratory test.

II. FIVE-LEVEL INVERTER TOPOLOGY

In this section, a five-level inverter topology that have been design is discussed. It is divided into two parts: the first part comprises of S1 - S4 as the three-level inverter (unipolar H-Bride inverter) and the second part is the next level comprises of S5. The five-level inverter power circuit is shown in Figure 1.

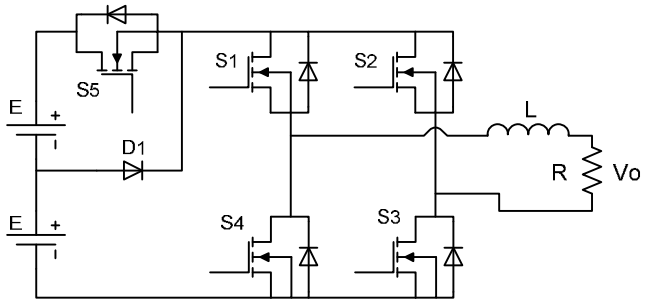

Fig. 1. Five-level power circuit

It is described as possible operating modes:

A. *The operation mode 1*

When the power switches: S5 and S1 are conducted, the current from the voltage source (E + E) flows to the load and returns to the voltage source (E + E) through the S3 power switch. The illustration of the operation mode is shown in Figure 2. This condition is represented in question (1):

$$E - E = v_L + V_o$$

$$2E = L\frac{di_L}{dt} + V_o$$

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$$L\frac{di_L}{dt} = 2E - V_o$$

$$L\Delta i_L = (2E - V_o)\Delta t = (2E - V_o)t_{on} \quad (1)$$

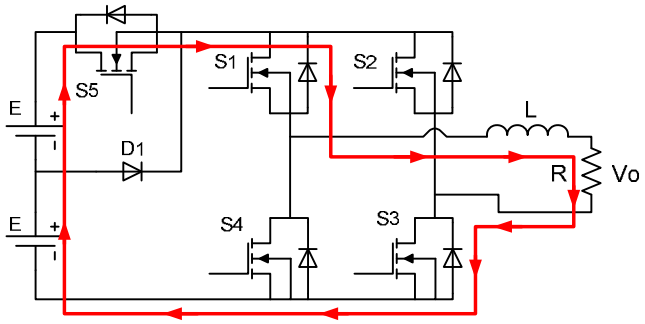

Fig. 2. The operaton mode 1

B. The operation mode 2

When the power switches: D1 and S1 are conducted, the current from the voltage source (E) flows to the load and returns to the voltage source (E) through the S3 power switch. The illustration of the first operation is shown in Figure 3. This condition is represented in question (2):

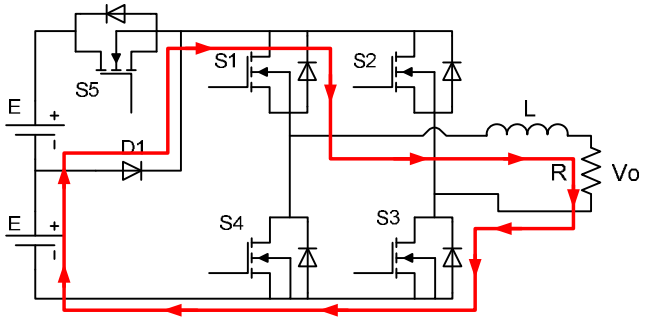

Fig. 3. The operaton mode 2

$$E = v_L + V_o$$

$$E = L\frac{di_L}{dt} + V_o$$

$$L\frac{di_L}{dt} = E - V_o$$

$$L\Delta i_L = (E - V_o)\Delta t = (E - V_o)t_{on} \quad (2)$$

C. The operation mode 3

When the power switches: S1 and S2 are conducted, the current flows in a freewheeling condition of the load for a positive value. While the combination of switches S3 and S4 result in a freewheeling condition for a negative value. The illustration of the operation mode is shown in Figure 4. This condition is represented in question (3):

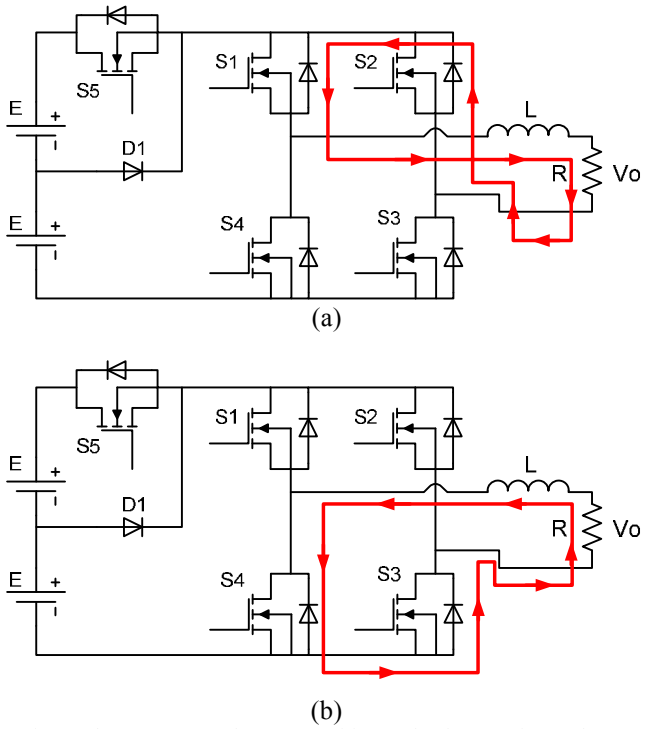

Fig. 4. The operaton mode 3. (a). Positive cycle, (b) Negative cycle

$$v_L = V_o - v_d$$

$$L\frac{di_L}{dt} = V_o - 0$$

$$L\Delta i_L = V_o\Delta t = V_o t_{off} \quad (3)$$

D. The operation mode 4

When the power switches: D1 and S2 are conducted, the current from the voltage source (E) flows to the load and returns to the voltage source (E) through the S4 power switch. The illustration of the first operation is shown in Figure 5. This condition is represented in question (4):

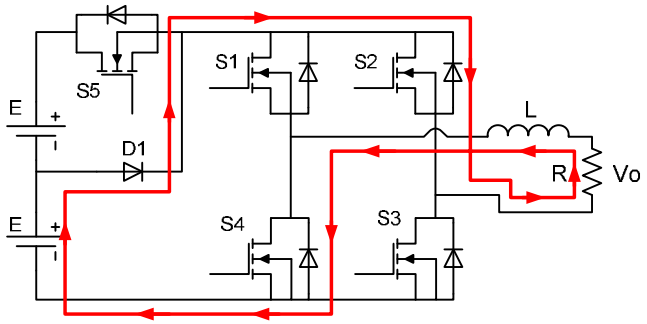

Fig. 5. The operaton mode 4

$$-E = v_L + V_o$$

$$-E = L\frac{di_L}{dt} + V_o$$

$$L\frac{di_L}{dt} = V_o - E$$

$$L\Delta i_L = (V_o - E)\Delta t = (V_o - E)t_{on} \quad (4)$$

E. The operation mode 5

When the power switches: S5 and S2 are conducted, the current from the voltage source (E+E) flows to the load and returns to the voltage source (E+E) through the S4 power switch. The illustration of the first operation is shown in Fig 6. This condition is represented in question (4):

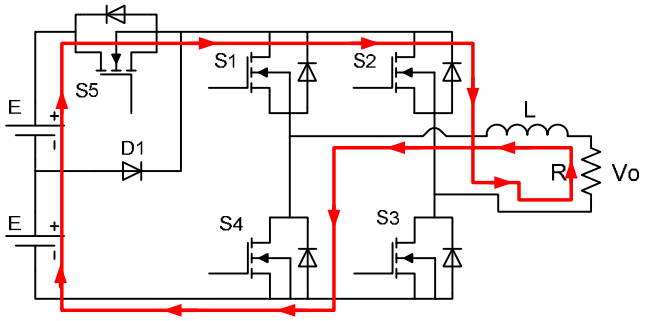

Fig. 6. The operaton mode 5

$$-(E-E)=v_L+V_o$$
$$-2E=L\frac{di_L}{dt}+V_o$$
$$L\frac{di_L}{dt}=V_o-2E$$
$$L\Delta i_L=(V_o-2E)\Delta t=(V_o-2E)t_{on} \quad (5)$$

The relation between question (1) – (5) could be expressed in matrix function is represented in question (6):

$$V_o=M\,2E \quad (6)$$

M: index modulation that consisting of m_1 ($0\le m_1\le\frac{1}{2}$) and m_2 ($\frac{1}{2}\le m_2\le 1$).

III. ONE LEG CONTROL STRATEGY

Based on the operation modes (1 - 6), the active power switches (S5, S1 and S4) operate at high frequency, while others operate in a 50 Hz frequency to produce a half positive cycle and negative cycle. The gate switching logic for operation modes are represented in Table 1.

TABLE I. FIVE-LEVEL INVERTER OUTPUT

Polarity Generator		Level generator			Vo
S2	S3	S1	S4	S5	
Off	On	On	Off	On	2E
Off	On	On	Off	Off	E
On	Off	On	Off	Off	0
Off	On	Off	On	Off	0
On	Off	Off	On	Off	-E
On	Off	Off	On	On	-2E

The constructing of the unique sinusoidal pulse width modulation (SPWM) of the five-level inverter is carried out by applying Table 1 to design the proposed new system using one leg control strategy. The expression for the level generator logic decoding sequence and polarity generator could be seen for each power switch. This proposes a new SPWM control circuit for the five-level inverter, as shown in Fig 7. The proposed SPWM gating signal used to construct a five-level inverter output is shown in Fig. 8.

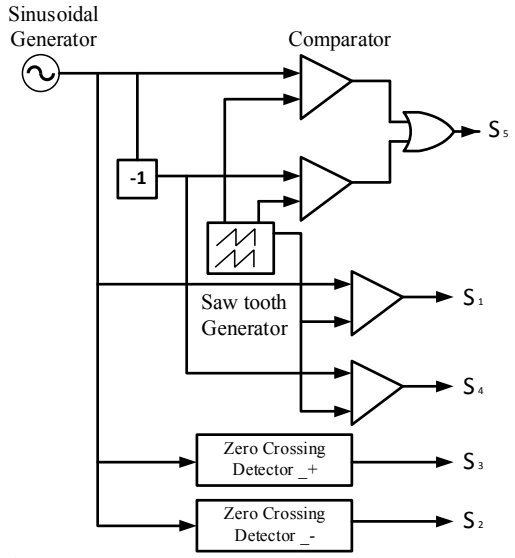

Fig. 7. The proposes a new SPWM control

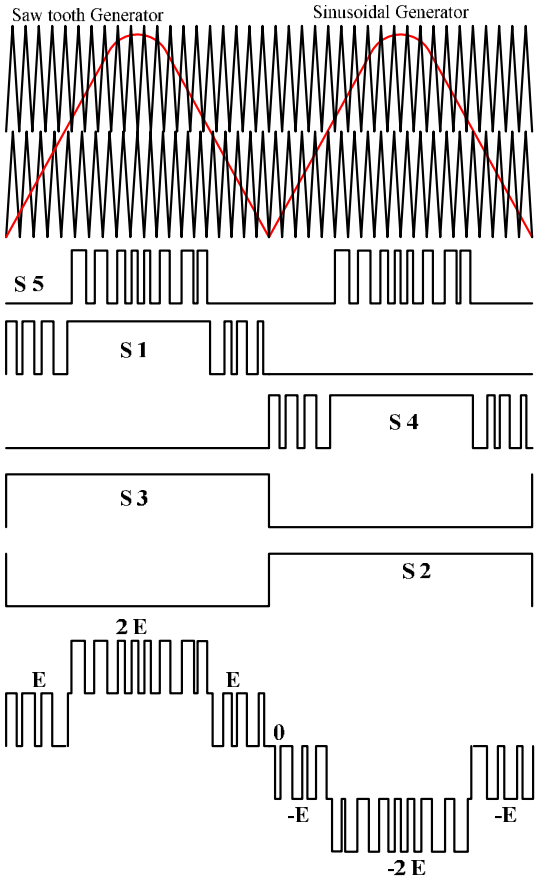

Fig. 8. The proposed SPWM gating signal to constructing five-level inverter output

IV. Results and Analisys

The verification used to validate the analysis is conducted by simulation of the proposed five-level inverter design using a new SPWM control strategy. These proses are simulated through PSIM software, with the parameters represented in Table 2.

TABLE II. Simulation and Implementation Parameters

Parameters	Value
Voltage input	200 Volt
Inductor	2 mH
Load	100 Ohm
Frequency Switching	10 KHz

The SPWM gating signal for the five levels is constructed on switches S5, S1, and S4 as represented in Fig 9. The gating signals for polarity generator are constructed on switches S2 and S3, as shown in Fig 10.

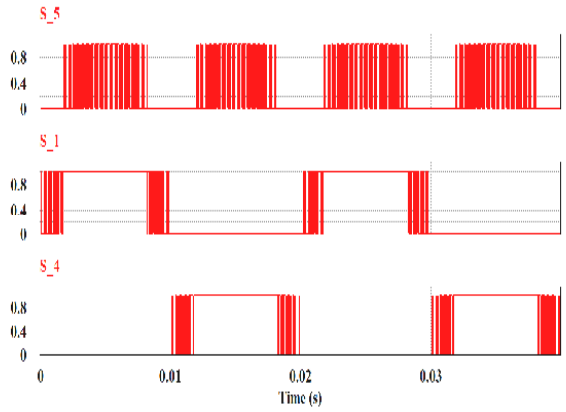

Fig. 9. The gating signal S5, S1 and S4

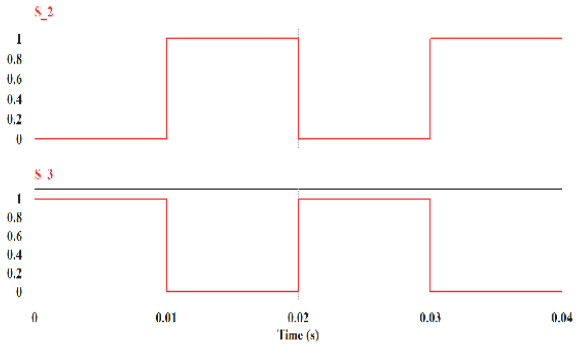

Fig. 10. The gating signal S2 and S3

The final tests of the simulation results in the construction of the five-level output waveform are seen in Fig 11. The magnitude voltage levels were at +200V, +100V, 0, −100V and −200V. The five-level output waveform is filtered through an inductive filter of 2mH which is seen in Fig 11.

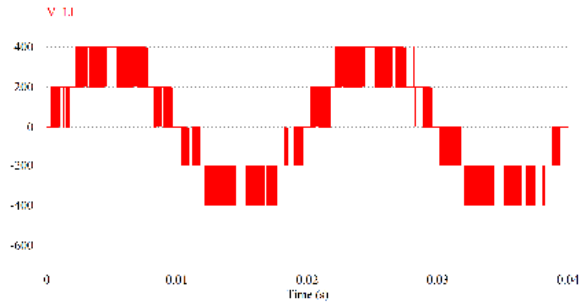

Fig. 10. Five-level inverter output waveform

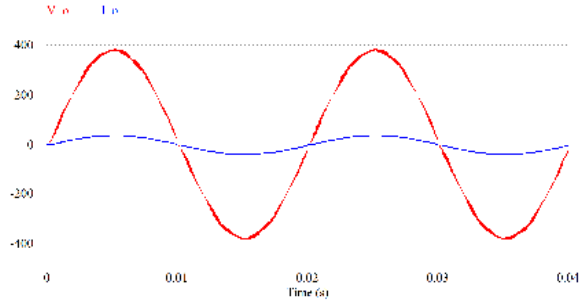

Fig. 11. The current (blue) and voltage (red) inverter output waveform

The core of one leg control strategy implements a micro-controller PIC 40F4550. The IGBT SKM75GB123D is used as active and passive power switches of five-level inverter. Furthermore, the TLP 250 is used as an electric isolator for active switch S5, while the TLP 250 and IR2110 are used as an electrical isolator for S1-S4. Fig 12 shown the gating signal for S5 (red), S1 (blue), and S4 (yellow). The gating signals for reduce switching loss are constructed on switches S2 (yellow) and S3 (blue), as shown in Fig 13.

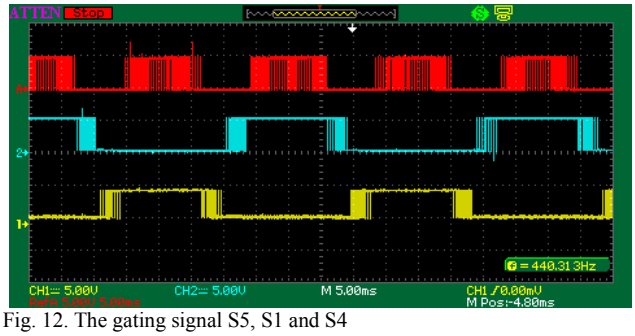

Fig. 12. The gating signal S5, S1 and S4

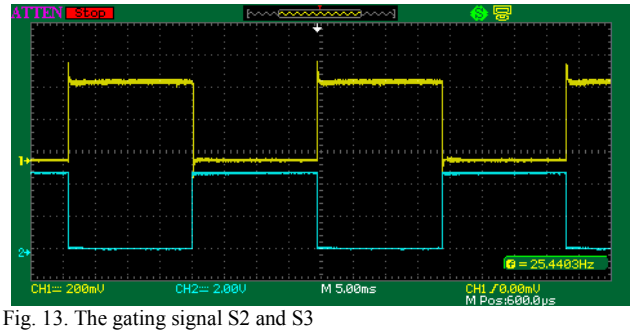

Fig. 13. The gating signal S2 and S3

The experimental results of five-level inverter output are depicted in Fig 14. Finally, the current and voltage inverter output is presented in Fig. 15.

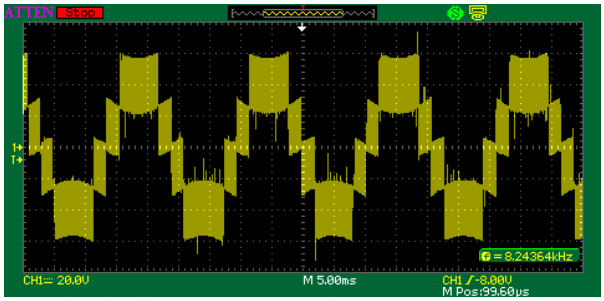

Fig. 14. Five-level inverter output waveform

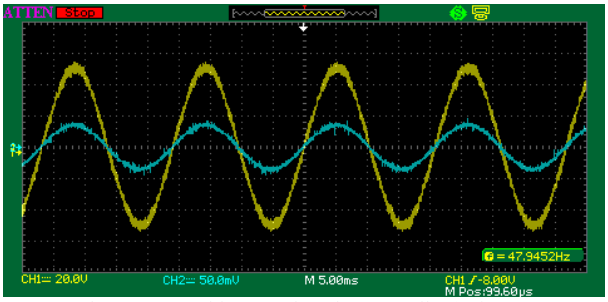

Fig. 15. The current (blue) and voltage (yellow) inverter output waveform

This verification of the simulation shown that the one leg control strategy for five-level inverter is straightforward to utilize using the level values and zero-crossing polarity detector.

V. Conclusion

The one leg control strategy for single-phase five-level inverter presented in this paper consists of three levels with high frequency switching on positive value and polarity generator with low frequency switching respectively. By utilizing this method, the switching losses are likely to be adequately reduced.

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References

[1] A. Nabae, I. Takahashi, and H. Akagi, “A new neutral-point-clamped PWM inverter,” IEEE Trans. Ind. Appl., vol. IA-17, no. 5, pp. 518–523, Sep. 1981

[2] L. Lin;Y. Zou; Z. Wang and H. Jin, “A simple neutral-point voltage balancing control method for three-level NPC PWM VSI inverters,” in Proc. IEEE Int. Conf. Electr. Mach. Drives, pp. 828–833, May 15, 2005

[3] S. Guanchu, K. Lee, L. Xinchun, and L. Chongbo, “New neutral point balancing strategy for five-level diode clamped converters used in STATCOM of wind energy conversion systems,” in Proc. IEEE 6th Int. Power Electron. Motion Control Conf, pp. 2354–2358, pp. 2354–2358 May 17–20, 2009

[4] T. A. Meynard and H. Foch, “Multi-level conversion: High voltage choppers and voltage-source inverters,” in Proc. IEEE 23rd Annu. Power Electron. Spec. Conf., vol. 1, pp. 397–403, Jun. 29–Jul, 1992

[5] M. Marchesoni, M. Mazzucchelli, and S. Tenconi, “A non-conventional power converter for plasma stabilization,” in Proc. IEEE 19th Annu. Power Electron. Spec. Conf. (PESC’88) Rec, , vol. 1, pp. 122–129, April 1988.

[6] P. Roshankumar, P. P. Rajeevan, K. Mathew, K. Gopakumar, Jose I. Leon, and Leopoldo G. Franquelo, “A Five-Level Inverter Topology with Single-DC Supply by Cascading a Flying Capacitor Inverter and an H-Bridge,” IEEE Trans on Power Electronics, vol. 27, pp. 3505-3512, August 2012.

[7] Shalchi Alishah, R.; Nazarpour, D.; Hosseini, S.H.; Sabahi, M., "Switched-diode structure for multilevel converter with reduced number of power electronic devices," Power Electronics, IET , vol.7, no.3, pp.648,656, March 2014.

[8] Krishna Kumar Gupta, Shailendra Jain,” Comprehensive review of a recently proposed multilevel inverter”, IET Power Electron., 2014, Vol. 7, Iss. 3, pp. 467–479, 2014.

[9] Ebrahim Babaei, Mohammad Farhadi Kangarlu, Farshid Najaty Mazgar,”Symmetric and asymmetric multilevel inverter topologies with reduced switching devices”, Electric Power Systems Research Vol. 86, pp.122-130, May 2012.

[10] J. M. Shen, L. H. Jou, C. J. Wu, and D. K. Wu, “Five-Level Inverter for Renewable Power Generation System”, *IEEE Transactions on Energy Convertion* , Vol 28, pp. 257-266, June 2013.

[11] L. H. Pratomo, F. D. Wijaya, and E. Firmansyah, “A Simple Strategy of Controlling a Balanced Voltage Capacitor in Single Phase Five-Level Inverter”, *International Journal of Power Electronics and Drive System,* Vol 6, pp. 160-167, March 2015.

[12] G. Ceglia, V. Grau, V. Guzmán, C. Sánchez, F. Ibáñez, J. Walter, A. Millán, M. I. Giménez, “A New Multilevel Inverter Topology,” Proceedings of the Fifth IEEE International Caracas Conference on Devices Circuits and Systems, Dominican Republic, vol. 1,pp. 212-218, May 2004.

[13] Harrish Pappu, G. SasiKumar and Shiva Teja Manala, “An FPGA based new single phase five level inverter”, *International Conference on Energy, Communication, Data Analytics and Soft Computing (ICECDS)*, 2017.

[14] Samir Kouro ; Jose I. Leon ; Dimitri Vinnikov ; Leopoldo G. Franquelo, “Grid-Connected Photovoltaic Systems: An Overview of Recent Research and Emerging PV Converter Technology,” IEEE Industrial Electronics Magazine ,Vol: 9 , Issue: 1 pp. 47 - 61, March 2015

[15] M. Prodanović, T. C. Green, "Control and filter design of three-phase inverters for high power quality grid connection", *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp. 373-380, January 2003.

[16] T. C. Wang, Z. Ye, G. Sinha, X. Yuan, "Output Filter Design for A Grid-Interconnected Three-Phase Inverter", *IEEE 34th Annual Power Electronics Specialist Conference (PESC'03)*, pp. 779-784, June 15–19, 2003.

[17] L. H. Pratomo, F. D. Wijaya, and E. Firmansyah, “Impedance matching method in two-stage converters for single phase PV-grid system”, International Journal of Electrical and Computer Engineering Vol. 5 no. 4, pp :626-635, Agust 2015