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Online Condition Monitoring System for DC-Link Capacitor in Industrial Power Converters

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***Abstract*—This paper proposes an online condition monitoring system for aluminum electrolytic capacitors used as dc-link capacitors in industrial power converters. Electrolytic capacitors are one of the most fragile components of a power converter system because of their wear-out failures and short lifespan. Therefore, the use of condition monitoring systems for aluminum electrolytic capacitors allow preventive maintenance to be performed, thereby avoiding unexpected shutdown and downtime. The dominant wear-out mechanisms in aluminum electrolytic capacitors are characterized by the increase in equivalent series resistance. Hence, the condition monitoring system proposed in this paper is based on the online estimation of the capacitor's equivalent series resistance using the switching frequency components of the dc-link capacitor voltage and current. The equivalent series resistance estimation method is tested using the PSpice circuit simulator and is validated experimentally using a custom-made inverter. Finally, the equivalent series resistance estimation method is adapted for the condition monitoring of capacitors in industrial power converters and the proposed condition monitoring system is implemented in a commercial ac drive system to prove the applicability of the proposed method to industrial power converters.**

***Index Terms*—Bandpass filters (BPFs), condition monitoring, electrolytic capacitors, parameter estimation, pulsewidth modulated inverters.**

I. Introduction

POWER converters are an integral part of many industries because of their undisputed performance in applications, such as motor drives, uninterruptible power supplies, and electrical heating. With the increase in the quest for more energy efficien systems, power converters are an important area for research in applications, such as renewable energy, hybrid vehicles, and many other safety-critical applications. This has already resulted in another subarea of research, which focuses on the condition monitoring of power converters to mitigate the issues of availability, maintenance cost, and safety in emerging applications. An electric drive system is one of the important areas where power converters are used extensively. Unfortunately, power converters are the most failure-prone component of an electric drive system. The major components of a power converter are power devices, printed circuit boards (PCBs), capacitors, and inductors. Therefore, a condition monitoring system for industrial power converters is proposed based on the work in [1].

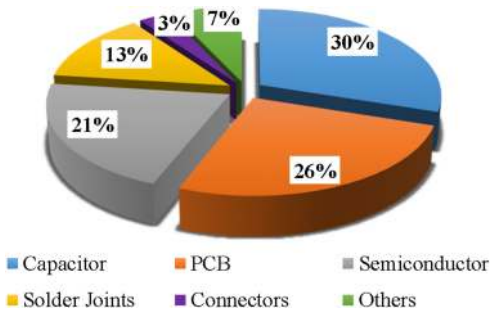

Fig. 1. Failure root-cause summary of power electronic systems.

Capacitors are one of the crucial components in power converters, playing significan roles, such as filters snubbers, and energy-storage elements. Aluminum electrolytic capacitor (AEC) and fil capacitor are the most popular capacitor types used in power converters. AECs provide a higher capacitance, higher volumetric efficien y, and better price over performance ratio than fil capacitors. However, AECs are perceived to be less reliable than fil capacitors because of the incidence of explosion and ignition that can accompany AEC failures in large high-voltage banks of ten or more capacitors [2]. Nevertheless, AECs are used in applications where high capacitance and low cost are preferred. Irrespective of the type, capacitors are one of the most fragile components of a power converter system due to the high failure rates compared to the other components [3]–[5]. The failure root cause distribution for power electronic systems discussed in [6] says that the capacitor contributes to around 30% of the total failures. Fig. 1 shows the pie chart for failure root cause distribution [6]. With the increase in the use of power

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converters in critical applications, condition monitoring of capacitors has become inevitable. In this paper, the focus is on the condition monitoring of electrolytic capacitors. The equivalent circuit of an AEC is explained in [7]. The equivalent circuit of a practical capacitor has all its loss components modeled as an equivalent series resistance (ESR).

In a well-designed system, the capacitor failures are mainly caused by the gradual deterioration of capacitor properties leading to wear-out failures. The dominant wear-out failure mechanisms in AECs are electrolyte evaporation and oxide-layer deterioration due to electrochemical reactions [8]. All the dominant failure mechanisms lead to an increase in the ESR and a decrease in capacitance. The increase in the ESR above 200% of its initial value and the decrease in capacitance below 80% of its initial value are generally considered as a failure [2], [4], [8]. However, these criteria may vary with different manufacturing processes and are usually specifie in the manufacturer datasheets or application notes [2], [9].

The most common methods to monitor electrolytic capacitors involve the estimation of parameters, such as capacitance and ESR. Several methods have been proposed in the literature regarding the estimation of ESR and capacitance, which can be categorized into online and offlin methods. In offlin methods, the system operation must be interrupted to disconnect the capacitor to measure the required parameters [10], [11]. Therefore, these methods cannot be applied to industrial power converters where the interruption of system operation and disconnection of the capacitor are not favored. If the health indicator can be obtained without interrupting the normal operation of the system, it is called online method. In [12], a method to identify capacitor degradation in dc–dc converters based on the ESR estimation has been proposed. In this method, the ESR is estimated using the output voltage ripple and the output current. This method requires a high-bandwidth sensor to calculate the output voltage ripple accurately. An adaptive filte modeling-based online parameter estimation method that takes input current as its input and estimates the ripple voltage to monitor the capacitor's health is proposed in [13]. The online method to estimate the ESR by calculating power loss and root-mean-square (rms) value of the capacitor current is proposed in [14].

In [15], a cost-effective solution to estimate the degradation-sensitive parameters, namely the ESR and the capacitance using bandpass filter (BPFs), is proposed. This method relies on the fact that the capacitive reactance dominates the impedance of a capacitor in the low-frequency region ($f < 300$ Hz) and the ESR dominates the impedance in the midfrequency region (few tens of kilohertz). Therefore, the low-frequency and switching frequency components of capacitor voltage and current are extracted using BPFs to calculate the capacitive reactance and the ESR using the rms value of BPF outputs. The main drawback is that the accuracy of this method depends on the frequency of the voltage and the current components that are used to calculate the parameters. In [16], a parameter estimation method for variable speed drives is proposed. This method estimates the ESR and the capacitance using the voltage and current data from the inverter whenever the motor is stopped. In [17], the ESR estimation method for monitoring of capacitor in a high-power electric vehicle drive system based on the capacitor's power loss and the ESR model is proposed. In [18], digital fil ters are used to estimate the ESR by using the capacitor voltage and current components. An output voltage transient analysis based condition monitoring approach for the capacitors is proposed in [19]. In [20], a new condition monitoring approach based on low-frequency impedance calculation is proposed. This method estimates the impedance at 120 Hz by modulating the switching signal to introduce a 120 Hz component in the capacitor voltage and current. Since the hotspot temperature of the capacitor is one of the important factors in deciding a capacitor's life, a temperature-sensitive electrical parameter based approach to estimate the hotspot temperature using capacitance measurement is proposed in [21].

In [22], an extensive review of condition monitoring solutions is presented. The advantages and disadvantages of various methods are compared, and the research gaps are identified Several condition monitoring methods have been proposed in the literature. However, those methods either lack accuracy or they are complex to implement in an industrial power converter. Therefore, an online condition monitoring system is proposed in this paper based on the ESR estimation method [1], which is cost effective and is easy to implement in industrial power converters.

II. Equivalent Circuit of an AEC

A capacitor consists of two parallel conducting surfaces separated by a dielectric medium. The capacitance of a capacitor is generally expressed as follows:

$$C = \frac{\varepsilon A}{d} \tag{1}$$

where "A" represents the area of the conducting surface, "ε" is the dielectric constant of the dielectric medium, and "d" is the distance between the parallel surfaces. Ideally, a capacitor is a reactive element that does not dissipate energy, but a practical capacitor is not purely capacitive because of the real-world constraints, such as nonavailability of perfect dielectric, resistance of the conductor, etc. As there is no perfect dielectric, a practical capacitor suffers from self-leakage, which leads to the loss of some charges. There is also some loss of energy due to the fl w of current through the electrolyte and other metallic parts, which has a nonzero resistance. Hence, a practical capacitor dissipates energy. Also, due to the loop formed by the terminals, tabs, and wound capacitor elements of a capacitor, the capacitor has a small amount of parasitic inductance inherent to the device, which dominates the capacitor's impedance at higher frequencies. Apart from these, the aluminum oxide dielectric, together with the electrolyte, acts like a rectifie with superior forward direction insulation and reverse conduction properties.

Figure 2 shows the equivalent circuit models of an AEC. In Fig. 2(a), "C" represents the nominal capacitance of the capacitor, "R_P" models the resistance of the dielectric, which causes self-leakage, "$D1$" models the polarized nature of an AEC, "R_S" represents the total resistive losses due to the electrolyte, aluminum foils, tabs, and terminals, and equivalent series inductance "(ESL)" represents the inductance associated with the capacitor.

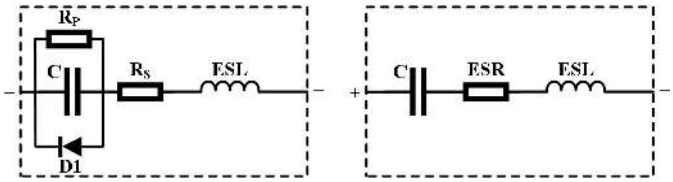

Fig. 2. Equivalent circuit models of an AEC. (a) Complete equivalent circuit. (b) Simplifie equivalent circuit.

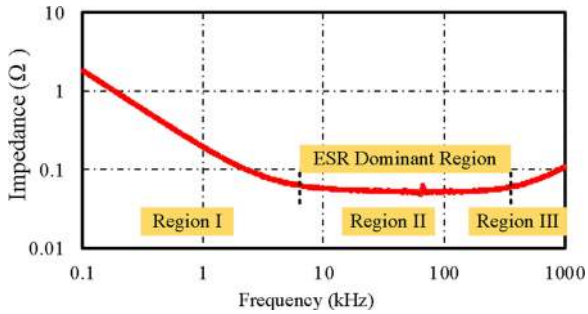

Fig. 3. Impedance characteristics of an AEC.

The equivalent circuit model of Fig. 2(a) can be simplifie by representing all the resistive components in series as the ESR, as shown in Fig. 2(b). The ESR parameter of an AEC has three different components as follows:

$$\mathrm{ESR} = R_O + R_E + R_D\,. \tag{2}$$

Resistance "R_O" represents the total ohmic resistance due to aluminum foil, terminals, and tabs. "R_E" is the resistance of the electrolyte. As the carrier mobility of the electrolyte increases with an increase in the temperature, the electrolyte resistance "R_E" decreases. Hence, the resistance component "R_E" is temperature sensitive with a negative temperature coefficien of resistance. These resistance components "R_O" and "R_E" dissipate some power as heat when current fl ws through them. Apart from these two resistive losses, the capacitor also dissipates heat due to frequency dependent dielectric losses as the aluminum oxide dielectric is subjected to the varying electric field Resistance "R_D" accounts for the dielectric losses in the capacitor. Therefore, the ESR of the capacitor varies with the temperature and frequency due to the presence of temperature-sensitive "R_E" and frequency-sensitive "R_D" components. As the ESR is frequency and temperature dependent, care should be taken to account for frequency and temperature variations during the measurement of the ESR to avoid wrong conclusions.

III. ESR Estimation Method

The ESR estimation method proposed in [1] is based on the frequency response characteristics of the capacitor's impedance. Fig. 3 shows that the impedance versus frequency plot of a capacitor can be divided into three regions. The capacitor's impedance is dominated by the capacitive reactance in region I, the ESR in region II, and the inductive reactance in region III.

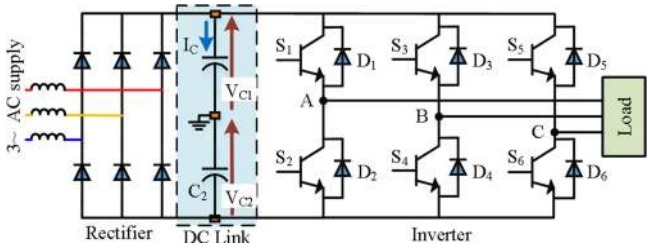

Fig. 4. Circuit diagram of an front-end rectifie -fed three-phase inverter.

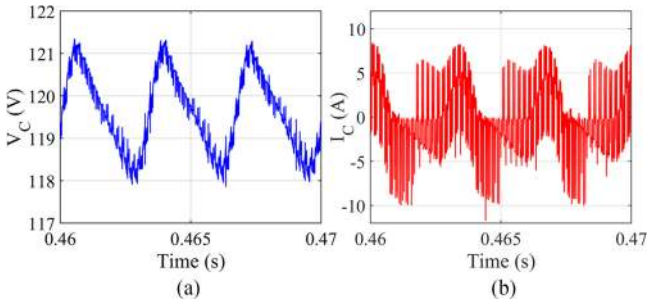

Fig. 5. PSpice simulation results for a dc-link capacitor in the front-end rectifie -fed three-phase inverter. (a) Capacitor voltage. (b) Capacitor current.

Fig. 4 shows the circuit diagram of a front-end rectifie -fed three-phase inverter. In this paper, the ESR estimation method is explained using the PSpice simulation of the front-end rectifie -fed three-phase inverter. Switching pulses are generated using sinusoidal pulsewidth modulation (SPWM) strategy and the switching frequency is 5 kHz. Fig. 5(a) and (b) shows the dc-link voltage waveform and the corresponding capacitor current waveform from the PSpice simulation. Due to the continuous charging and discharging of the dc-link capacitor, there is a small ac content superimposed on the dc content of the capacitor voltage.

The ac content of capacitor voltage is dominated by a 300-Hz component as the capacitor is charged by the three-phase front-end rectifie . The higher frequency components generated by the switching action of the inverter are superimposed on the low-frequency 300-Hz component. As the capacitor voltage changes are due to the capacitor current, the dc-link capacitor current also has ac components of same frequencies. The capacitor voltage and current are analyzed using the fast Fourier transform (FFT) analysis tool in MATLAB, where the fundamental frequency is set as 50 Hz. Fig. 6(a) and (b) shows the FFT plots of dc-link capacitor voltage and capacitor current. The FFT analysis of capacitor voltage and current shows that the dominant higher frequency harmonics are distributed mainly around the switching frequency and its multiples. These harmonic components around the switching frequency and its multiples can be extracted accurately using an analog or digital BPF since the magnitude of other nearby frequency components is negligible. Therefore, these components are used to estimate the ESR in this paper based on the concept explained in the following.

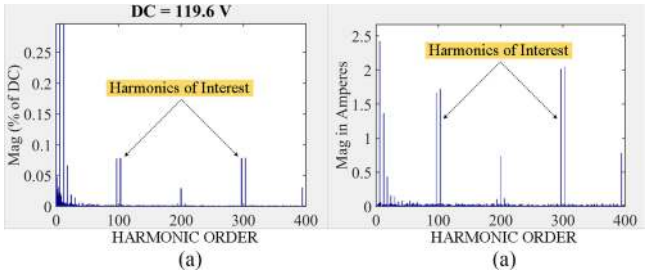

Fig. 6. FFT analysis plots of PSpice simulation results. (a) Capacitor voltage. (b) Capacitor current.

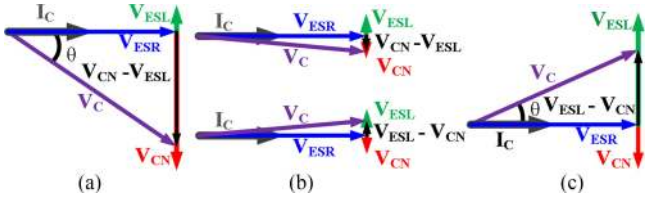

Fig. 7. Phasor diagram of the capacitor voltage. (a) Region I. (b) Region II. (c) Region III.

The sinusoidal component of a capacitor's terminal voltage at frequency "f" is composed of the voltage drops across its various elements of the equivalent circuit. The voltage drops across C, and the ESR and ESL components of the equivalent circuit can be expressed in phasor quantities as $V_{\rm CN}\angle -90^\circ$ or $-jV_{\rm CN}$, $V_{\rm ESR}\angle 0^\circ$ or $V_{\rm ESR}$, and $V_{\rm ESL}\angle 90^\circ$ or $jV_{\rm ESL}$. Fig. 7 shows the phasor diagrams of capacitor's terminal voltage for different frequency regions shown in Fig. 3. The terminal voltage of the capacitor "V_C" is expressed as follows:

$$V_C = V_{\rm ESR} - jV_{\rm CN} + jV_{\rm ESL}. \tag{3}$$

The value of the ESL is very low (20–50 nH) for screw terminal AECs [2]. Therefore, the voltage drop across the ESL is negligible for sinusoidal components with frequencies less than 100 kHz for individual capacitors with capacitance less than few thousands of microfarads. But for capacitors with large capacitances, the effect of the ESL on the impedance is significan for frequencies as low as tenths of kilohertz. In applications, such as marine drives, where the switching frequency is limited to be around 3 kHz, the ESL can be neglected. In case of industrial drives, the maximum switching frequency is generally limited to around 16 kHz [23]–[25]. Therefore, the ESL can be neglected for most cases.

Assuming that the voltage drop across the ESL is negligible for most cases, V_C can be expressed as follows:

$$V_C = V_{\rm ESR} - jV_{\rm CN} \tag{4}$$

$$V_{\rm ESR} = I_C \times {\rm ESR} \tag{5}$$

$$V_{\rm CN} = I_C \times -jX_C \tag{6}$$

$$X_C = \frac{1}{2\pi f C}. \tag{7}$$

As the ESR and capacitive reactance depend on frequency, the switching frequency component ($f = f_{\rm SW}$) of the capacitor's terminal voltage can be expressed as follows:

$$V_{C\_f{\rm SW}} = I_{C\_f{\rm SW}} \times \sqrt{{\rm ESR}_{f{\rm SW}}{}^2 + X_{C\_f{\rm SW}}{}^2} \tag{8}$$

where $f_{\rm SW}$ represents the switching frequency and the subscript "fSW" indicates that these components are measured at the switching frequency. Since the capacitive reactance "X_C" is inversely proportional to the frequency, the capacitive reactance is dominant in the low-frequency region and it decreases with the increase in frequency. Therefore, for higher frequencies, the value of capacitive reactance will be negligible compared to the ESR and it can be neglected. The impedance across capacitor terminals can be assumed almost equal to the ESR for higher frequencies as follows:

$$\sqrt{{\rm ESR}_{f{\rm SW}}{}^2 + X_{C\_f{\rm SW}}{}^2} \cong {\rm ESR}_{f{\rm SW}}. \tag{9}$$

From (8) and (9), for higher frequencies, the ESR can be expressed as follows:

$${\rm ESR}_{f{\rm SW}} = \frac{V_{C\_f{\rm SW}}}{I_{C\_f{\rm SW}}} = \frac{V_{C\_f{\rm SW\_PEAK}}}{I_{C\_f{\rm SW\_PEAK}}} \tag{10}$$

where $V_{C\_f{\rm SW\_PEAK}}$ and $I_{C\_f{\rm SW\_PEAK}}$ are the peak values of switching frequency components of the capacitor voltage and the capacitor current, respectively. If the switching frequency components are extracted using BPFs, the peak value or the rms value of those sinusoidal components can be used to estimate the ESR.

The ESR estimation method proposed in [15] for boost converter uses the rms value of switching frequency components extracted using BPF to estimate the ESR. The ESR estimation method proposed in [15] and similar methods using (10) is based on the condition that the capacitive reactance "X_C" is very small compared to the ESR. If that condition fails, the presence of appreciable capacitive reactance will increase the total impedance and introduce error in the ESR estimation. The method proposed in [15] is suitable for dc–dc converters, since they are usually operated at high switching frequencies. On the other hand, the switching frequency of ac drives varies from few kilohertz to 16 kHz depending on the design and application requirements. Therefore, the method proposed in [15] cannot be used. The theoretical condition to estimate the ESR using (10) with error less than 5% is derived and presented in (11)–(14). The estimation error less than 5% can be achieved using (10), only if the total impedance is not greater than the ESR by 5%.

$$\sqrt{{\rm ESR}^2 + X_C{}^2} < 1.05 \times {\rm ESR} \tag{11}$$

$${\rm ESR}^2 + \left(\frac{1}{2\pi f C}\right)^2 < 1.1025 \times {\rm ESR}^2 \tag{12}$$

$$\frac{1}{fC} < 2.0116 \times {\rm ESR} \tag{13}$$

$$f > \frac{1}{2.0116 \times {\rm ESR} \times C}. \tag{14}$$

Based on the above-mentioned discussion, if the frequency of voltage and current components is greater than the condition specifie by (14), the estimation error will be less than 5%.

Therefore, using (10) or the method proposed in [15] for the ESR estimation requires the following conditions to be satisfied

1) Inductive reactance due to the ESL is negligible at the frequency in which the ESR is estimated.
2) Capacitive reactance is negligible, which can be ensured by using (14).

The use of (14) itself is difficul because it requires the measurement of capacitor parameters at the switching frequency to ensure that the reactance components are negligible. It can be used in cases where the condition monitoring system is planned at the time of designing the power converter because it may lead to a simpler ESR estimation method based on (10). If the switching frequency fails to meet the condition specifie in (14), there are two solutions available to achieve the desired accuracy, which are discussed as follows.

Solution 1: The FFT analysis of capacitor voltage and current in Fig. 6(a) and (b) shows that the harmonics around $3f_{\mathrm{SW}}$ or 15 kHz (harmonic order 300) also have significan magnitude. If the condition specifie in (14) fails for the switching frequency f_{SW}, the voltage and current components around $3f_{\mathrm{SW}}$ can be used to estimate the ESR. The harmonics at $2f_{\mathrm{SW}}$ and $4f_{\mathrm{SW}}$ are avoided here only because of their lesser magnitude. They can be used in cases where they are sufficientl high. The magnitude of harmonics beyond the order 400 is very less and cannot be used. In summary, if condition (14) fails for f_{SW}, the harmonics around $3f_{\mathrm{SW}}$ can be used to estimate $\mathrm{ESR}_{3f\mathrm{SW}}$ using the following equation, provided $f = 3f_{\mathrm{SW}}$ satisfie condition (14)

$$\mathrm{ESR}_{3f\mathrm{sw}} = \frac{V_{C\_3f\mathrm{SW}}}{I_{C\_3f\mathrm{SW}}} = \frac{V_{C\_3f\mathrm{SW\_PEAK}}}{I_{C\_3f\mathrm{SW\_PEAK}}}. \tag{15}$$

Using "Solution 1" also requires satisfying (14), which may be difficul in the case of off-the-shelf converters. In some cases of low-switching frequency systems, (14) may fail for "Solution 1" also. Therefore, "Solution 2" is proposed, which does not require condition (14) and it can even be used for cases, where the ESL is not negligible.

Solution 2: The reason for the decrease in accuracy if condition (14) fails or if there is a presence of ESL is that the reactance voltage drop is not negligible. The presence of appreciable capacitive or inductive reactance will introduce error, if (10) is used. To improve the estimation accuracy, the ESR voltage drop "V_{ESR}" must be extracted from the capacitor terminal voltage V_C. Since the ESR voltage drop "V_{ESR}" is in phase with the capacitor current "I_C", the phase difference between capacitor terminal voltage V_C and the ESR voltage drop "V_{ESR}" can be measured using the BPF outputs of the capacitor's terminal voltage and capacitor current. Once the phase difference "θ" between V_{ESR} and V_C is known, then the following equation can be written using Pythagorean trigonometric identity to extract V_{ESR} from the terminal voltage V_C

$$\cos\theta = \frac{V_{\mathrm{ESR}}}{V_C}. \tag{16}$$

If the phase difference "θ" and the capacitor's terminal voltage "V_C" are known, V_{ESR} can be estimated. Using (5), for a frequency component of frequency f

$$\mathrm{ESR}_f = \frac{V_{C\_f} \times \cos\theta_f}{I_{C\_f}} = \frac{V_{C\_f\mathrm{PEAK}} \times \cos\theta_f}{I_{C\_f\mathrm{PEAK}}}. \tag{17}$$

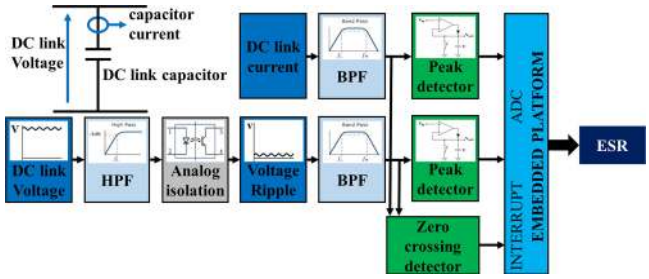

Fig. 8. Block diagram of the proposed ESR estimation scheme.

The phase difference "θ_f" can be measured as the phase difference between capacitor voltage and current. As the voltage drop across ESR is used, (17) can be used to estimate the ESR accurately, irrespective of the presence of reactive components.

Figure 8 shows the block diagram of the ESR estimation scheme. The only difference would be the sign of "θ" between the dominantly capacitive and dominantly inductive cases. This method requires filterin of switching frequency components using either analog or digital BPFs. The peak values of BPF output can be extracted using a simple peak detector (PD) circuit and the ESR estimation method based on (17) can be implemented in a low-cost microcontroller as the bandwidth requirement is low. Even though "Solution 1" can be used when (14) fails, it cannot be used in cases where the capacitor parameters at the required frequency are not known to ensure (14) or the ESL is not negligible, as shown in Fig. 7(c). On the other hand, "Solution 2" can be used for all the cases and it does not require ensuring (14) or negligible ESL. Therefore, this paper focuses on "Solution 2" and the following section presents the simulation and experimental results for "Solution 2."

IV. Simulation Results

A simulation model is developed using the PSpice circuit simulator for testing the ESR estimation scheme in the front-end rectifie -fed three-phase inverter circuit shown in Fig. 4. The equivalent circuit model shown in Fig. 2(b) is used to model the dc-link capacitor. The equivalent circuit parameters are capacitance 1000 μF, ESR 45 mΩ, and ESL 10 nH. SPWM switching pulses are generated at the switching frequency of 5 kHz. This switching frequency is selected because both "Solution 1" and "Solution 2" can be used. In this simulation model, the variation of ESR with frequency and temperature are not considered.

Since the ESR estimation scheme is based on extracting the switching frequency components, the Sallen–Key topology BPFs are designed using the method explained in [26] to extract the required harmonic components. Since the ac content of capacitor voltage rides on the top of high dc voltage of the dc link, it is filtere using a high-pass filte before the BPF stage.

The ESR estimation procedure is simulated in the PSpice circuit simulator as follows. To decide the appropriate ESR estimation solution, condition (14) is applied for the switching frequency of 5 kHz, capacitance 1000 μF, and ESR 45 mΩ.

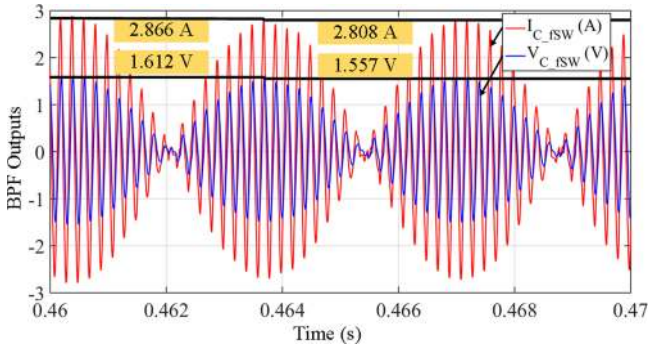

Fig. 9. BPF outputs—Capacitor voltage and current (5 kHz).

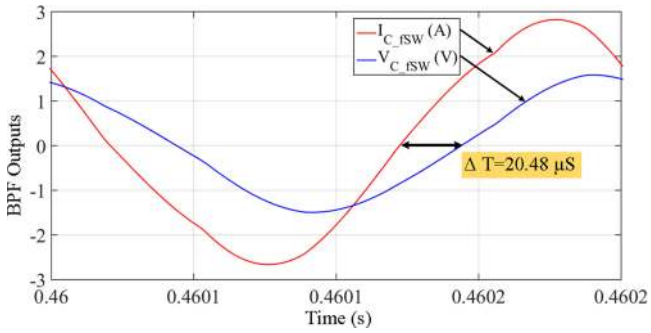

Fig. 10. Phase difference between capacitor voltage and current (5 kHz).

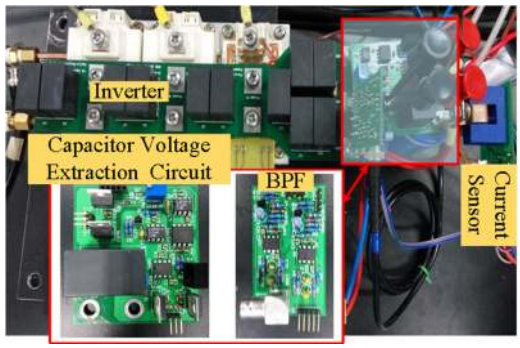

Fig. 11. Experimental setup of an front-end rectifie -fed three-phase inverter equipped with the proposed ESR estimation circuit.

TABLE I
DC-LINK CAPACITOR PARAMETERS

Sample No.	Manufacturer Part No.	Capacitance (2.5 kHz and 25 ºC)	ESR (2.5 kHz and 25 ºC)
C1	Cornell Dubilier 500R112M500BC2B	954.4 μF	46.4 mΩ
C2	Cornell Dubilier 500R112M500BC2B	963.7 μF	44.8 mΩ
C3	Kemet ALS30AKF450	850.9 μF	39.5 mΩ
C4	Kemet ALS30AKF450	845.6 μF	39.8 mΩ

The switching frequency (5 kHz) is less than 11 047 Hz, the frequency limit set by (14), and therefore, condition (14) fails. Since $3f_{\mathrm{SW}}$ (15 kHz) is greater than 11 047 Hz, "Solution 1" can be used to estimate the ESR at 15 kHz as shown in [1]. In this paper, the simulation results are shown only for the ESR estimation using "Solution 2" as it is more promising for industrial power converters.

To estimate the ESR using the method described in "Solution 2", the Sallen–Key BPFs are used to filte the harmonics around 5 kHz. The BPF has a gain of 10 for 5-kHz components. When the BPF is used to filte out 5 kHz, the output of the filte will have the resultant of two frequency components shown in the FFT analysis [see Fig. 6(a) and (b)] on either side of 5 kHz at 4850 and 5150 Hz. The resultant component will reach its peak every 3.33 ms, corresponding to 300 Hz, which is the difference between the frequencies of two components. Fig. 9 shows the BPF outputs for the ac content of the capacitor voltage and the capacitor current. The ESR estimation using "Solution 2" requires the peak values of extracted harmonic components and the phase difference between them. The average of peaks over 10-ms period is used to account for the intrinsic variations in peak values. From Fig. 10, the zero crossings of extracted capacitor voltage and current are 20.48 μs apart, which corresponds to a phase difference of $\theta_{5k} = 0.6434$ rad.

Using a scaling factor of 0.1 to account for the sensor and filte gains in (17), the ESR can be estimated as follows:

$$\mathrm{ESR}_{5k} = \frac{\left(\frac{1.612+1.557}{2}\right) \times 0.1 \times \cos 0.6434}{\left(\frac{2.866+2.808}{2}\right)}$$
$$= 44.68\ \mathrm{m\Omega}. \quad (18)$$

The actual value of the ESR is 45 mΩ and the error in estimation is 0.32 mΩ (or 0.7%). If the effect of capacitive reactance is not considered as in the case of existing methods, the estimation of the ESR using (10) would have given 55.85 mΩ against the actual value of 45 mΩ (24% error), which is not acceptable.

V. EXPERIMENTAL RESULTS

The ESR estimation method is verifie experimentally using a custom-made front-end rectifie -fed three-phase inverter setup before it is implemented in an industrial power converter. This is because the industrial power converter has a lot of constraints in terms of space and customization of components, whereas the custom-made converter can be modifie easily for testing the ESR estimation method reliably. The experimental setup is shown in Fig. 11. The switching pulses for the inverter are generated using the SPWM strategy and the switching frequency of the inverter is 2.5 kHz. The switching pulse generation strategy and the ESR estimation algorithm are implemented using the PE-Expert4 controller board from Myway. The experiment is repeated for four different capacitor samples given in Table I. As the ESR is a temperature dependent parameter, the core temperature of the capacitor is necessary to verify the accuracy of this method in real operating conditions. For this purpose, the capacitors used in this experiment have embedded thermocouples to measure the core temperature with better accuracy. The core temperature can be used to validate the estimated ESR at different operating temperatures.

Apart from the core temperature, the actual value of the ESR at present operating conditions is also necessary to validate the estimated ESR. Therefore, the ESR values at different core

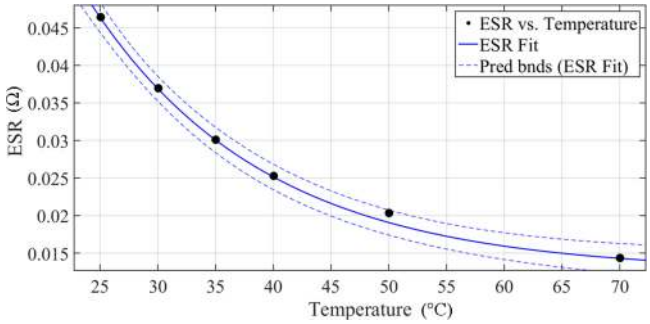

Fig. 12. Thermal response of the ESR.

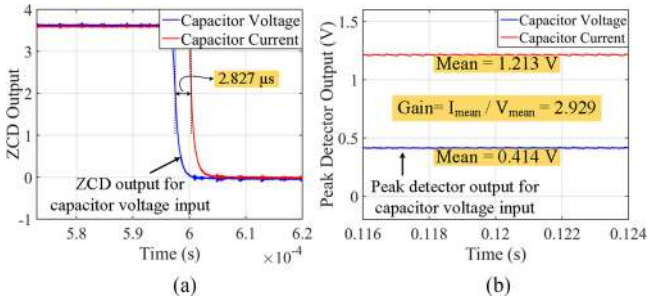

Fig. 13. Experimental results for sensor calibration. (a) ZCD outputs for phase calibration. (b) PD outputs for phase calibration.

temperatures are measured using an *LCR* meter. In order to measure the ESR at almost the same temperature conditions as in real operating conditions, the capacitor is kept in ambient temperature and heated up through the power loss generated using AMETEK power supply CSW5550 in dc + ac mode. Since the capacitor parameters cannot be measured when the capacitor is connected to the power supply, the capacitor is heated up to a temperature greater than 70 °C and the measurements are done when the capacitor is cooling down. The variation of the ESR with temperature is modeled as a mathematical equation using the curve fittin technique in MATLAB. Fig. 12 shows the curve fittin plot and its results. The thermal behavior of the ESR is modeled as follows:

$$\text{ESR}\ (T) = \left(\alpha * e^{-\beta*(T-25)}\right) + \gamma \tag{19}$$

where $\alpha = 0.03385$, $\beta = 0.06588$, and $\gamma = 0.01255$ obtained by curve fittin are the constants for the capacitor used. Once the operating temperature and thermal behavior mathematical model of the ESR in (19) are known, the ESR estimated at any temperature can be validated by comparing its actual value. In condition monitoring applications, the thermal behavior model of the ESR can be used as the initial values of the ESR and the health of the capacitor is determined based on the deviation of the estimated value of the ESR from its initial value. In case of industrial power converters, where the thermal behavior model is not known, the initial value of the ESR at different operating temperatures can be measured during transient conditions or different operating conditions.

The ESR estimation circuit has three important components, namely the circuit to extract the ac content of capacitor voltage, the capacitor current measurement circuit, and the BPF circuit. The components of the ESR estimation circuit are shown in Fig. 11. The circuit to extract the ac content of capacitor voltage consists of a high-pass f lter to f lter out the dc content followed by an analog isolation circuit using HCNR201. The ac content of the capacitor voltage from analog isolation circuit is passed through the Sallen–Key BPF to extract the voltage harmonics around 2.5 kHz. The capacitor current is measured using the commercial current sensor with part number LA-55P. The measured current is then filtere using the Sallen–Key BPF to extract the capacitor current harmonics around 2.5 kHz. The peak values of voltage and current harmonics are extracted using PD circuits. The phase difference between voltage and current is calculated by using the zero crossing detector (ZCD) circuits and the timer function in PE-Expert4.

In spite of the meticulous design, the intrinsic variations in the components used for BPFs, different scaling factors and phase shifts introduced by the voltage and current sensors may introduce some variations in the BPF output's magnitude and phase, which will affect the estimation accuracy. Therefore, the following calibration procedure is adopted to calibrate the estimation circuit. Ideally, if the same signal is given to the voltage and the current input of the estimation circuit, the ratio of PD outputs should be unity and the phase difference should be zero making the estimated ESR equal to "1" as follows

$$\text{ESR}_f = \frac{V_{C\_f\text{PEAK}}}{I_{C\_f\text{PEAK}}} \times \cos\theta_f = 1 \times \cos 0 = 1. \tag{20}$$

The calibration procedure adopted here aims to satisfy (20) by introducing a gain factor and phase in the actual equation for the ESR (17) to account for the offsets and phase shifts. The equation for the ESR with calibration constants for magnitude and phase is

$$\text{ESR}_f = \frac{V_{C\_f\text{PEAK}} \times \text{Gain} \times \cos(\theta_f - \emptyset)}{I_{C\_f\text{PEAK}}}. \tag{21}$$

The voltage and current inputs of the estimation circuit are fed with the same signal at 2.5 kHz. The calibration procedure is repeated for different signal levels. From the experimental results, the multiplication factor to make the ratio of $V_{c\_f\text{PEAK}}$ to $I_{c\_f\text{PEAK}}$ unity is calculated as 2.97. Therefore, the actual value "Gain" in (21) calculated by including the scaling factor of current sensor is 0.1485. Similarly, the average value of phase shift constant "$\emptyset$" calculated using the calibration procedure is 0.04276 rad. Fig. 13(a) shows the ZCD outputs for phase shift measurement and Fig. 13(b) shows the PD outputs for calculating "Gain." With these calibration constants, the ESR can be estimated using

$$\text{ESR}_f = \frac{V_{C\_f\text{PEAK}} \times 0.1485 \times \cos(\theta_f - 0.04276)}{I_{C\_f\text{PEAK}}}. \tag{22}$$

Finally, the experiment is carried out with *C*1 as the dc-link capacitor. The dc-link capacitor voltage is maintained around 100 V. Fig. 14 shows the BPF output peaks and the phase difference for calculating the ESR. The results shown are estimated at an operating temperature of 23.6 °C, which is the room temperature before starting the experiment, and the results are taken as

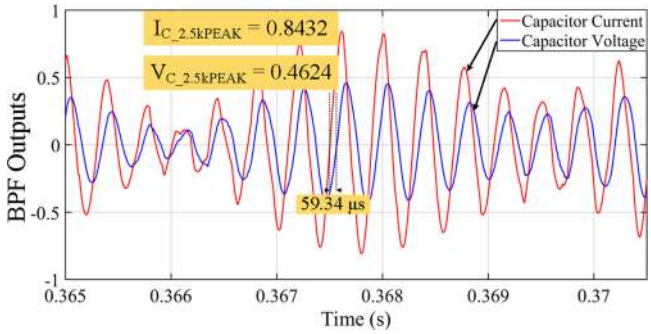

Fig. 14. BPF outputs for the capacitor voltage and current.

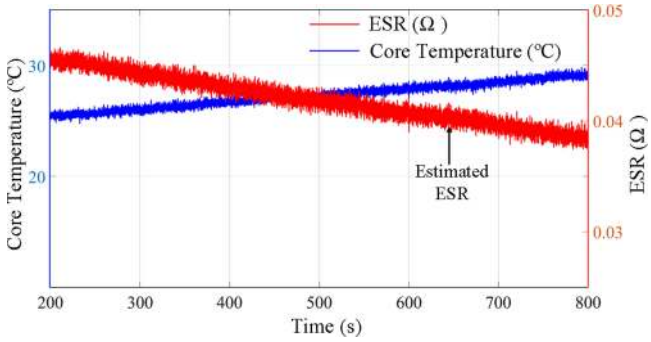

Fig. 15. Estimated ESR and core temperature of one capacitor sample.

soon as the inverter is turned ON. It is also verifie by measuring the core temperature of the capacitor using thermocouple.

For the switching frequency of 2.5 kHz, θ can be calculated using

$$\theta = \frac{\Delta T}{2 \times 10^{-4}} \times \pi \text{ rad} \tag{23}$$

where ΔT is the time difference between the BPF outputs of voltage and current, 2×10^{-4} is used because π rad correspond to 200 μs for 2.5 kHz. From Fig. 14, $\Delta T = 0.5934 \times 10^{-4}$. Therefore, θ can be calculated using (23) as 0.9321 rad. For the experimental results shown in Fig. 14, the ESR of capacitor $C1$ can be estimated using (22) and the estimated ESR is as follows:

$$\text{ESR}_{2.5k} = 51.30 \text{ m}\Omega. \tag{24}$$

From (19), the actual value of the ESR at 23.6 °C is 49.67 mΩ. Therefore, the error in the ESR estimation is 1.63 mΩ (3.28%). The ESR estimation is explained using one cycle of BPF output shown in Fig. 14. In PE-Expert4, the results from every 50 cycles are averaged to achieve better accuracy. Fig. 15 shows the plot of the estimated ESR and the corresponding core temperature for $C1$ from PE-Expert4. This experiment is repeated for the capacitor samples $C2$, $C3$, and $C4$. The comparison of the estimated ESR with actual ESR measured using the *LCR* meter is given in Table II.

In real scenario, prior measurements, such as the thermal response of ESR and thermal resistance, are not needed. Those measurements are done only to validate the proposed method reliably. The condition monitoring system requires only the initial value of ESR measurements and it can be taken by the monitoring system when the converter is introduced into service. The thermal resistance and capacitance can be usually found in the datasheet or else the manufacturer can provide those data. Also, the calibration procedure is a one-time process during the production stage.

TABLE II
ESTIMATION RESULTS SUMMARY

Sample No.	Actual ESR (2.5 kHz and 23.6 ºC)	Estimated ESR (2.5 kHz and 23.6 ºC)	Percentage Error
C1	49.67 mΩ	50.73 mΩ	2.13 %
C2	47.91 mΩ	49.54 mΩ	3.40 %
C3	42.48 mΩ	44.12 mΩ	3.86 %
C4	42.63 mΩ	44.21 mΩ	3.71 %

To prove the applicability of the ESR estimation method [1] to industrial power converters, the proposed method is also implemented in Vacon NXP 0016 5A2H1SSS ac drive system. The capacitor with part number ALS30R1009KF (1000 μF, 420 V) is used as the dc-link capacitor. Some important changes are made to make the method suitable for industrial power converter compared to the method used in the custom-made inverter, which are given as follows.

1) In industrial power converters, the conventional current sensors cannot be used to measure the capacitor current because it requires modificatio in the existing circuit, which is not preferred. Another disadvantage is the additional inductance introduced by the sensor. Therefore, the capacitor current is measured using a Rogowski coil-based current sensor from Power Electronic Measurements Ltd because of the advantages, such as very low inductance, lesser space requirements, and high bandwidth. Using a commercial Rogowski coil may seem expensive. But large-scale implementation of this method and developments in Rogowski current sensor technology can bring down the cost greatly.
2) In most cases, the capacitors in industrial power converters do not have in-built temperature sensors to measure the core temperature. Therefore, the core temperature is estimated using the thermal model.

Adding the condition monitoring circuit to an existing ac drive requires the following steps:

1) attaching the voltage input leads of monitoring circuit to the capacitor's terminals;
2) installing Rogowski current sensor around capacitor's terminal;
3) attaching the temperature sensor to the capacitor.

The thermal resistance R_{th} of the capacitor from core to case is 0.84. If the power loss inside the capacitor and the case temperature are known, the core temperature of the capacitor in steady state can be estimated using [27] as follows

$$T_{\text{CORE}} = T_{\text{CASE}} + P_{\text{LOSS}} \times R_{\text{CC}}. \tag{25}$$

The case temperature of the capacitor is measured using LMT70 temperature sensor. The power loss inside the capacitor is calculated digitally based on (26) using the capacitor voltage and current. This power loss computation method has been pro-

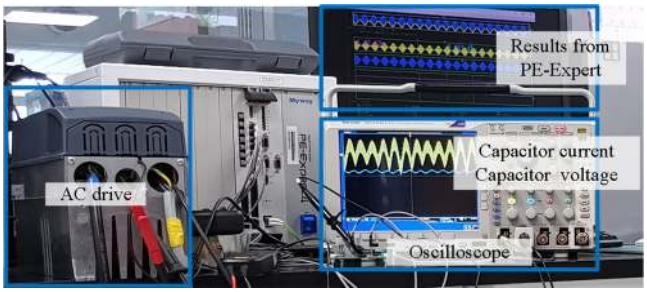

Fig. 16. Condition monitoring of an industrial power converter.

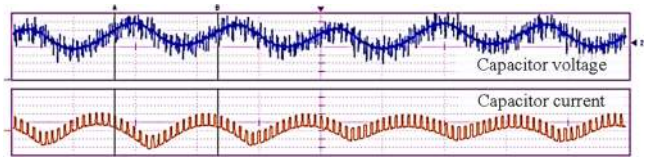

Fig. 17. Experimental waveforms of the capacitor voltage and current.

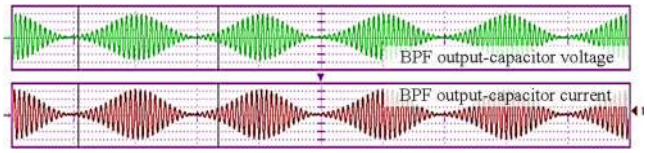

Fig. 18. BPF outputs of the respective waveforms in Fig. 17.

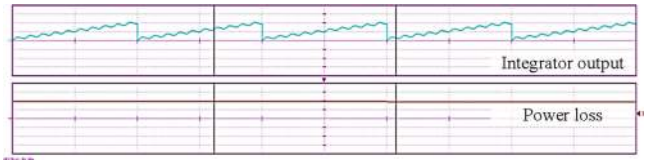

Fig. 19. Online power-loss calculation of the capacitor.

posed in [28] to estimate the ESR. The power loss computation based on (26) can be implemented in a low-cost microcontroller as most of the computations are simple multiplication followed by addition and the complex division operation is performed only once per integration period

$$P_{\mathrm{LOSS}} = \frac{1}{T}\int_0^T v_c(t) i_c(t)\,\mathrm{dt}. \tag{26}$$

Figure 16 shows the experimental setup using a commercial ac drive from Vacon. The capacitor voltage and current are shown in Fig. 17. The BPF outputs for the ESR estimation are shown in Fig. 18. The power loss calculation is shown in Fig. 19. Since the phase shifts introduced by voltage and current sensors vary with frequency, it is difficul to account them in power loss calculation and are neglected. Therefore, some error in temperature estimation is expected due to the phase shifts introduced by sensors. The experimental results showed that the maximum error in temperature estimation is 5 °C. As the slope of the ESR versus frequency curve decreases with the increase in temperature, as shown in Fig. 12, the temperature estimation error of 5

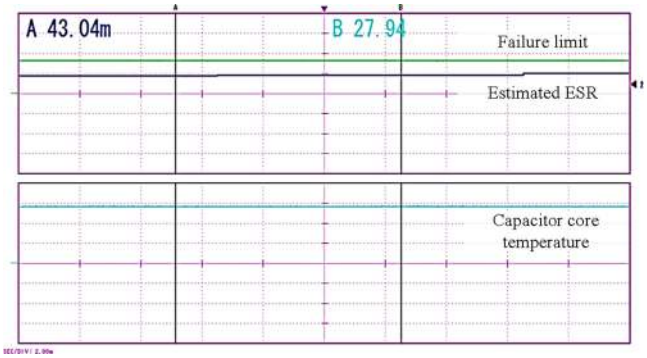

Fig. 20. Failure limit, estimated ESR, and core temperature.

°C can be tolerated for condition monitoring applications as the failure threshold is twice the initial value of the ESR as specifie in the manufacturer datasheet. The experimental results of core temperature, estimated ESR, and failure threshold limit are shown in Fig. 20. The failure threshold limit is calculated at the present core temperature. The capacitor is considered to be failed when the estimated ESR rises above the failure threshold.

VI. Conclusion

A condition monitoring technique for industrial power converters based on ESR estimation has been presented in this paper. The ESR estimation circuit requires only a few op-amps, passive elements, and a low-cost microcontroller to estimate the ESR. The ESR estimation method has been validated experimentally using a custom-made inverter. The adaptation of the ESR estimation method [1] for the condition monitoring of capacitors in industrial power converters is discussed and the experimental results are presented for Vacon NXP 0016 5A2H1SSS ac drive system. As the ESR is dependent on the operating temperature of the capacitor, the thermal behavior of the ESR is modeled using the curve fittin technique. Once the core temperature is known, the ESR estimated at any temperature can be compared to its initial value at the same temperature using the thermal behavior model of the ESR to estimate the capacitor's health. The core temperature is measured using a thermocouple for the custom-made converter whereas in the case of industrial power converters, the thermal model of capacitor is used. Although capacitor current measurement using a Rogowski-based current sensor has many advantages, it increases the overall cost of the system. The future research will focus on developing ESR estimation methods that do not require direct capacitor current measurement. Moreover, the accuracy of the temperature estimation method needs to be improved as the operating temperature is one of the important factors that decide a capacitor's life.

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