Open Defects Detection within 6T SRAM Cells using a No Write Recovery Test Mode

Josh Yang, Baosheng Wang and André Ivanov
SOC Lab, Department of Electrical & Computer Engineering, University of British Columbia, Vancouver, B.C., Canada, V6T 1Z4
{joshy, baosheng, ivanov}@ece.ubc.ca

Abstract

The detection of all open defects within 6T SRAM cells is always a challenge due to the significant test time requirements. This paper proposes a new design-for-test (DFT) technique that we refer to as No Write Recovery Test Mode (NWRTM) to detect all open defects, some of which produce Data Retention Faults (DRFs) but are undetectable by typical March tests. We demonstrate the effectiveness of our proposed technique by only applying it to fault-free memory cells and faulty cells with those undetectable defects but all the open defects are covered since our DFT technique is implemented by simply adding extra test cycles into typical March tests. Two 6T SRAM cell models, one a high-speed version and the other a low-power one, representing extreme cases according to traditional design methodologies, were designed to validate our proposed NWRTM at the circuit level. Simulation results show that our NWRTM amounts to a shorter total test time and improved open defect detection capability. In addition, in comparison to other DFT techniques, NWRTM requires the least additional design effort, and imply less area and no performance penalties.

Keywords: Memory testing, Open Defects, 6T SRAM, Test Time, Area Penalty, Write Recovery

1. Introduction

The nature of SRAM testing is different from that of logic testing since a memory is actually more of a mixed-signal device whose faulty behavior is often analog in nature. Thus, defect coverage, instead of fault coverage, provides a better estimate for overall test quality [1]. However, within the 6T SRAM cells, the detection of some open defects producing Data Retention Faults (DRFs) has been shown to amount to a very time consuming process. These faults are generally not detected by typical March tests but can be detected by reading the memory cells after a certain delay time [2]. Therefore, achieving high defect coverage by detecting all the open defects within 6T SRAM cells poses large challenges in regards to test time.

Previous Design-for-Test (DFT) techniques on detecting these DRFs mainly focus on removing the delay time from the detection process by incorporating these specialized techniques and associated algorithms [3-6]. By applying simple power supply current monitoring techniques, e.g., [3] and [4], most open defects can be detected without introducing additional delay time in the test sequences. Alternatively, by introducing hardware modifications in addition to specialized test algorithms, in [5] and [6], the special write disturb schemes on each column I/O are designed to distinguish defective cells from good ones.

Using similar concepts to those exploited in [5] and [6], this paper proposes a technique that we refer to as *No Write Recovery Test Mode (NWRTM)* as an alternative or supplement to those in [5] and [6]. The major difference between our technique and the former resides in the type of cell that fails to flip logic value as a consequence of the designated Write operation. In the schemes proposed in [5] and [6], good cells fail to flip, while in our case faulty cells will fail to flip. This latter feature yields the advantage that the NWRTM can be merged into any March tests, e.g., March 9N, since it can share the same write operations mechanism with them, i.e., faulty cells will fail to flip during the tests. In other words, NWRTM has the advantageous characteristic of being mergable into any typical March tests without incurring additional test patterns, as do other DFT techniques. Hence, NWRTM yields easy open defects detection at fewer design efforts.

Moreover, symmetric and asymmetric defects on the faulty PMOS source or drain sides are built in the open defect cell models in [3-6]. In this paper, all the possible operations on the faulty cells are examined in the presence of an open. In other words, the proposed NWTRM is validated under a more complete defect model. In addition, our validation experiments show that our technique amounts to virtually negligible penalties in regards to design effort, area, and no performance impacts.

The remainder of this paper is organized as follows. In Sec. 2, some background is introduced. The proposed NWRTM is presented in detail in Sec. 3, as well as its

IEEE COMPUTER SOCIETY

merging into typical March tests, e.g., March 9N. To validate the proposed technique at the circuit level, two extreme cases of SRAM cells were designed according to the design methodology in [8] and using a 0.18um technology. These designs are presented in Sec. 4. Simulation results are compared and also discussed in Sec. 4. The evaluations of the proposed NWRTM are discussed in Sec. 5. Finally, Sec. 6 draws some conclusions.

2. Open Defects within a 6T SRAM Cell

In order to easily define all potential opens within a cell, a graph that corresponds to the circuit diagram in Figure 1, can readily be derived. In this graph, every branch is labeled by such a potential defect. Due to the symmetric structure of the memory cell, opens at locations Ocx and Ocxc (where "x" and "xc" denote node numbers) show a complementary fault behavior [9]. Thus, only the faults denoted by Ocx need to be considered when examining all possible operations in the presence of an open.

Among those opens, only OC1, OC2, OC5 and OC11 are producing DRFs and undetectable by using any typical March test according to [3-6] and [9]. Because these are all related with the pull up PMOS components, we refer to such open defects as "All the Open Defects Related to the PMOS" or AODRP for simplicity. Subsequently, we focus on special techniques required to test the faults caused by any one of the AODRP.

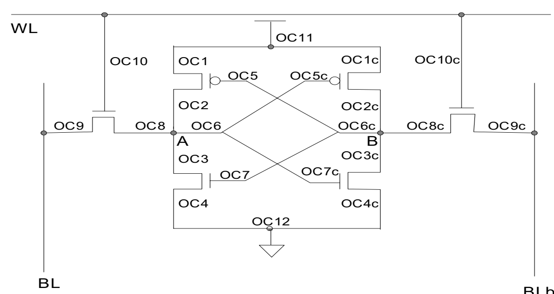

Figure 1. Opens within a 6T Cell

3. No Write Recovery Test Mode (NWRTM)

3.1 Concepts

Similarly to the methodology in [5] and [6], in NWRTM, a special write cycle is created to distinguish a good cell from a faulty cell subjected to an open defect of AODRP. We use the cell shown in Figure 1 to illustrate the differences between our specifically designed write cycle and the normal write cycle. Due to the symmetric structure of the memory cell, we only explicitly illustrate the W1 cycle with the initially stored cell value of ZERO. The dual cycle should be obvious to the reader.

During the normal W1 cycle, node B is pulled down by the bitline BLb, driven to strong GND by the write control logic, and node A is pulled up due to the charge sharing with the floating bitline BL that has already been pre-charged to VCC, where strong GND means the node is driven at GND voltage level by some sources. Due to the latch mechanism of the memory cell, the cell flips its value from ZERO to ONE as long as the voltage level of node B is pulled to a sufficiently low level.

In [5] and [6], by setting the bitlines BL and BLb to some certain voltage level between VCC and GND during the write operation, i.e., during the time when the access NMOS is on, a good cell fails to flip but a faulty cell would. Following a similar concept, we set the voltage level of BL and BLb to weak GND and strong GND respectively, here weak GND means the node voltage level is at GND but no sources drive this node. This causes an opposite result, i.e., a good cell succeeds at flipping its logic value while a faulty cell fails to do so. For a good cell, there is no problem in writing a ONE because node B can be pulled down by BLb and the cell can flip to ONE due to the latch mechanism. However, for a faulty cell subject to any of AODRP, it fails to flip because the voltage level of node A never exceeds that of node B. The voltage level of node A always remains at GND since (i) lacking the PMOS or path to the supply rail, node A is not pulled high regardless of how low the node B voltage level reaches, so the latch in this faulty cell malfunctions; and (ii) there are no charge sharing effects with BL because we set BL at weak GND. Since GND is the lowest achievable voltage level and node A remains at GND, the voltage level of node A never exceeds that of node B and thus the faulty cell fails to flip.

3.2 Implementations

To present the proposed implementations, we define some related terms in this section.

Bit line pre-charge state: here, we assume that the bit lines are pre-charged to the supply voltage level.

Write Recovery (WR): the operation where all the bit lines and data lines are charged back to the pre-charge state in the write cycle.

No Write Recovery Cycle (NWRC): a write cycle with no Write Recovery (NWR) operation, i.e., the bitlines remain at the previous state right after the write cycle is completed.

To implement the concept of NWRTM, i.e., setting the voltage levels of BL and BLb to weak GND and strong GND, respectively, in the write operation, we follow the latter cycle with a NWRC with a complementary value. From Sec. 3.1, a faulty cell will fail to flip in the

IEEE COMPUTER SOCIETY

NWTRM, just as it would in a conventional March test. Therefore, it is easy to merge NWRTM with any typical tests by using the two steps below instead of adding extra test patterns like in [3-6]: (i) remove all the test sets that are specially designed to detect AODRP or data retention faults; (ii) add a NWRC before the write cycle.

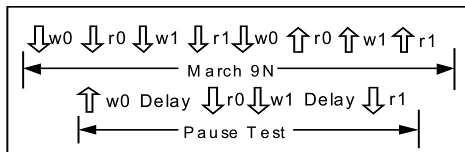

Figure 2. The March 9N Test and Pause Test

To illustrate the NWRTM, we use the popular March 9N test algorithm with Data Retention Test. This algorithm is shown in Figure 2, where, "⇑" represents an increasing address sequencing during test, while "⇓" represents a decreasing address sequence. "Delay" denotes a specific time assumed to be required for detecting DRFs. Moreover, "0" and "1" represent the test patterns and their complementary values, i.e., "5" and "A" of the check-board test patterns, instead of only ZERO and ONE. To more clearly illustrate our NWRTM, we divide March 9N with Data Retention test algorithm into two stages: a first stage is a "Pause" test targeting the Data Retention faults and the other is March 9N.

According to the two steps above, the newly generated March test algorithm that we refer to as the *No Write Recovery March Test Algorithm (March NWR)* is shown in Figure 3, where "Nw0/Nw1" represents writing 0/1 in the NWRC and the parts involving the NWRC are referred to as NWRTM0 and NWRTM1, respectively.

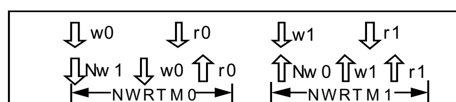

Figure 3. The March NWR

3.3 Operations

Before presenting detailed explanations of the March NWR operations, we need to specify some additional notation and terminology. In the forgoing, "X" denotes an unknown value, (w) represents a weak voltage on a node, "→" represents a node voltage moving in the direction of a certain logic value, while "0" corresponds to the GND voltage level.

March NWR amounts to not changing any normally test part of a March 9N test set, but simply adding two NWRCs. Hence, we only need to explain the detection of AODRP that are not detectable by typical tests like March 9N. Due to the symmetric structure of a memory cell, here we only describe the operations of the test cycles NWRTM1 (NW0 W1 R1) for detecting AODRP in the cell shown in Figure1. By symmetry, the behavior and function of complementary NWRTM0 (NW1 W0 R0) should be obvious to the reader.

(i) Fault-Free Cell

Table 1 shows the voltage levels of bit lines and storage nodes in a fault-free cell when applying NWRTM1.

Table 1. NWRTM1 on a Fault-Free Cell

Patterns		BL	BLb	A	B
Initial		VCC	VCC	X	X
NW0	WL on	0	VCC (w)	→0	→VCC
	WL off	0	VCC (w)	0	VCC
	NWR	0 (w)	VCC (w)	0	VCC
W1	WL on	0 (w)	0	→ >0	0
	WL off	0 (w)	0 (w)	→ VCC	0
	WR	VCC	VCC	VCC	0
R1	WL on	VCC(w)	<VCC-VTN	VCC	0

Initially the bit lines are in the pre-charge state and the memory cell storage value is unknown before entering the NWRTM, so both bit lines will float with the voltage levels GND and VCC respectively, after the NWRC. In the subsequent W1 cycle, the cell flips to ONE as long as the voltage level of node B is pulled down to a sufficiently low voltage due to the cell's latch mechanism. Therefore, the return value of the R1 operation is expected to be the correct one.

(ii) Faulty PMOS Cell: Open at OC1, OC2 or OC5

Table 2 shows the voltage levels of bitlines and storage nodes in a faulty PMOS cell when applying NWRTM1.

Table 2. NWRTM1 on a Faulty PMOS Cell

Patterns		BL	BLb	A	B
Initial		VCC	VCC	X	X
NW0	WL on	0	VCC (w)	→0	→VCC
	WL off	0	VCC (w)	0	VCC
	NWR	0 (w)	VCC (w)	0	VCC
W1	WL on	0 (w)	0	0	>0
	WL off	0 (w)	0 (w)	0	→VCC
	WR	VCC	VCC	0	VCC
R1	WL on	<VCC-VTN	VCC (w)	0	VCC

Compared with the fault-free cell in Table 1, in this case, the cell fails to return a correct value ONE in the R1 cycle because the voltage level of BL is lower than that of BLb. The reason for this failure is that a ONE is not successfully written into this faulty cell after the NW0 operation. In the W1 cycle, the lack of the pull-up PMOS and charge sharing effects with BL results in node A not being pulled high. As a result, node A remains at its GND voltage level all the time and node B eventually charges back to VCC when the word line is turned off. In other

1063-9667/04 $ 20.00 © 2004 IEEE

IEEE COMPUTER SOCIETY

words, the stored value after the W1 cycle is still ZERO. Obviously, this defect is detected when the return value in the following R1 cycle is ZERO.

(iii) Faulty Cell at VCC with an Open OC11

Table 3 lists the voltage levels of bit lines and memory cell storage nodes in a faulty cell at VCC with an open defect in VCC when applying NWRTM1. With a similar faulty behavior as that of the faulty PMOS cell in Table 2, in this case the cell will not return a ONE in the R1 cycle because node A always remains at GND and thus assumes a lower voltage that of node B by the end of the W1 cycle. Consequently, in the subsequent R1 cycle the voltage level of BL is lower than that of BLb in the following R1 cycle. As a result, the returned value from the following R1 cycle will not be ONE.

Table 3. NWRTM1 on a Faulty Cell at VCC

Patterns		BL	BLb	A	B
Initial		VCC	VCC	X	X
NW0	WL on	0	VCC (w)	→0	→VCC-VTN
	WL off	0	VCC (w)	0	VCC-VTN
	NWR	0 (w)	VCC (w)	0	VCC-VTN
W1	WL on	0(w)	0	0	>0
	WL off	0(w)	0(w)	0	>0
	WR	VCC	VCC	0	>0
R1	WL on	BL < BLb		A < B	

4. Experimental Results

To validate the proposed March NWR, models of twelve faulty cells, each with one of the twelve possible open defects stated in Sec. 2 were implemented. These were modeled for a 0.18µm technology using TSMC Salicide 1P6M 1.8V SPICE model. Each open defect is modeled by a single resistance ranging in value from 1 KΩ to 1000 GΩ on a logarithmic scale, just as in [7]. Three test patterns corresponding to the March 9N, Pause Test and the March NWR are applied to our faulty cells.

4.1 SRAM Models

For simplicity but without losing generality, the SRAM simulation model shown in Figure 4 that includes one memory column I/O was developed. That is, our model includes one memory cell, two pre-charge PMOS, two equivalent bitline loadings, and two simplified write control NMOS gates. Both WR0 and WR1 are inactive low in the read cycle. In the write cycle, WR0 (WR1) is active high and WR1 (WR0) is inactive low while writing data 0(1) into the memory cell.

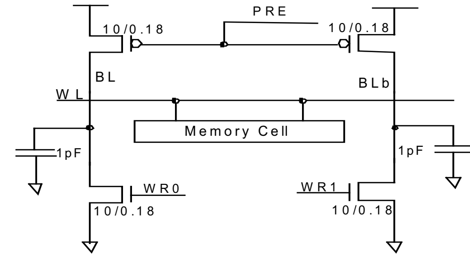

Figure 4. The SRAM Circuit Simulation Model

In order to run the circuit level simulations, the pre-charge PMOS devices and write control NMOS devices are assumed to be of the same size, i.e., 10/0.18 um (width/length), and the bit line capacitance is assumed to be 1pf. Using the traditional methodology in [8], we design two extreme cases, high-speed and low-power, to evaluate our entire faulty cell cases under the following simulation parameters and variations (corners): (i) 10% variation on supply voltage (1.62 -- 1.98V); (ii) temperature effects (0 -- 100^{0}C); (iii) MOS Models (SS, SF, TT, FS, FF); (iv) Static Noise Margin in [10-11] > 0.18V (10% of power supply). The transistor size of both of them, Cell_LP for lower power case and Cell_HS for high speed one, is shown in Table 4.

Table 4. Transistor Sizes of Memory Cells

	Cell_LP (um)	Cell_HS (um)
Pull-up PMOS	0.22/0.18	0.22/0.18
Pull-down NMOS	0.22/0.18	0.405/0.18
Access NMOS	0.22/0.29	0.22/0.18

4.2 Input Test Patterns

Three input patterns represent three test algorithms respectively. The first corresponds to the simulation of the March 9N test algorithm: (i) initializing both bit lines to the pre-charge state and the stored value of the memory cell to ZERO; (ii) W1; (iii) R1; (iv) W0; (v) R0.

The second simulation trace corresponds to a Pause test: (i) initializing both bit lines to the pre-charge state and the stored value of the memory cell as ONE; (ii) pause for a delay of 2ms according to the simulations; (iii) R1.

The last patterns are specifically for the proposed March NWR: (i) initializing both bit lines to the pre-charge state and the stored value of the memory cell as ONE; (ii) NWR0; (iii) W1; (iv) R1; (v) NWR1; (vi) W0; (vii) R0.

To represent faulty behaviors of open defects during simulations, the following terminologies are defined.

Strong fault (SF): a fault that can be easily sensitized. In this paper, a strong faulty behavior occurs when, during a read cycle, the bit lines are changing into the inverse direction as expected, or the voltage difference between two bitlines is less than 2.5% of supply voltage.

1063-9667/04 $ 20.00 © 2004 IEEE

IEEE COMPUTER SOCIETY

Weak fault (WF): a fault that may or may not be sensitized. In this paper, we assume that a weak faulty behavior occurs when, during a read cycle, the value on the bit lines difference by an amount in the range 2.5% to 10% of power supply voltage.

Undetected fault (UF): a fault that is never sensitized by any read operation. In this paper, an undetected faulty behavior occurs when, during a read cycle, the bit line voltage differential exceeds 10% of supply voltage.

4.3 Validations

In order to save the space, the simulation results for all twelve opens are briefly listed in Table 5 in terms of faulty behavior and detectability. The detectability is quantified by the minimal value of open resistance that is detectable by the applied test patterns.

Table 5. Open Defects Detection Capabilities

Opens	Test Algorithms	Behavior	Detectability (LP/HS)
OC1	9N	UF	
	Pause	SF	1000 /1000 (Gohms)
	March NWR	SF	100/100 (Kohms)
OC2	9N	UF	
	Pause	SF	100/100 (Gohms)
	March NWR	SF	1/0.1 (Mohms)
OC3	9N	SF	100/100 (Kohms)
	March NWR	SF	100/100 (Kohms)
OC4	9N	SF	100/10 (Kohms)
	March NWR	SF	100/10 (Kohms)
OC5	9N	UF	
	Pause	UF	
	March NWR	SF	100/100 (Mohms)
OC6	9N	SF	100/10 (Mohms)
	March NWR	SF	100/10 (Mohms)
OC7	9N	SF	1/0.1 (Gohms)
	March NWR	SF	100/10 (Mohms)
OC8	9N	SF	100/100 (Kohms)
	March NWR	SF	100/100 (Kohms)
OC9	9N	SF	100/100 (Kohms)
	March NWR	SF	10/10 (Kohms)
OC10	9N	SF	100/100 (Mohms)
	March NWR	SF	100/100 (Mohms)
OC11	9N	UF	
	Pause	UF	
	March NWR	SF	10/10 (Mohms)
OC12	9N	WF	1/0.1 (Mohms)
	March NWR	WF	1/0.1 (Mohms)

In Table 5, the proposed March NWR can detect all the twelve defects while March 9N with data retention test (March 9N plus a Pause Test) can only detect ten of them. Moreover, the minimum detectable resistance values in our proposed test are not larger than that of the March 9N or Pause test for both extreme cases. In other words, the March NWR can detect all twelve open defects and its detectability is better than that of the March 9N with data retention tests for any SRAM cells designed according to the traditional design methodology in [8].

5. Evaluations

5.1 Test Time, Defect Coverage and Detectability

We used the same assumptions as in [5] to compare the test time, i.e., we assumed a memory array with 128 word lines, 250ms for the duration of the delay in the Pause Test and a clock period of 50 ns.

Table 6 shows the test time for the different test methods. Because the differences only lie in the detection of defects producing DRFs, only the test time required for specifically detecting these defects is listed. For typical Pause Test algorithms with 250ms delay, the test time is at least 500ms because of the two parts of delay. Due to the 4*128 test cycles and extra time required for exercising the DFTs, both the test times for the Weak Write Test Mode and IDDQ test schemes are about 26us. For NWRTM, because the test period of WWTM is longer than the normal read or write a cycle test period, which is shared by NWTRM according to [5], the test time is less than 13us, resulting from only two extra NWRCs. In other words, NWRTM reduces DRF test time by a factor greater than two in comparison to other DFT schemes.

Table 6. Test Time Comparisons

	Extra Cycles for DRFs	Test time
Pause Test	W0; delay; R0; W1; delay; R1	500ms
WWTM [5]	W0; R0; W1; R1	26us
IDDQ test	W0; R0; W1; R1	26us
NWRTM	Nw0; Nw1	<13us

From Sec. 4, the successful implementation of NWRTM shows both the defect coverage and detectability of the March NWR are better than that of March 9N test patterns augmented with data retention tests because the latter cannot detect two opens, OC5 and OC11, and the minimum detectable resistance values are not smaller than those for our proposed NWRTMA methodology.

5.2 Design Efforts, Area Penalty and Performance Impact

The necessary design effort in our NWRTM is simply a modification on the global logic control circuitry, i.e., disabling the write recovery operation in the no write recovery test cycle. In the case of other previous DFT schemes, not only is a global logical modification required to enter the special test mode but a special DFT circuitry also needs to be added in each column I/O or

IEEE COMPUTER SOCIETY

data I/O. For example, a generic weak RAM write (WRW) circuit is added in WWTM of [5] and a current sensor is required in IDDQ test scheme of [3]. The modifications on the column I/O or data I/O obviously amount to costly extra design efforts. These also amount to area penalties and cause negative performance impacts since the bit lines or data lines loads increase due to extra connections. In summary, it appears as though NWRTM yield detection benefits and test time reduction bearing negligible negative implications in regards to design efforts and area, and no performance impacts.

6. Conclusions

Specifically detecting open defects within 6T SRAM cells represents a major challenge in the context of general SRAM cells testing. The reason is that typical March tests combined with Pause tests, i.e., March 9N with Data Retention tests, are generally very time-consuming while other proposed DFT techniques, e.g., those in [3-6], amount to increased design efforts, increased area and negative performance impacts. Furthermore, due to their incomplete defect models (e.g., without OC5), all of the previously reported techniques may not detect all of the open defects within the cells.

In terms of Strong Faults or Weak Faults, all the open defects, including the undetectable opens at OC1, OC2, OC5 and OC11 under the write and read operations of the typical March test algorithms, are proved to be detected under the March NWR.

We validated the NWRTM when applied to two extreme SRAM cell designs (high speed and low power) under the comprehensive defect models. We showed that our proposed NWRTM can significantly reduce test time and improve defect coverage when detecting open defects, in comparison to those acquired by the combination of March 9N and Pause Test. In comparison to the previous DFT techniques reported in [3] and [5], not only is less test time with more complete defect model, but also our proposed NWRTM implies a smaller design effort, negligible area penalty and no performance impacts.

7. Acknowledgements

We wish to thank Gennum, NSERC, Micronet, and the Canadian Microelectronics Corp. for providing support for this work.

8. Reference

[1] Jee A., “Defect-oriented analysis of memory BIST tests”, Proceedings of the 2002 IEEE International Workshop on Memory Technology, Design and Testing, pp. 7-11, 2002.

[2] Rajsuman Rochit, “An algorithm and design to test random access memories”, Proceedings of International Symposium on Circuits and Systems, Vol.1, pp. 439-442, 10-13 May 1992.

[3] Champac V.H., Castillejos J. and Figueras J., “I_{DDQ} testing of opens in CMOS SRAMs”, Proceedings of 16th IEEE VLSI Test Symposium, pp. 106–111, 26-30 Apr 1998.

[4] D. H. Yoon, H. S. Kim and S. Kang, “Dynamic Power Supply Current Testing for Open Defects in CMOS SRAMs”, Electronics and Telemmunication Research Institute Journal, Vol. 23, No. 2, pp. 77-84, June 2001.

[5] Meixner A. and Banik J., “Weak write test mode: an SRAM cell stability design for test technique”, Proceedings of International Test Conference, pp. 309–318, 20-25 Oct 1996.

[6] Champac V.H., Avendano V.,and Linares M., “Bit line sensing strategy for testing for data retention faults in CMOS SRAMs”, Electronics Letters, Vol. 36, Issue 14, pp. 1182-1183, 6 Jul 2000.

[7] T.M. Mark, D. Bhattacharya, C. Prunty, B. Roeder, N. Ramadan, J. Ferguson and J. Yu, “Cache Ram Inductive Fault Analysis With Fab Defect Modeling”, Proceedings of International Test Conference, pp. 862 –871, 1998.

[8] K. Anami, M. Yoshimoto, H. Shinohara, Y. Hirata and T. Nakano, “Design Consideration of a Static Memory Cell”, IEEE Journal of Solid State Circuits, Vol. SC-18, No. 4, August 1983.

[9] Said Hamdioui, A. J. van de Goor, “An experimental analysis of spot defects in SRAMs: realistic fault models and tests”, Proceedings of the Ninth Asian Test Symposium, pp. 131-138, 2000.

[10] E. Seevinck, F. J. List, and J. Lohstroh, “Static-Noise Margin Analysis of MOS SRAM Cells”, IEEE Journal of Solid State Circuits, Vol. SC-22, No. 5, October 1987.

[11] M. Lee, W. I. Sze and C. M. Wu, “Static Noise Margin and Soft-Error Rate Simulations for Thin Film Transistor Cell Stability in a 4 Mbit SRAM Design”, 1995 IEEE International Symposium on Circuits and Systems, Vol. 2, pp. 937-940, 28 April-3 May 1995.

[12] Montanes R.R., de Gyvez J.P. and Volf P., “Resistance characterization for weak open defects”, IEEE Design & Test of Computers, Vol. 19 Issue 5, pp. 18 -26, Sept.-Oct. 2002.

1063-9667/04 $ 20.00 © 2004 IEEE

IEEE COMPUTER SOCIETY