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Operating conditions for a pulse-quantized AC and DC bipolar voltage source

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Operating Conditions for a Pulse-Quantized AC and DC Bipolar Voltage Source

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Abstract—We have developed an accurate ac and dc bipolar voltage source based on the quantized pulses of Josephson junctions. A factor-of-6 increase in output voltage over previous unipolar waveforms is achieved by generating bipolar waveforms where arrays of junctions are biased with both a broadband two-level digital code and a sine wave. We use simulations to determine the optimum operating conditions as a function of frequency and as a function of the phase difference between the digital code and the sinusoidal drive.

I. INTRODUCTION

In this paper we describe a method for generating accurate ac and dc bipolar voltage waveforms using pulse-quantizing Josephson junctions. The accuracy of the bipolar voltage source is based on the fact that every voltage pulse generated by a Josephson junction has a time-integrated area that is perfectly quantized. A number of circuit designs using Josephson junctions have been proposed for generating accurate ac voltage waveforms [1]-[6]. Potential applications of accurate voltage sources include: (1) generation of digitally synthesized ac signals with calculable rms voltages and high spectral purity, (2) characterization of D/A and A/D converters, and (3) calibration of dc and ac reference standards, power meters and voltmeters.

We generate bipolar voltages by driving an array of Josephson junctions with a combined input waveform consisting of both a two-level broadband digital code and a single-frequency sinusoidal drive. Combining the sine wave with the digital code input enables the direct control of individual pulses of both positive and negative polarity. Our previous pulse-driven source [4], [5] used only the digital code generator input signal and was therefore limited to single polarity pulses and unipolar voltage waveforms. Bipolar output voltages can be 6 times higher than unipolar voltages using a digital code generator with the same clock frequency. We have experimentally generated a bipolar ±18 mV, 5 kHz sine wave and demonstrated that pulse quantization reduced the quantization noise power of all in-band harmonics to 80 dB below the fundamental [1].

In this paper, simulations are used to characterize the optimum operating conditions, in particular, the output current range. We focus on the case where the sinusoidal frequency is 3/2 times the digital code clock frequency. We determine the optimum phase difference between the digital code signal and the sinusoidal drive, and we discuss issues related to the optimum junction characteristics.

II. BIPOLAR VOLTAGE GENERATION

When biased with a sinusoidal microwave signal $I_{ac}\sin(2\pi ft)$, with frequency f and amplitude I_{ac}, a Josephson junction exhibits constant voltage steps at $V_n = n\Phi_0 f$. The flux quantum $\Phi_0 = h/2e$ is the ratio of Planck's constant and twice the electron charge. These steps are shown in the junction voltage-current curve of Fig. 1. The step voltage is the time-averaged value of many junction voltage pulses. The quantum step number $n = -1$, 0, or +1 corresponds to the number and polarity of quantized voltage pulses per period $1/f$. The time integral of every pulse is precisely equal to the flux quantum. The step voltage is constant over a *current range* that depends on the sine wave amplitude and frequency. For an array of N junctions, the time-averaged dc voltage of the nth step is NV_n.

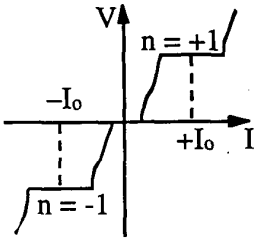

Fig. 1. Simulated voltage-current curve of a sinusoidally driven resistively shunted Josephson junction with constant voltage steps.

Bipolar pulse-quantized waveforms are generated by direct control of individual pulses of both polarities, such as those on the $+n$ and $-n$ steps. The amplitude and frequency of the sinusoidal drive are adjusted to maximize the current range ΔI_n of the $\pm n$th steps. The voltage-current curve in Fig. 1 shows the maximized current range for $n = 1$ when the drive frequency is equal to the junction's characteristic frequency $f_c = I_cR/\Phi_0$. I_c is the junction critical current and R is the junction resistance. The center of the current range of each step is selected by appropriately choosing bias currents $\pm I_o$.

In this paper we determine the current range of constant voltage steps using a simulation method which has been described previously [7], [8]. The method searches for a periodic solutions of the resistively shunted junction model. The range of dc bias currents over which a periodic solution exists determines the current range.

For the above example, where $n = 1$ and $f = f_c$, the maximum current range $\Delta I_1 = 1.02I_c$ of the $n = 1$ step occurs when the amplitude is $I_{ac} = 2.17I_c$. The bias currents of the step centers are $\pm I_o = \pm 1.07I_c$. If the bias current is set to the high $+I_o$ level for exactly one period, then a single pulse occurs with a positive voltage polarity. If the bias is set to the low $-I_o$ level, then a negative polarity voltage pulse occurs for each period. Consecutive positive and negative polarity pulses are generated by alternately switching between these two levels at each period in synchrony with the sinusoidal drive, yielding a time-averaged voltage of 0.

Time-averaged voltages between the values $+V_n$, 0 and $-V_n$ are generated by repeating periodic sequences of pulses of appropriate number and polarity. The appropriate pulse sequences are created by using a digital code that specifies the timing of the high $+I_o$ and low $-I_o$ current biases. The input and output waveforms are shown in Fig. 2 for a specific

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pattern of high (1) and low (0) biases corresponding to a 011101 bit pattern. If this six-bit pattern is continually repeated, then a net increase of two positive-polarity pulses occurs for each period of the pattern yielding a voltage of $\Phi_0 f/3$. In general, any dc voltage $(p-q)V_n/(p+q)$ can be generated using a digital code with p 1's and q 0's. The *current range* ΔI of the constant voltages steps for periodic digital codes are also found by searching for periodic solutions.

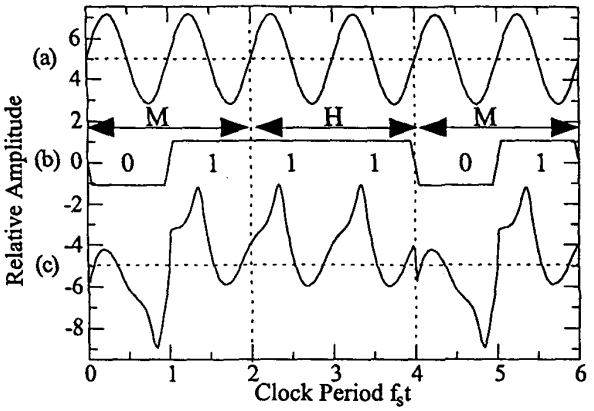

Fig. 2. Simulated input and output waveforms for an example 6 bit code. (a) Sinusoidal drive current $I_{ac}(t)/I_c$ of frequency $f = f_s$ (m = 2) [+5 offset]. (b) Digital code bias $I_o(t)/I_c$. (c) Time-dependent junction voltage $V(t)/(I_cR)$ showing quantized voltage pulses of different polarity [–5 offset].

Similarly, time-dependent periodic voltage waveforms are synthesized by repeating more complex bit patterns. The peak amplitude of these bipolar ac waveforms is V_n. Figure 3(a) shows an example of how a sine wave is generated using a two-level digital code. The sine wave peak amplitude corresponds to the highest density of 1's. The nodes correspond to an equal density of 1's and 0's.

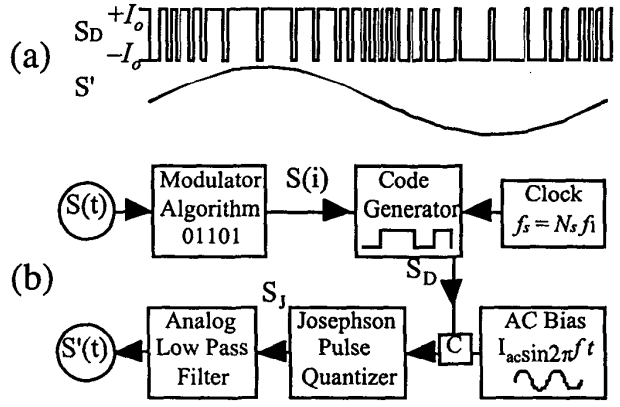

Fig. 3. (a) A two-level high-speed bias corresponding to the digital code of a synthesized sine wave S'. (b) A block diagram of the synthesized bipolar voltage source based on a Josephson junction pulse quantizer. "C" designates the directional coupler.

Figure 3(b) shows a block diagram of the method used to synthesize a sine wave of frequency f_1 or any other bipolar periodic waveform $S(t)$ using quantized pulses. The modulator algorithm is a computer program that digitizes the input waveform and creates a digital code $S(i)$ of length N_s at a sampling frequency f_s. The digital code generator re-creates this two-level code as a bipolar output voltage in real time $S_D(t)$ by clocking its memory at the sampling frequency. The two-level high-speed code is combined with a sinusoidal drive of frequency f using a directional coupler, indicated by "C". The combined signal is used to current bias the Josephson quantizer consisting of either a single junction or an array of junctions. A three-pole low-pass Butterworth filter is used to remove unwanted quantization noise from the spectrum of the quantizer output signal $S_J(t)$, leaving the desired waveform $S'(t) \approx S(t)$. Knowledge of the digital code, the drive frequency, and the number of junctions in the array is sufficient to precisely calculate the output waveform.

III. SIMULATED OPERATING CONDITIONS

Optimal generation of bipolar voltage waveforms requires specific frequency and phase relationships between the sinusoidal and sampling frequencies. The sinusoidal frequency should be at precisely half-integral multiples of the sampling frequency $f = mf_s/2$, where the integer $m \geq 2$. Figure 2 shows the junction input currents and output voltage for the m = 2 case where $f = f_s$, $f = f_c$, and the phases of the inputs are such that the transitions of the two-level digital code occur at nodes of the drive frequency. Simulations show that this is the optimum phase alignment between the two inputs. The minimum current range $\Delta I = 0.93I_c$ for all input codes occurs for the repeated 01 pattern, which corresponds to 0 output voltage. Optimization of the current range will be described below in more detail for the m = 3 case.

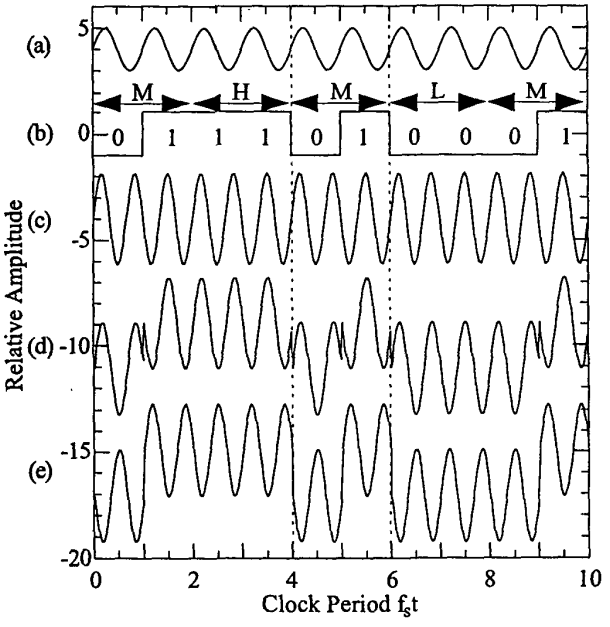

Fig. 4. Input and output waveforms for m = 3, $f = f_c$. (a) Clock signal [+4 offset]. (b) Digital code signal I_{dc}/I_c and pattern. (c) Sinusoidal drive $I_{ac}(t)/I_c$ [–4 offset]. (d) "In-phase" combined input current [–10 offset]. (e) "Out-of-phase" combined input current with sine wave phase shifted 180° [–16 offset].

There are two distinctly different transitions in Fig. 2. At the 1-to-0 transitions, $f_s t$ = 4 and 6, the digital code signal decreases, approximately canceling the rising slope of the sine wave. However, at the 0-to-1 transitions, $f_s t$ = 1 and 5,

the sine wave and the digital code are both increasing resulting in a slope much steeper than the slope of the sine wave. This steeper slope requires the junction to respond more quickly and may lead to a decrease in current range. Fortunately, we can remove all steeply sloped transitions by using a specific phase and code configuration for the $m = 3$ case.

The input waveforms for the $m = 3$ case, where the sinusoidal frequency is 3/2 times the clock frequency, are shown in Fig. 4. For this frequency, all of the steeply rising edges are removed from the input code by separating the code into three pairs of consecutive bits, Low (00), Medium (01), and High (11). Requiring the Medium level to always be 01 and never 10 breaks the symmetry of the waveform. An example code and its corresponding waveform are shown in Fig. 4(b) with the Low, Medium, and High pairs indicated. The combined input current when the code and sine wave are "in-phase" is shown in Fig. 4(d). Note that there are no steep transitions. However, if the sine wave is phase shifted by 180°, that is, the "out-of-phase" case, then all of the transitions are steeply sloped as shown in 4(e). Note that the junction is pulsing twice as often for the 01 pattern in the out-of-phase case than the in-phase case.

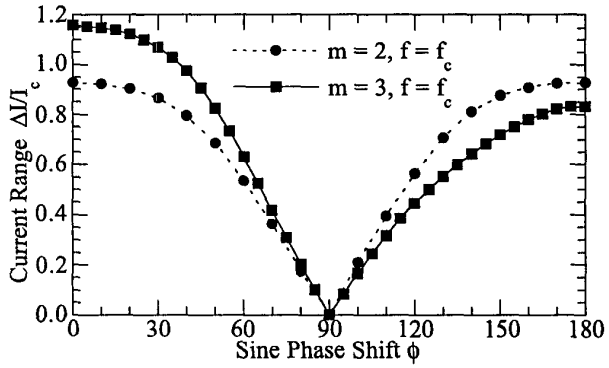

Fig. 5. Current range $\Delta I/I_c$ vs. sine wave phase shift ϕ relative to the digital code signal for $m = 2$ and $m = 3$, $f = f_c$, $n = 1$, $I_{ac} = 2.17I_c$, $\pm I_o = \pm 1.07\ I_c$, and the periodic 01 pattern.

Figure 5 shows how the current range for the periodic 01 pattern varies as the sine wave shifts in phase ϕ relative to the digital code. Both the $m = 2$ and 3 cases are shown. The sine frequency is equal to the characteristic frequency ($f = f_c$) and biases are set for $n = 1$ operation. Both cases show that the current range decreases to 0 when the sine wave is shifted by 90°. However, the current range is symmetric about 90° for the $m = 2$ case but not for $m = 3$. The in-phase ($\phi = 0$) $m = 3$ case has a 25% larger current range ($\Delta I = 1.16I_c$) for the 01 pattern than the $m = 2$ case ($\Delta I = 0.93I_c$), but the out-of-phase case ($\phi = 180$) is 11% lower ($\Delta I = 0.83I_c$). This suggests that, at least for the 01 pattern, steeply sloped transitions decrease the current range of the device.

Next, we investigate the current range at four different voltages for both in-phase and out-of-phase codes. Figure 6 shows the current range vs. voltage for nine digital codes where $m = 3$, $f = f_c$, and $n = 1$. Note that shifting the pattern by one bit is equivalent to a 180° phase shift, which corresponds to an out-of phase input waveform. The in-phase $m = 3$ case has a larger maximum current range for all bit patterns ($\Delta I_{max} = 1.02I_c$) than both the out-of-phase $m = 3$ case ($\Delta I_{max} = 0.83I_c$) and the $m = 2$ case ($\Delta I_{max} = 0.93I_c$). The in-phase $m = 3$ case is therefore the optimum mode of operation for the bipolar source, and the all 1's (111111) pattern determines the maximum operating current range, which corresonds to the $n = 1$ step width.

IV. PRACTICAL IMPLEMENTATION

Sinusoidal drive frequencies much higher than the clock frequency ($m > 3$) are possible, but it is likely that they will also have maximum current ranges where the relative phase and code are chosen to minimize the number of steep transitions. Realistically, however, the code generator's physical rise time limits the maximum sinusoidal drive frequency so that $m \leq 3$ will be the typical operating condition. Note that our simulations do not take finite rise times of the digital code transitions into account. Experimental current ranges using a real digital code generator with finite rise time will probably be lower than those determined here.

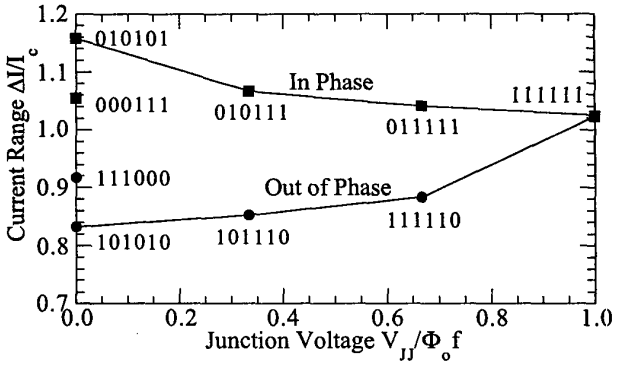

Fig. 6. Current range $\Delta I/I_c$ vs. junction voltage $V_{JJ}/(\Phi_o f)$ for $f = f_c$, $n = 1$. Nine example bit codes are shown for both in-phase and out-of-phase input waveforms.

The generation of bipolar waveforms is different from the generation of unipolar waveforms [5]. Unipolar waveform generation does not use an additional sinusoidal drive, so the digital code generator creates pulses of a single polarity with a code that returns to 0 every other bit. The maximum peak-to-peak unipolar voltage is thus limited to $n\Phi_o f_s/2$. For bipolar waveforms, the pulse polarity and digital code do not have these limitations yielding a maximum peak-to-peak voltage of $mnf_s\Phi_o$. Thus, for a code generator with a fixed maximum clock frequency, bipolar voltages can be $2m$ times larger than unipolar voltages.

The final parameters to be determined are the junction critical current and characteristic frequency. Many issues are involved in determining these values, including junction technology and uniformity, on-chip power dissipation, power uniformity to junctions distributed along a transmission line, system current noise, and current loading of the system when used as a voltage source. As shown above, the maximum current range for all patterns $\Delta I_{max}/I_c$ for the $n = 1$, $m = 3$ case is equivalent to the maximum current range for the $n = 1$ constant voltage step of a sinusoidally driven junction. This maximum current range and corresponding bias conditions (I_o and I_{ac}) are plotted in Fig. 7 as a function of the normalized sinusoidal frequency $\Omega = f/f_c$. For sinusoidal frequencies

greater than the characteristic frequency, the maximum current range remains on the order of the critical current ($\Delta I \approx I_c$), while the bias currents increase in proportion with the frequency ($I_o \approx I_c\Omega$ and $I_{ac} \approx 2I_c\Omega$).

The above analysis shows that significantly more total ac and dc input power ($I_o^2 + I_{ac}^2/2$)R is required to operate at higher frequencies. For example, 5.2 dB more power is required to operate at $\Omega = 2$ than at $\Omega = 1$ for only a 10% increase in current range, assuming the junctions have the same parameters. Secondly, Kautz [9] concluded that nonhysteretic junctions have maximum stability against noise-induced phase slippage when the sinusoidal frequency is in the range Ω = 1-3. Finally, Borovitskii et al. [10] have shown that the greatest tolerance of step position to critical current variation in arrays is obtained for $\Omega = 1$. This is also apparent from the frequency dependence of the bias conditions. Thus for optimum power, uniformity, and stability, the characteristic frequency should be approximately equal to the sinusoidal frequency.

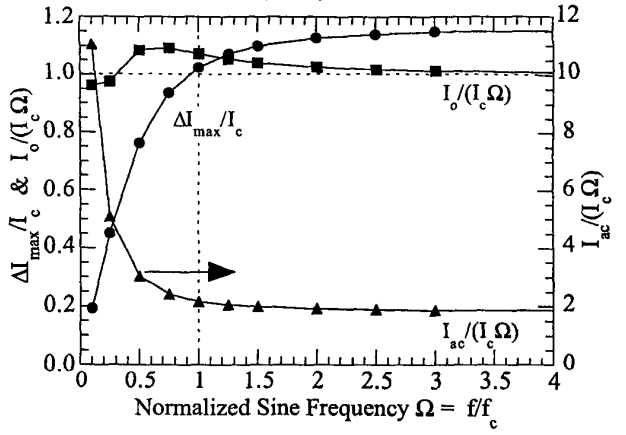

Fig. 7. Maximum output current range $\Delta I_{max}/I_c$, digital code bias current $I_o/(I_c\Omega)$, and total ac and dc input power as functions of sine frequency $\Omega = f/f_c$. $n = 1$ and $m = 3$.

With the characteristic frequency fixed, we can now choose the critical current. Since the maximum current range is proportional to the critical current, I_c should be as large as possible for the lowest sensitivity to system noise and the largest possible load current. I_c can be constrained by either on-chip heating from input power dissipation or by the ±20 mA maximum bias currents that can be supplied to a 50 Ω transmission line by the broadband code generator. The amplitude of the sinusoidal drive is usually not a limitation, since it is relatively easy to amplify a single-frequency sinusoidal signal as opposed to the broad band signal of a digital code generator. Finally, the Josephson penetration length λ_J can limit the maximum junction critical current and the associated maximum current range. Kautz [11] has shown that the maximum critical current for a square junction of area $(4\lambda_J)^2$ is about 10 mA. Large uniform arrays of Nb-PdAu-Nb junctions with critical currents up to 10 mA have been fabricated for programmable voltage standard applications [3], [12].

The following procedure can be used to experimentally optimize the bias conditions for the bipolar voltage standard source operating at a maximum output voltage V_1 ($n = 1$): (1) Find the fastest digital code generator available (e.g. f_s = 12 GHz). (2) Fabricate junctions with $f_c = 1.5f_s$. (3) Set the sinusoidal frequency $f = 1.5f_s$. (4) Adjust I_{ac} to maximize the $n = 1$ step voltage. (5) Using an all 1's code, adjust $+I_o$ so that the current range of the $n = 1$ step is centered on the zero current axis. (6) Using an all 0's code, adjust $-I_o$ so that the $n = -1$ step is centered on the zero current axis. (7) Find in-phase operation using the periodic 01 pattern by adjusting the relative phase between the code generator and the sinusoidal source until the current range of the 0 V step is maximized. Be aware that the current range should be 0 at $\phi = 90°$ and a lower relative maximum should occur at $\phi = 180°$.

IV. CONCLUSIONS

We determined the optimum operating conditions for the bipolar voltage standard source. Through simulations we found the relative frequencies and phases between the digital code signal and the sinusoidal drive that yield the maximum operating current range. We provided a recipe for experimentally optimizing the bias conditions. We also determined the optimum bias current amplitudes for these conditions. Finally, we discussed relevant criteria for choosing the optimum junction parameters for bipolar operation.

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