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Operation and control of a dynamic voltage restorer using transformer coupled H-bridge converters — Source link

Bingsen Wang, Mahesh S. Illindala

Institutions: University of Wisconsin-Madison

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Topics: Voltage regulation, Voltage regulator, H bridge, Power electronics and Transformer

Operation and Control of a Dynamic Voltage Restorer Using Transformer Coupled H-Bridge Converters

Bingsen Wang, *Student Member, IEEE*, Giri Venkataramanan, *Member, IEEE*, and Mahesh Illindala, *Member, IEEE*

***Abstract*—The dynamic voltage restorer (DVR) as a means of series compensation for mitigating the effect of voltage sags has become established as a preferred approach for improving power quality at sensitive load locations. Meanwhile, the cascaded multilevel type of power converter topology has also become a workhorse topology in high power applications. This paper presents the detailed design of a closed loop regulator to maintain the load voltage within acceptable levels in a DVR using transformer coupled H-bridge converters. The paper presents system operation and controller design approaches, verified using computer simulations, and a laboratory scale experimental prototype.**

***Index Terms*—Dynamic voltage restorer (DVR), H-bridge converter, voltage sags.**

I. Introduction

With the rapid technology advancement in industrial control processes, electric utilities are experiencing more demanding requirements on the power quality from the large industrial power consumers. Such power quality problems have been better appreciated when the price paid due to the economic losses caused by them is large. These concerns are reflected in the newer versions of power quality standards, such as IEEE 1159-1995 [1] and IEC61000-4-30 [2]. Trends of deregulation happening in Europe and America exert pressures on the utilities to accommodate such demanding requirements in a competitive electricity market environment.

Among the various power quality problems, the voltage sag, usually resulting from the faults on parallel transmission/distribution feeders, is attracting quite a large amount of attention of researchers from both industry and academia [3]–[5]. A definitive solution to this problem at large power levels has been commonly called dynamic voltage restorer (DVR), under the rubric of the custom power concept introduced by EPRI [6]. The main function of DVR is to mitigate the voltage sag, although sometimes, additional functions such as harmonics compensation and reactive power compensation are also integrated to the device. It has also been shown in a previous study that the series compensation device such as the DVR as shown in Fig. 1(a) is preferred over shunt compensation strategy as shown in Fig. 1(b) for stiff systems [7], typical of large industrial load installations.

Much of the published literature on DVRs deals with a voltage source converter (VSC) realized using two-level converters, which are well suited for 480-V systems [8], [9]. While in high power applications such as at distribution voltage levels, a multilevel converter is a more attractive solution, whose application in a DVR has not been well addressed. On the other hand, for the control of DVR, the open loop feed-forward technique is found to be a common practice, which generally results in poor damping of the output harmonic filter [10]. In this paper, the power circuit design and controller design considerations of an ac stacked multilevel converter using cascaded H-bridges is studied for DVR application. The paper is organized as follows. The power architecture is introduced in Section II followed by the modulation strategy presented in Section III. The modeling and controller design are detailed in Section IV. The complex sequence filter for isolating negative and positive sequence quantities is explained in Section V. The simulation and experimental results are presented in Section VI followed by a summary presented in the concluding section.

II. Power Architecture

Although various topologies may be used to realize the VSC illustrated in Fig. 1, at higher power levels cascaded H-bridge multilevel power converters are seen to have advantages in several aspects [11], [12]. First, multilevel converters can realize the higher power and high voltage using semiconductor switches of relative small ratings while avoiding the voltage sharing and current sharing problems associated with series and parallel connection of switches commonly employed in two-level converter realization. Second, multilevel converters can synthesize the output voltage with smaller steps and reduced harmonic content, while potentially resulting in smaller dv/dt thus lower electromagnetic interference (EMI). Third, compared with diode clamped multilevel topology, the H-bridge cascaded structure can avoid unequal device rating and unbalanced dc link voltage problems. Compared to flying-capacitor topology, the H-bridge cascaded multilevel converter has less storage capacitors and requires simpler control [13]. Finally, it is worth noting that the modularity nature of the H-bridge cascaded multilevel converter makes an easier realization.

The proposed power architecture of the transformer coupled H-bridge converter is illustrated in Fig. 2. Each phase is composed of three H-bridge inverters. The ac outputs of the converters are connected in series through transformers. This architecture fits squarely with the DVR application, which necessarily involves a series injection of the compensating

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B. Wang and G. Venkataramanan are with the Department of Electrical and Computer Engineering, University of Wisconsin, Madison, WI 53706 USA (e-mail: bingsen@cae.wisc.edu).

M. Illindala is with the Technology and Solutions Division, Caterpillar, Inc., Peoria, IL 61602 USA.

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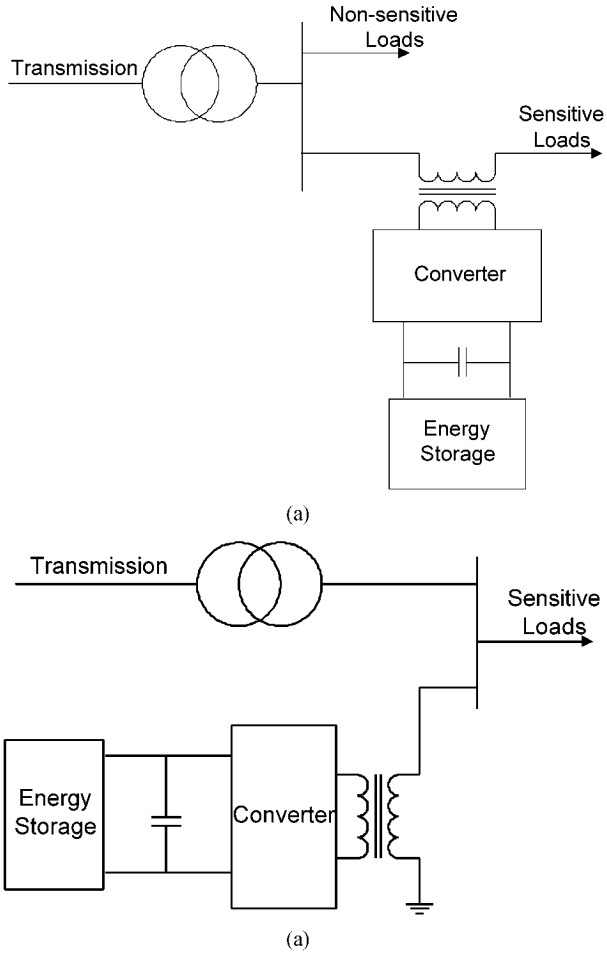

Fig. 1. Interconnection schematic of (a) series and (b) shunt compensation configurations for power quality improvement.

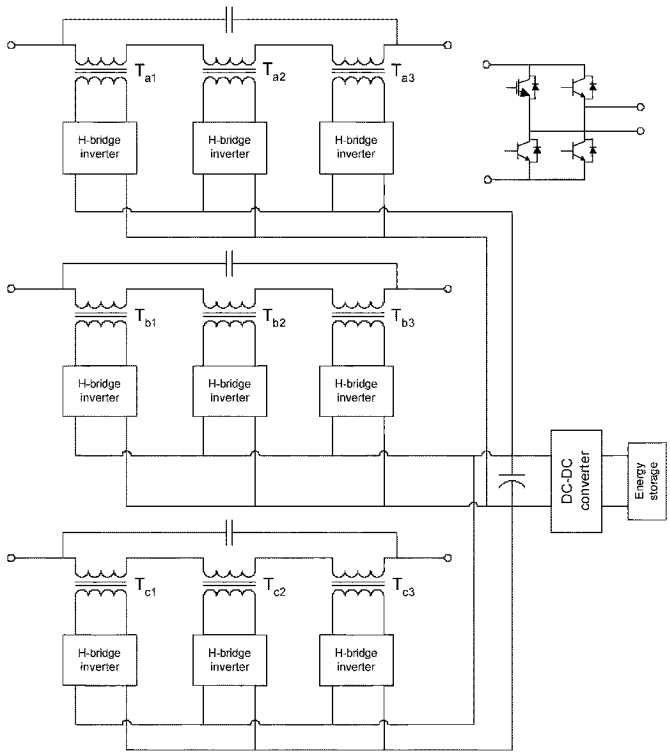

Fig. 2. Proposed power architecture of the transformer coupled H-bridge converter applied to DVR.

voltage source. Use of the transformers here allows for voltage matching, isolation, series injection and multilevel waveform synthesis simultaneously. Furthermore, instead of using isolated dc link for each H-bridge inverter, a common dc link bus connects all the nine H-bridge inverter dc ports in parallel. This is different from the conventional H-bridge cascaded multilevel converter [13]. This is also different from the multipulse converter which includes multiple six-pulse three-phase converters [14]. Compared to the transformerless realization of the DVR with the conventional H-bridge cascaded multilevel converter [15]–[17], the common dc bus (CDCB) structure significantly simplifies the energy management on the dc side while retaining all the other good features of the multilevel converter, such as high quality waveforms, low EMI, and evenly load-sharing among semiconductor switches, etc.

Furthermore, CDCB structure reduces the low frequency dc link ripple current due to the phase shift between the three phases and high frequency ripple currents resulting from switching harmonics cancelled due to the carrier phase shift. The three transformers in each phase could be one transformer with three secondary windings, which is a preferred approach since the switching harmonics cancellation will reduce the core loss. However, to keep the modularity of the design, a separate injection transformer is used for each H-bridge.

As seen in Fig. 2, the primary side of the injection transformer carries the rated load current. The voltage rating of the transformer depends on the grid voltage level and the depth of voltage sag required to compensate. So the rated current multiplied by the injection voltage level gives the VA rating of each phase. The phase VA rating divided by the number of series connected module is the rating for one module. The number of series connected modules is an additional degree of freedom that may be chosen to fulfill other requirements. The turns ratio of the transformer is determined by the available voltage and current rating of semiconductor switches for a given VA rating. The filter capacitor can be sized based on the leakage inductance of the transformer such that the cut off frequency the LC filter is about a decade below the switching frequency.

Depending on the load condition, mainly the power factor, two different compensation strategies may be applied, zero active power compensation (ZAP) and minimum active power compensation (MAP) [7]. Under ZAP condition, the converter injects purely reactive component of voltage to maintain regulation. When the load and line conditions preclude ZAP operation, the MAP strategy is invoked. Under MAP condition, the dc link voltage will be controlled by drawing energy from the storage. The two different compensation strategies can be realized by varying the relative phase angle between the grid voltage space vector and injection voltage space vector. For resistive load, the only choice is MAP, which results in injected voltage exactly in phase with grid positive sequence voltage. Under this operating condition, the rating of the energy storage is based on the VA rating and duration of the sag for a unity power factor load.

III. Modulation Strategy

Stair-case modulation (SCM) is commonly used for cascaded H-bridge converters [18]. For SCM, the switching instants of each module are calculated offline to attenuate certain harmonics. In that case, we have to vary the dc link voltage in order to achieve variable ac output voltage. Variable dc link voltage generally results in slow dynamic response due to the bulk dc link capacitor. For the DVR application, fast dynamic response is critical because the voltage sag duration typically ranges from half cycle to 30 cycles. Based on this consideration, carrier phase-shifted PWM modulation scheme is adopted so that we can maintain a relatively constant dc link voltage while achieving the fast dynamic response required of the output voltage by varying modulation index.

By shifting the carrier signal for each module in the same phase by 120°, the harmonics on the ac side of each H-bridge in that phase cancel each other resulting in the effective switching frequency for one phase leg three times higher than that of each module. The frequency scaling effect provides opportunity for reducing passive filter requirement. The experimental steady-state output voltage waveforms in one phase are shown in Fig. 3(a) using such a modulation strategy. It may be observed that although the waveform from each H-bridge looks almost identical to each other, their summation approaches the sinusoidal waveform more closely. Vanishing low order harmonics in the phase voltage spectra as shown in Fig. 3(b) exemplifies the frequency scaling effect of the carrier phase-shifted modulation scheme. The similarity among spectra of H-bridge output voltages in each phase makes it easy to practice modular design. The further details about the implementation will be discussed in Section VI.

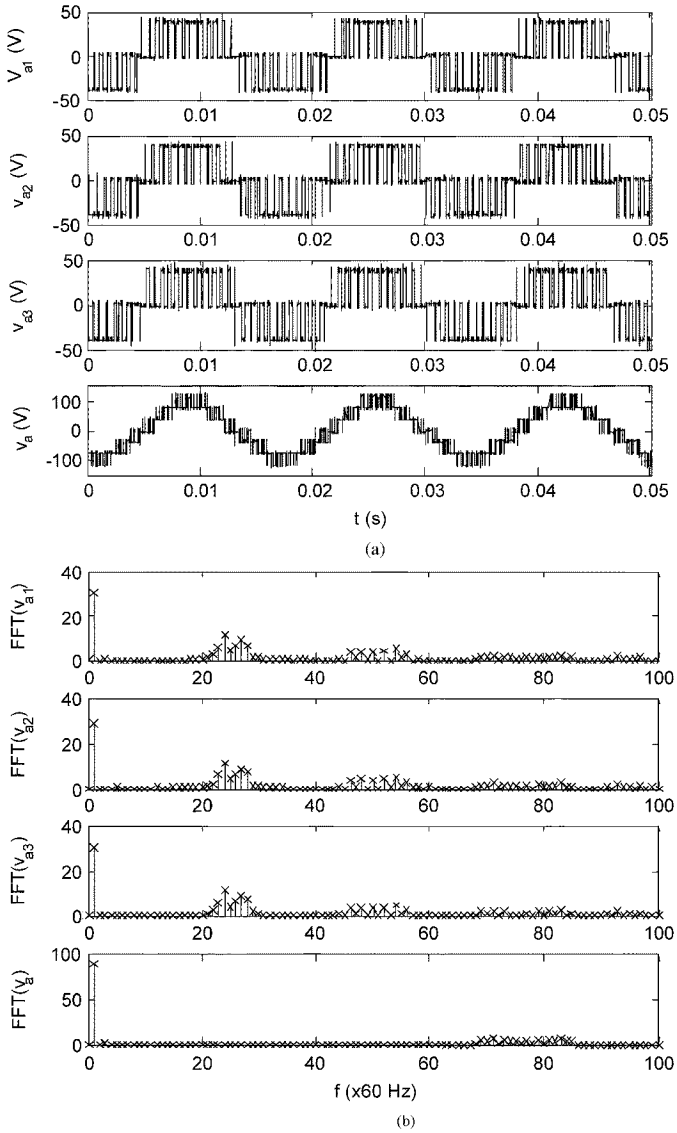

Fig. 3. Experimental measurement of the steady-state PWM output waveforms of modules in one phase, and their Fourier spectra. (a) Steady-state output voltages with phase-shifted modulation method. The top three traces are output voltages from each H-bridge in one phase. The last trace is summation of three H-bridge outputs. (b) Spectra of output voltage of each H-bridge module and the phase voltage.

IV. System Modeling and Controller Design

The overall system control structure is shown in Fig. 4. In this control scheme, the three-phase power grid side voltages (a,b,c) are sensed and transformed to an orthogonal equivalent two-phase system (α, β) in the stationary reference frame. Then the positive sequence and the negative sequence voltages are isolated from each other using a complex coefficient filter, whose operation will be explained further in a subsequent section. In the positively (counter clockwise) rotating synchronous reference frame (PRSRF), positive sequence grid voltage vector is compared against the positive sequence load voltage command vector. The difference between them becomes the desired injected positive sequence voltage vector across the filter capacitor, which represents the missing voltage during the interval of voltage sag. To counter unbalanced voltages commonly accompanying voltage sag events, in the negatively rotating synchronous reference frame (NRSRF), the negative sequence grid voltage vector is compared against the negative sequence load voltage command vector, which is often the null vector, producing the command of injected negative sequence voltage vector. This injected voltage may be considered the extraneous and undesirable additional voltage that needs to be nullified during the interval of voltage sag.

Thus, the controller generates the correct voltage references to the modulator integrating the missing positive sequence component and extraneous negative sequence component. From the command voltage, the gating signals for the nine H-bridges may be generated. However, since the converter output voltage is interfaced to the load and line through the injection transformer and the capacitive filter, effect at the power frequency due to positive and negative sequence disturbances needs to be compensated. For this purpose, a closed loop controller that incorporates appropriate decoupling elements is employed as described further.

The single-line diagram of the power circuit is shown in Fig. 5, where the injection transformer is modeled as the leakage inductance $\mathrm{L_f}$ and series resistance R_f. The injection voltage V_inj is the output voltage of H-bridges reflected to the

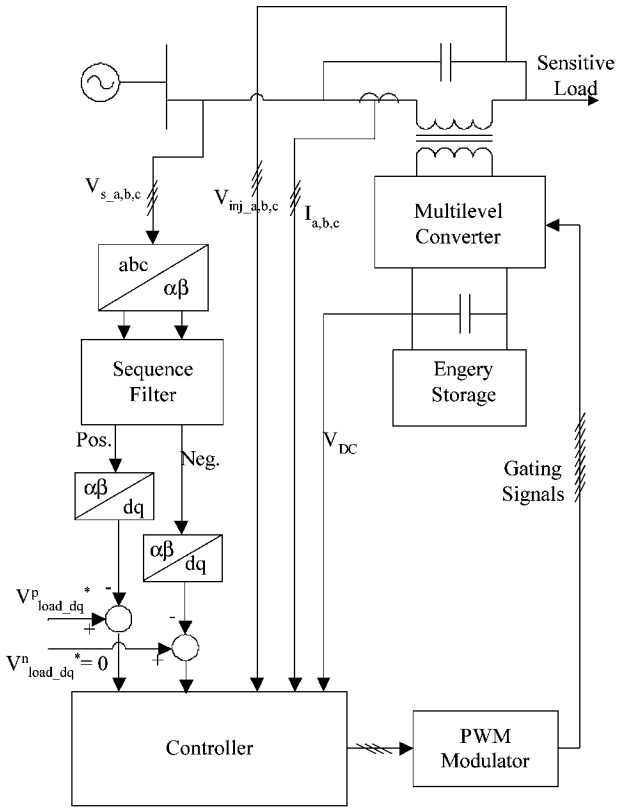

Fig. 4. Block diagram of the overall system structure illustrating controller.

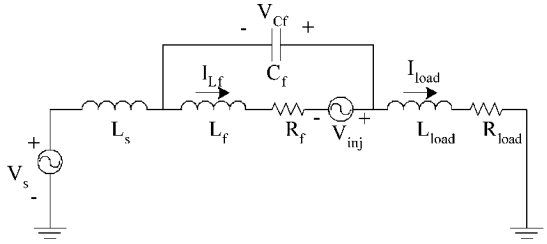

Fig. 5. Single-line diagram of the power circuit of the DVR system.

primary side of the injection transformer. The state equations associated with $\mathrm{L_f}$ and $\mathrm{C_f}$ can be written as

$$\begin{aligned}\frac{di_{\mathrm{Lf\_x}}}{\mathrm{dt}} &= \frac{1}{\mathrm{L_f}}[V_{\mathrm{inj\_x}} - V_{\mathrm{Cf\_x}} - R_{\mathrm{f}} i_{\mathrm{Lf\_x}}] \\ \frac{dv_{\mathrm{Cf\_x}}}{\mathrm{dt}} &= \frac{1}{\mathrm{C_f}}[i_{\mathrm{Lf\_x}} - i_{\mathrm{load\_x}}]\end{aligned} \tag{1}$$

where $\mathrm{x} \in \{\mathrm{a}, \mathrm{b}, \mathrm{c}\}$.

In the stationary orthogonal α-β reference frame, the state equations become

$$\begin{aligned}\frac{di_{\mathrm{Lf}\_\alpha\beta}}{\mathrm{dt}} &= \frac{1}{\mathrm{L_f}}[V_{\mathrm{inj}\_\alpha\beta} - V_{\mathrm{Cf}\_\alpha\beta} - R_{\mathrm{f}} i_{\mathrm{Lf}\_\alpha\beta}] \\ \frac{dv_{\mathrm{Cf}\_\alpha\beta}}{\mathrm{dt}} &= \frac{1}{\mathrm{C_f}}[i_{\mathrm{Lf}\_\alpha\beta} - i_{\mathrm{load}\_\alpha\beta}]\end{aligned} \tag{2}$$

where $y_{\alpha\beta} = (2/3)(y_{\mathrm{a}} + y_{\mathrm{b}} e^{-\mathrm{j}2\pi/3} + y_{\mathrm{c}} e^{-j2\pi/3})$, $y \in \{i_{\mathrm{Lf}}, V_{\mathrm{Cf}}, V_{\mathrm{inj}}, i_{\mathrm{load}}\}, \mathrm{j} = \sqrt{-1}$.

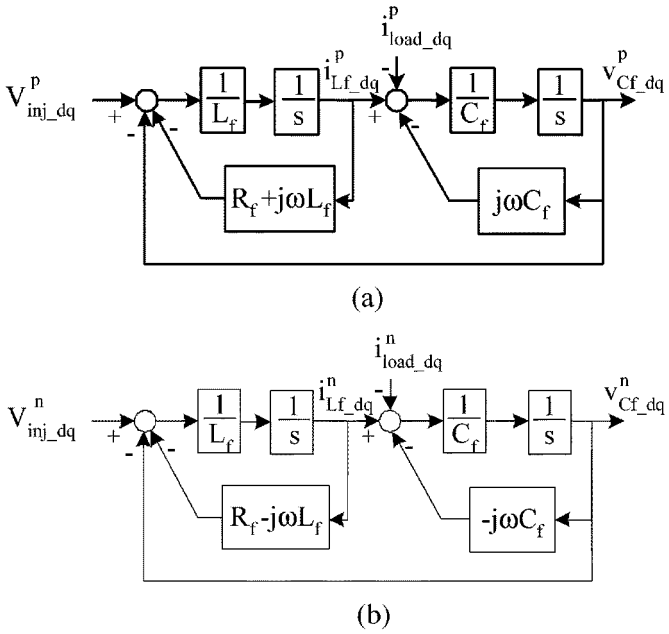

Fig. 6. Complex form of state block diagrams of the plant in PRSRF and NRSRF: (a) plant model in PRSRF and (b) plant model in NRSRF.

In the PRSRF and NRSRF, the dynamic equations can be expressed in complex form as (3) and (4), respectively

$$\begin{aligned}\frac{di^{\mathrm{p}}_{\mathrm{Lf\_qd}}}{\mathrm{dt}} &= \frac{1}{\mathrm{L_f}}\left[v^{\mathrm{p}}_{\mathrm{inj\_qd}} - v^{\mathrm{p}}_{\mathrm{Cf\_qd}} - R_{\mathrm{f}} i^{\mathrm{p}}_{\mathrm{Lf\_qd}}\right] - \mathrm{j}\omega i^{\mathrm{p}}_{\mathrm{Lf\_qd}} \\ \frac{dv^{\mathrm{p}}_{\mathrm{Cf\_qd}}}{\mathrm{dt}} &= \frac{1}{\mathrm{C_f}}\left[i^{\mathrm{p}}_{\mathrm{Lf\_qd}} - i^{\mathrm{p}}_{\mathrm{load\_qd}}\right] - \mathrm{j}\omega v^{\mathrm{p}}_{\mathrm{cf\_qd}}\end{aligned} \tag{3}$$

$$\begin{aligned}\frac{di^{\mathrm{n}}_{\mathrm{Lt\_qd}}}{\mathrm{dt}} &= \frac{1}{\mathrm{L_f}}\left[v^{\mathrm{n}}_{\mathrm{inj\_qd}} - v^{\mathrm{n}}_{\mathrm{Cf\_qd}} - R_{\mathrm{f}} i^{\mathrm{n}}_{\mathrm{Lf\_qd}}\right] + \mathrm{j}\omega i^{\mathrm{n}}_{\mathrm{Lf\_qd}} \\ \frac{dv^{\mathrm{n}}_{\mathrm{Cf\_qd}}}{\mathrm{dt}} &= \frac{1}{\mathrm{C_f}}\left[i^{\mathrm{n}}_{\mathrm{Lf\_qd}} - i^{\mathrm{n}}_{\mathrm{load\_qd}}\right] + \mathrm{j}\omega v^{\mathrm{n}}_{\mathrm{Cf\_qd}}\end{aligned} \tag{4}$$

where $y^{\mathrm{p}}_{\mathrm{\_qd}} = y_{\mathrm{\_}\alpha\beta} e^{-\mathrm{j}\omega t}$, $y^{\mathrm{n}}_{\mathrm{\_qd}} = y_{\mathrm{\_}\alpha\beta} e^{\mathrm{j}\omega t}$, $y \in \{i_{\mathrm{Lf}}, V_{\mathrm{Cf}}, V_{\mathrm{inj}}, i_{\mathrm{load}}\}$.

The block diagrams for (3) and (4) are shown in Fig. 6. Alternatively, the state equation can also be written in scalar form by taking real part and imaginary part of (3) and (4) or by taking the magnitude and argument of (3) and (4), respectively [19].

As may be observed from Fig. 6, in the phasor domain d–q synchronously rotating reference frames, the$R_{\mathrm{f}} \pm j\omega \mathrm{L_f}$ and $\pm j\omega \mathrm{C_f}$, terms appearing as complex state feedback are the result of the cross-coupling between the d-axis and q-axis states. It is desirable to decouple the d-axis state and q-axis state interactions so that they can be controlled independently; or equivalently in polar coordinate frame, both the injected voltage amplitude and phase angle can be controlled with desired dynamic performance.

The structure of the controllers in PRSRF and NRSRF are illustrated in Fig. 7(a) and (b), respectively. The controller employs a classic inner current loop/outer voltage loop structure. The inner current regulator, with a proportional regulator R_{a} is designed to yield necessary bandwidth of the inner current loop. In this design, the bandwidth of the inner loop is chosen to be 1 kHz. The outer voltage regulator is a classical PI regulator$K_{\mathrm{p}} + K_{\mathrm{i}}/\mathrm{s}$, which generates the current command for the

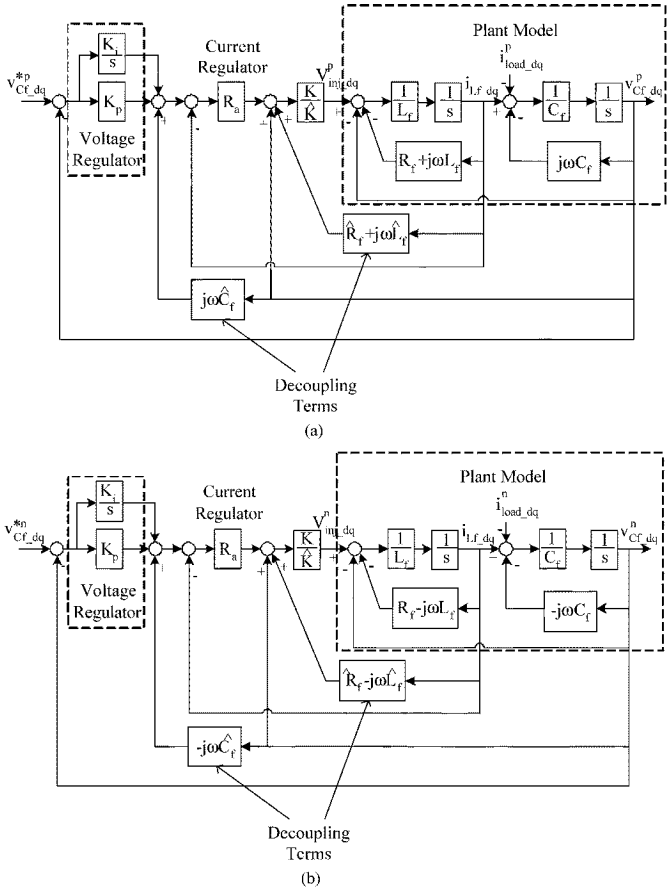

Fig. 7. Block diagram of the complex state feedback controller in PRSRF and NRSRF. (a) Controller in PRSRF. (b) Controller in NRSRF.

inner current loop. K_{p} and K_{i} are chosen to shape the loop gain of the outer loop, yielding zero steady state error and acceptable bandwidth, while maintaining an adequate stability margin.

In addition to the inner current loop gain and the outer voltage loop PI coefficients, the regulator also incorporates decoupling terms that are used to compensate for the coupling that is present between the d and q axis quantities. They introduce correction terms that compensate for the voltage across the transformer series impedance by measuring the transformer current and for the current through the filter capacitor by measuring the injected capacitor voltage.

With the plant and controller parameters listed in Table I, (the controller parameters are purposely detuned to illustrate the robustness features) the inner current loop has bandwidth about 1 kHz and the outer voltage loop has 100-Hz bandwidth, indicating a settling time of about 10 ms, corresponding to about half cycle of the period of the ac waveform. The value of C_{f} is chosen such that the LC cutoff frequency is about 250 Hz. The loop gain transfer function of the outer voltage loop in PRSRF is plotted in Fig. 8. Almost identical frequency response of the voltage loop gain in NRSRF is achieved with the same parameters and it is not plotted here for the sake of brevity. The magnitude of the incremental output impedance is plotted in Fig. 9(a), which is zero at 0 Hz in the synchronous reference frame, corresponding to 60 Hz in the stationary reference frame. Similarly, the load voltage response to line voltage disturbance [Fig. 9(b)] is null at 0 Hz. Thus, the controller has excellent load regulation and line regulation capabilities.

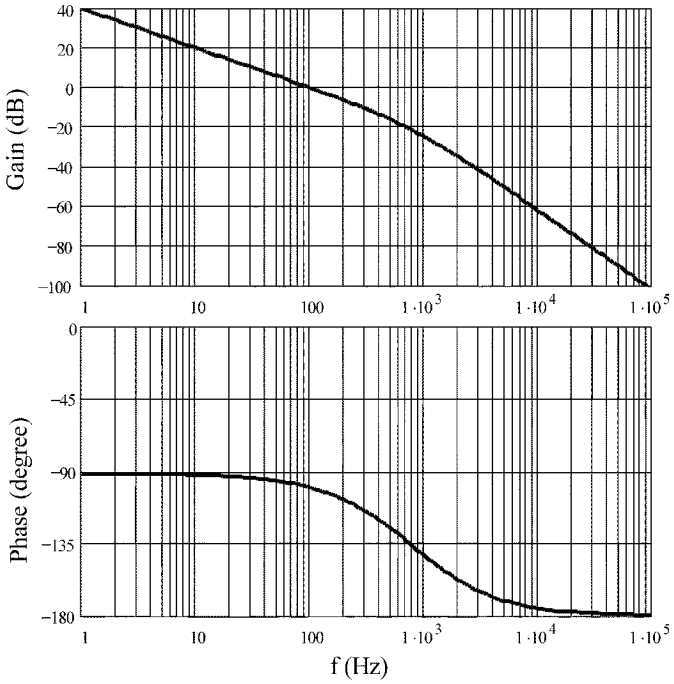

Fig. 8. Bode plot of the loop gain of outer voltage loop.

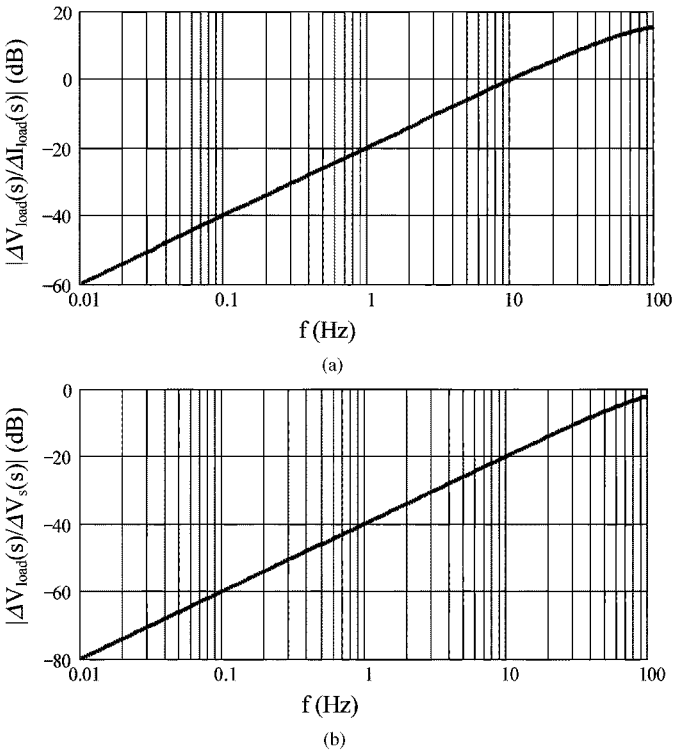

Fig. 9. Plot of the frequency response of incremental output impedance magnitude and line regulation characteristics. (a) Incremental output impedance. (b) Load voltage response to line voltage disturbance.

V. Complex Sequence Filter

To generate the injection voltage command, positive sequence and negative sequence components in the sensed grid

TABLE I
PARAMETERS OF PLANT AND CONTROLLER

C_f (μF)	50	$\hat{C}_f$ (μF)	45
R_f (Ω)	0.96	$\hat{R}_f$ (Ω)	0.86
L_f (mH)	8.23	$\hat{L}_f$ (mH)	7.4
K_p (Ω^{-1})	0.03	R_a (Ω)	47
K_i ($\Omega^{-1}s^{-1}$)	60		

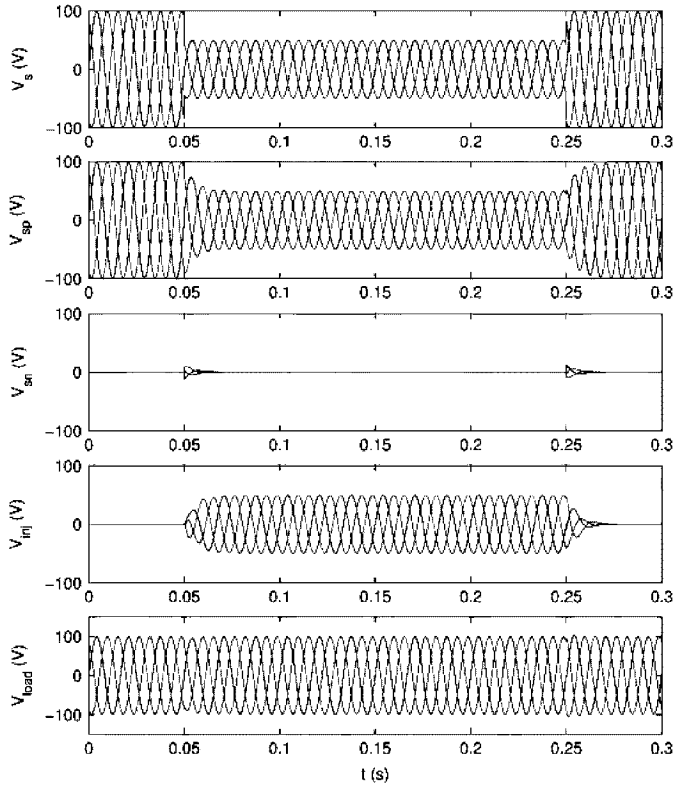

Fig. 10. Simulation results for balanced sag. From top to bottom traces are grid voltage, positive sequence of grid voltage, negative sequence of grid voltage, injected voltage, and load voltage.

voltage are separated using a complex filter. For completeness, the complex filter developed in [20], [21] is explained here.

A low pass filter with bandwidth of $f_{\rm bw}$ having the transfer function of (5) can pass "real" signal whose frequency spectrum centering at 0 Hz within the bandwidth

$$G_{\rm lpf}({\rm s}) = \frac{1}{1+\frac{\rm s}{2\pi f_{\rm bw}}}. \tag{5}$$

While a complex filter of bandwidth $f_{\rm bw}$ having the transfer function of (6) can pass complex signal whose spectrum centering at $f_{\rm o}$ within the bandwidth of $f_{\rm bw}$

$$G_{\rm lpf}({\rm s}) = \frac{1}{1+\frac{{\rm s}-{\rm j}2\pi f_{\rm o}}{2\pi f_{\rm bw}}}. \tag{6}$$

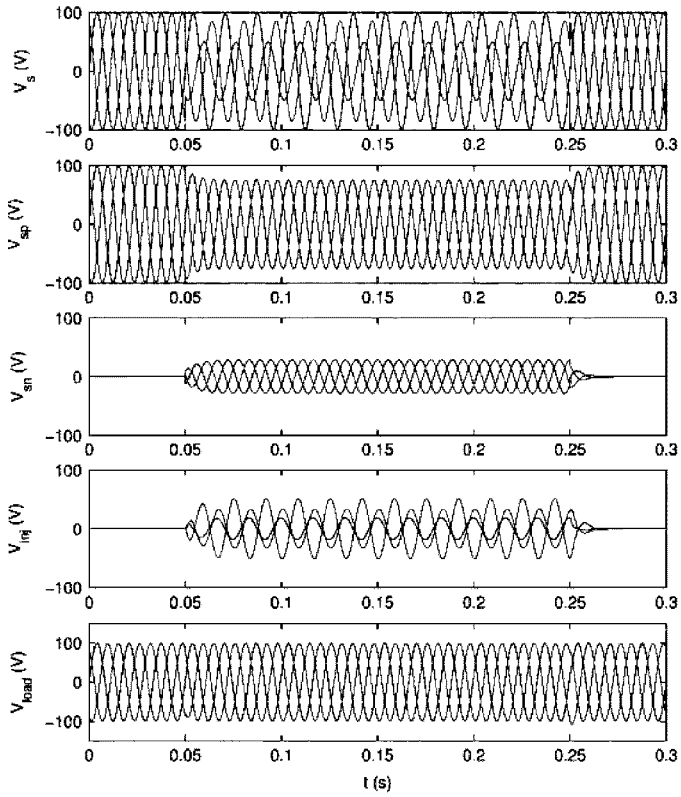

Fig. 11. Simulation results for unbalanced sag. From top to bottom traces are grid voltage, positive sequence of grid voltage, negative sequence of grid voltage, injected voltage, and load voltage.

The complex filter proposed in [22] with transfer function of (7) can both pass the positive sequence space vector (which is a complex signal) and reject the negative sequence space vector

$$G_{\rm PSF}(s) = \frac{1}{1+\left(\frac{2{\rm j}\omega_{60}(s-{\rm j}\,\omega_{60})}{K_I(s+{\rm j}\,\omega_{60})}\right)} \tag{7}$$

where $\omega_{60} = 2\pi 60$.

VI. SIMULATION AND EXPERIMENTAL RESULTS

In order to verify the proposed control scheme, the detailed numerical simulation has been carried out using Matlab-Simulink. The simulation results for the balanced case and unbalanced voltage sags are shown in Figs. 10 and 11. For both cases, three phase balanced resistive load is used. The sag duration is twelve 60-Hz cycles. During unbalanced sag, $V_{\rm a} = 1.0, {\rm V_b} = 0.5e^{-{\rm j}2\pi/3}, {\rm V_c} = 0.866e^{{\rm j}5\pi/6}$ all in p.u.

The controller in the experimental setup is realized using a digital control platform built from a floating-point digital signal processor (DSP) TMS320C31 along with a Xilinx field programmable gate array (FPGA) XCS40. The DSP acquires the sensed inputs and computes the control algorithm, while the input/output interfacing functions are managed through the FPGA. The carrier shifted PWM modulator is implemented in FPGA. As shown in Fig. 12, three carrier waveforms phase shifted by 120° are generated using 16-b counters. For each phase, there is one reference signal compared against three carries to produce the switching events for three modules in that

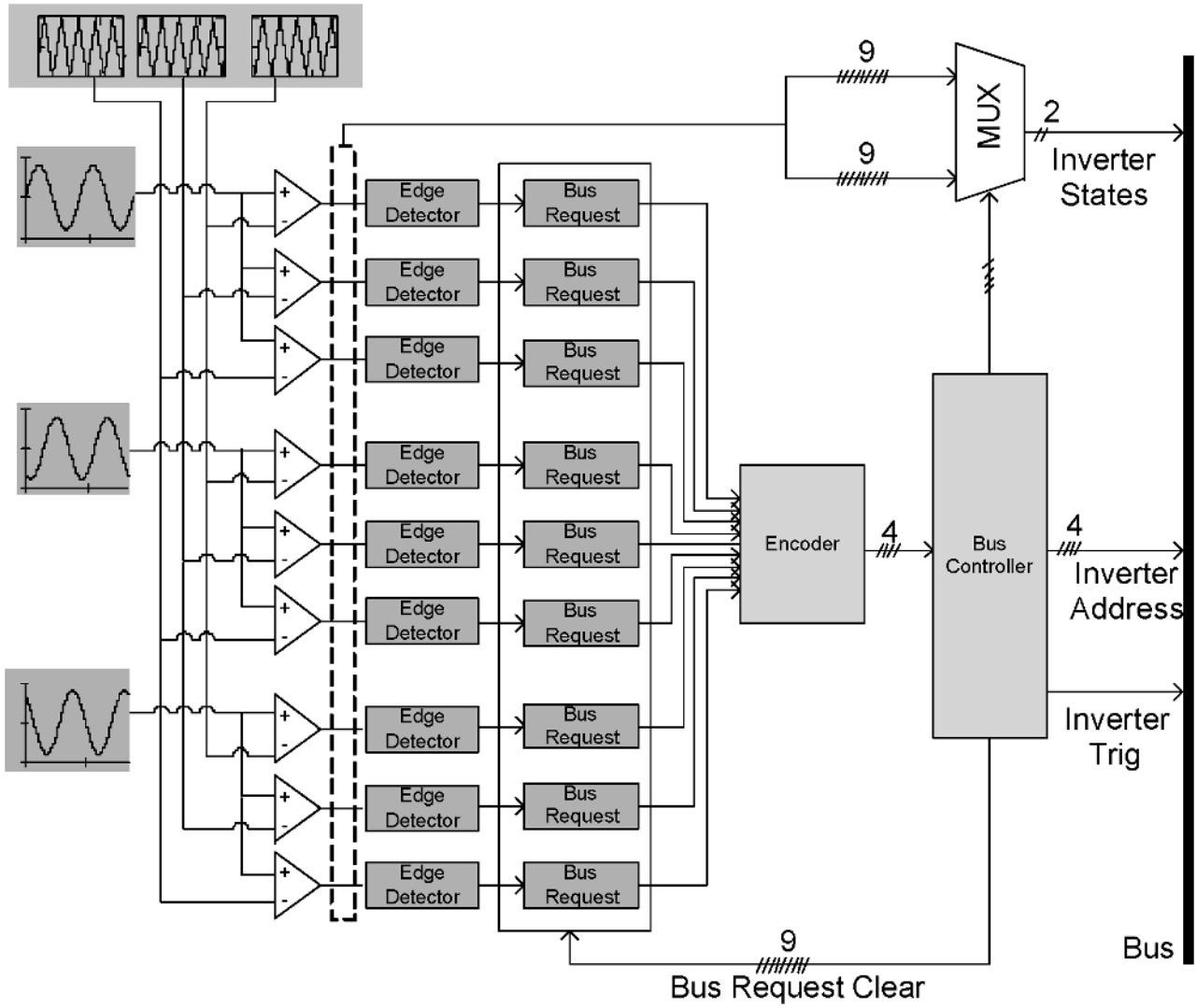

Fig. 12. Implementation of phase shifted carrier based PWM modulator.

phase. All the switching events for nine modules (36 switches) are encoded into data packets, comprised of switching states and address, triggering etc. These data packets are sent to each module via a data bus connecting the nine modules to a central controller where the FPGA resides. Hardware implementation of PWM renders fast speed and saves the resources of DSP.

Voltage sag for the laboratory system is generated with SmartSource 345-ASX, which is programmable to generate voltage sags. A photograph of the experimental setup is shown in Fig. 13. The transient response of the experimental system to a balanced sag in the line voltage is shown in Fig. 14 to match the results of simulation illustrated in Fig. 10. It may be observed that in both computer simulations and experimental results, the response time of the system soon after the disturbance is about a half a cycle of the ac waveform, confirming the prediction based on closed loop transfer functions. However, this response speed would only lead to an acceptable deviation from the nominal conditions, as defined by power quality susceptibility norms such as the SEMI-F47 or the CBEMA curve [23], [24]. Due to the difficulties generating appropriately controlled unbalanced voltages in the laboratory experimental results for unbalanced voltage sag are not reported here.

VII. Conclusion

This paper has presented the realization and control features of a DVR using an ac stacked multilevel converter with cascaded H-bridges. The power circuit architecture has been discussed followed by a model development leading to the regulator design. The system is modeled in the synchronous reference frame accounting for positive and negative sequence voltage sags to be mitigated. The multiloop regulator with complex state feedback decoupling is designed with an inner current loop and outer voltage loop. The controller features robust design margins, excellent output impedance, and line regulation as illustrated using frequency response predications. Detailed numerical simulation has been carried out to verify the power circuit operation and control scheme. A laboratory scale experimental prototype was developed that verifies the power circuit operation and controller performance. Experimental results indicate excellent agreement with digital simulations.

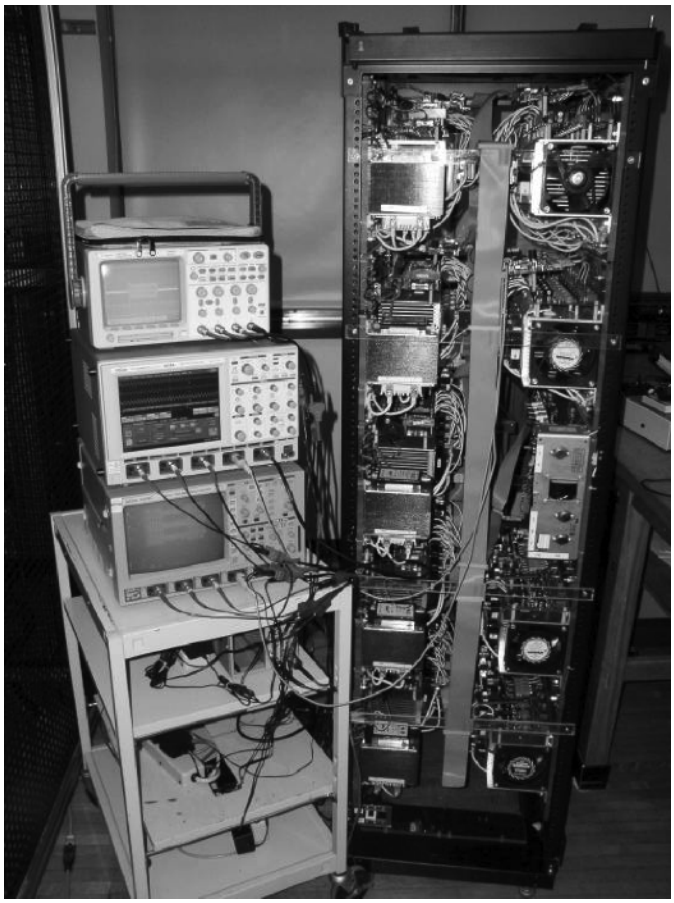

Fig. 13. Photograph of the experiment setup.

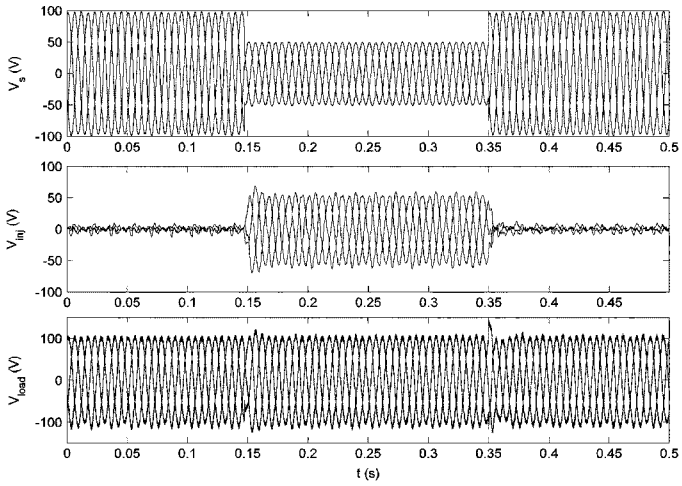

Fig. 14. Experimental results for balanced case: from top to bottom traces are source voltages, injected voltages, and load voltages.

The realization of the power and control circuit incorporates a common filter capacitor and a centralized controller. It may, however, be desirable to distribute the filter capacitor across each series injection module to accommodate voltage sharing. Such a realization would multiply the present second-order dynamic system per phase into a sixth-order dynamic system per phase, leading to a larger number of degrees of freedom, requiring an alternative controller structure. For instance, part of the control function could be distributed to each module and a hierarchical structure may be obtained. The other control schemes such as optimal controller are under investigation and results will be reported in future work.

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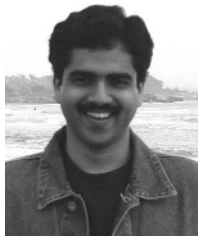
Bingsen Wang (S'01) was born in China. He received the M.E. degree in electrical engineering from Shanghai Jiao Tong University, Shanghai, China, in 1997, the M.S. degree in electrical engineering from the University of Kentucky, Lexington, in 2002, and is currently pursuing the Ph.D. degree in the Department of Electrical and Computer Engineering, University of Wisconsin, Madison.

From 1997 to 2000, he was with Carrier Air Conditioning Equipment Co., Shanghai, as an Electrical Engineer. He is a member of Wisconsin Electric Machine and Power Electronics Consortium (WEMPEC). His research interests include power converter topologies, particularly multilevel converters and matrix converters, dynamic modeling and control of power electronics systems, application of power electronics to power quality problems and FACTS, and electric drives.

Giri Venkataramanan (M'92) received the B.E. degree in electrical engineering from the Government College of Technology, Coimbatore, India, in 1986, the M.S. degree from the California Institute of Technology, Pasadena, in 1987, and the Ph.D. degree from the University of Wisconsin, Madison, in 1992.

After teaching electrical engineering at Montana State University, Bozeman, he returned to the University of Wisconsin, as a faculty member in 1999, where he continues to direct research in various areas of electronic power conversion as an Associate Director of the Wisconsin Electric Machines and Power Electronics Consortium (WEMPEC). He holds five U.S. patents and has published a number of technical papers. His interests are in the areas of microgrids, distributed generation, renewable energy systems, matrix and multilevel power converters, and ac power flow control.



Mahesh Illindala (S'01–M'06) was born in Hyderabad, India. He received the B.S. degree from the National Institute of Technology, Calicut, India, in 1995, the M.S. degree from the Indian Institute of Science, Bangalore, in 1999, and the Ph.D. degree from the University of Wisconsin, Madison, in 2005.

Currently, he is a Power Electronics Engineer with the Technology and Solutions Division, Caterpillar, Peoria, IL. His earlier industrial experience was with Larsen and Toubro, Ltd., India and Bull Power Systems, Ltd., India. His research interests include power electronics, utility applications, distributed generation, and control systems.