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Operational Testing of 4H-SiC JFET ICs for 60 Days Directly Exposed to Venus Surface Atmospheric Conditions

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ABSTRACT Prolonged Venus surface missions (lasting months instead of hours) have proven infeasible to date in the absence of a complete suite of electronics able to function for such durations without protection from the planet's extreme conditions of ~460 °C, ~9.3 MPa (~92 Earth atmospheres) chemically reactive environment. Here, we report testing data from a successful two-month (60-day) operational demonstration of two 175-transistor 4H-SiC junction field effect transistor (JFET) semiconductor integrated circuits directly exposed (no cooling and no protective chip packaging) to a high-fidelity physical and chemical reproduction of Venus surface atmospheric conditions in a test chamber. These results extend the longest reported duration of electronics operation in Venus surface atmospheric conditions almost threefold and were accomplished using prototype SiC JFET chips of more than sevenfold increased complexity. The demonstrated advancement marks a significant step toward realization of electronics with sufficient complexity and durability for implementing robotic landers capable of returning months of scientific data from the surface of Venus.

INDEX TERMS Silicon carbide, high-temperature techniques, JFET integrated circuits, space technology.

I. INTRODUCTION & MOTIVATION

A variety of planetary science committee reports have described the importance of achieving improved understanding of Venus and its greenhouse effect atmosphere and geology [1]–[4]. For example, such insight has relevance to understanding solar system formation as well as a better understanding of the Earth. Towards this end, these reports call for long-term surface observations of seismic activity and atmospheric conditions that can only be acquired via prolonged Venus lander missions.

Long-term operation of silicon-based integrated circuits (ICs) has enabled a variety Mars lander missions to successfully operate in its cold (−143 °C to +27 °C) atmospheric environment returning valuably insightful scientific data for months and years [1], [5], [6]. However, achieving similar mission duration on the surface of Venus has proven an insurmountable challenge to date, in large part due to the absence of mission-enabling electronics that can operate unprotected from the ~460 °C, ~9.3 MPa and the highly reactive chemical media that are characteristics of the Venus surface environment [5]–[8]. Since Venus surface conditions fall well beyond the operating realm of silicon-based ICs [9]–[11], all prior Venus landers have employed pressure vessels and/or thermal insulation systems to protect mission-critical IC electronics. Such protection measures added substantial launch mass and mission expense, yet were only effective for an hour or two before the surrounding Venus environment overcame the protection and thermally failed the silicon IC-based lander electronics. To date, the longest

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duration of data return from the surface of Venus surface is 2 hours and 7 minutes in 1978 by the ~760 kg Venera 13 lander [3], [5]–[8].

A number of updated Venus lander designs have been studied over the intervening decades, including combinations of active cooling (refrigerator) subsystems and expanded silicon-IC capabilities [3], [8]. Common drawbacks of proposed lander designs whose electronics (or even a fraction of the electronics) must be sheltered from the Venus environment in order to function are that the proposed durations of useful science return have been limited to less than a few days, and the proposed lander masses have exceeded 500 kg. The historical consequence of these severe drawbacks has been that no landers have touched down on the surface of Venus in over three decades, despite the widely recognized high scientific value of obtaining more comprehensive observations from the surface of Venus. Robotic missions featuring lower payload mass offering more prolonged scientific data return from other regions of the solar system have out-competed proposed brief-duration with high-mass Venus landers for available planetary exploration flight funding.

Given the electronics protection driven limitations of prior Venus lander designs, it has been recognized for some time that long duration Venus lander missions would require a complete suite of lander operations electronics and sensors functioning for long-duration in, and without protection from, the extreme environment. As a variety of wide bandgap semiconductor (SiC and III-Nitride) transistors and circuits have been reported to operate at $T \geq 460$ °C over the last two decades, these progressing wide bandgap technologies have been pondered as candidates for use in Venus surface exploration missions [12]–[14]. The fact that wide bandgap ICs are far less complex/developed/capable than modern silicon ICs is arguably a perceived technical barrier. However, considering the successful pioneering space exploration missions (including landers) launched prior to the 1980's using comparably immature silicon IC technology of the time [15], the simplicity of today's wide bandgap ICs is not actually a major impediment preventing successful engineering of scientifically useful prolonged-mission Venus lander electronics. Arguably, a larger technical barrier to prolonged-mission Venus lander IC feasibility was that stable electrical operation in excess of 1 week has not been reported for the majority of wide bandgap $T \geq 460$ °C IC demonstrations conducted to date [16]–[23].

As of this writing, the only reports of months of stable $T \geq 460$ °C semiconductor IC operation have been circuits based on integrated SiC JFETs and resistors tested in high-temperature ceramic packages in Earth-air atmosphere ovens [24]–[32]. In 2016, such SiC JFET IC chips successfully demonstrated 21 days (3 weeks) of operation in a high-fidelity reproduction the Venus surface environment comprised of the first 9 chemical atmospheric constituents (including sulfur dioxide and gaseous acids HCl and HF) at full Venus pressure (~9.3 MPa, ~92 Earth atmospheres) and ambient temperature (460 °C) [33]. In that demonstration, two ring-oscillator chips (one with 12 JFETs and the other with 24 JFETs) were immersed in the Venus surface environment without package lid or any other form protection or cooling. The landmark demonstration verified for the first time that SiC JFET IC electronics can be operated for prolonged duration without highly cumbersome and/or challenging physical protection (e.g., pressure vessels, thermal management, Venus-hermetic chip packaging, etc.) from the Venus surface environment, including its corrosive chemical constituents. Based upon this realization, NASA has now initiated development of paradigm-shifting Venus surface mission concepts and demonstration hardware. An example of such a mission concept is the ~10 kg Long-Lived (or Long-Life) In-Situ Solar System Explorer (LLISSE) lander designed to return Venus surface meteorological data (including temperature, pressure, wind, and concentrations of selected atmospheric gasses) for more than 60 days [34]. Another example based on the same fundamental approach but with emphasis on seismology is the Seismic and Atmospheric Exploration of Venus (SAEVe) lander [35]. By eliminating the need to protect its electronics from the Venus surface environment, the LLISSE and SAEve concepts promise the order of 50-fold improvements in both mission duration and lander mass compared to designs that rely on environmentally sheltered electronics.

A more-recent generation of prototype SiC JFET ICs developed and fabricated by NASA Glenn have now progressed to over a year of continuous operation at 500 °C in Earth air atmosphere ovens with complexity up-scaled to 195 transistors per IC [31], [32]. This upscaled level of integrated circuit complexity for ICs proven durable for months at $T \geq 460$ °C is comparable to silicon chip complexities flown in 1970's era planetary exploration missions and Earth-orbiting satellites [15]. Here, we report electrical test data of two of these more-complex SiC JFET ICs that operated successfully for two months (60 days) immersed in and unprotected from a high-fidelity test chamber reproduction of Venus surface atmospheric conditions. The results represent a significant advancement in demonstrated Venus surface environment IC complexity and duration of operation towards levels sufficient for implementation of initial long-duration Venus lander missions.

II. EXPERIMENTAL

The electrical characterization of ICs operating inside a hazardous high-pressure and high-temperature test chamber that reproduces the atmospheric conditions found at the Venus surface remains a challenging and rarely-attempted endeavor. While the focus of this publication is the SiC JFET ICs and their measured electrical performance during functional testing in simulated Venus surface atmospheric conditions, this Experimental section also describes aspects of the setup

and procedures that influenced the fidelity of IC electrical measurement data. Unless specified otherwise below, the experimental setup and procedures employed to carry out the 21-day Venus environment IC test described in [33] (and its "Supplemental Materials" addendum) were repeated for this 60-day test.

A. INTEGRATED CIRCUITS

The IC chips tested in this report were diced from a recent 4H-SiC JFET IC prototype wafer (designated "Wafer 10.1") fabricated at the NASA Glenn Research Center. The basic device structures, logic gate approach, fabrication process, circuit schematics, and more than 10,000 hours of 500 °C Earth-air oven-testing of chips from this wafer have been described in previous publications [31], [32]. The n-channel JFET (6 μm gate-length) and resistor IC topology with two levels of interconnect is effectively the same as employed for the "Wafer 9.2" ICs run in the previously reported 21-day Venus environmental test [33]. In this topology, logic signals are represented by negative voltages, with logic "1" voltage V_{OH} near 0 V and logic "0" voltage V_{OL} near -10 V. However, compared to previous prototype NASA Glenn JFET IC wafers, Wafer 10.1 implemented demonstration ICs with more than 7-fold higher transistor counts (up to 195 JFETs per IC). Yields in excess of 70 % were documented for the higher-complexity circuits in room-temperature probing prior to dicing the wafer into individual chips [31].

A pair of 175-JFET "÷2/÷4 Clock" demonstration IC chips from Wafer 10.1 were selected and separately prepared for the 60-day Venus environment test. As reported in [31] and [32], this technology demonstration IC provides a "base" frequency clock signal generator (a 21-stage ring oscillator) with electronically selectable divide by 2 or divide by 4 output signal frequencies achieved using two D-type flip flops and control signal logic. The complete functionality of this IC can be verified using only four input signals (SELECT input plus chip power lines $+V_{DD}$, GND, and $-V_{SS}$) and one output signal. It should be noted that additional functionality intended for this IC was not realized due to a mask layout error that precluded a third D-type flip flop residing on the chip from functioning. The JFETs that physically reside in this non-functional flip flop have thus been excluded from the 175 functional JFET count.

The two 3 mm × 3 mm ÷2/÷4 clock IC demonstration chips were die-attached and wire bonded into separate high-temperature co-fired ceramic (HTCC) packages without lids and mounted at the ends of separate high-pressure/temperature feedthroughs as described in [36].

B. TEST CHAMBER (GEER) AND FEEDTHROUGH ASSEMBLIES

The prototype ICs were tested in the NASA Glenn Extreme Environments Rig (GEER). The GEER apparatus consists of an 800-liter cylindrical shaped stainless-steel pressure vessel outfitted with three internal AC-phase controlled electric heaters and gas injection system needed to reproduce Venus surface atmospheric conditions of 460 °C, ~9.3 MPa pressure consisting mostly of CO_2 and N_2 as well as traces of SO_2, H_2O, CO, OCS, HCl, HF, and H_2S [9]. Further details of the GEER system and its operation are described in [33] and [37].

A major challenge of Venus-environmental IC testing is implementation of electrical feedthroughs that enable wires to safely and reliably carry signals between ICs residing inside the 460 °C, ~9.3 MPa GEER chamber environment and electrical measurement instrumentation residing outside in benign Earth-air ambient. Towards this end, two feedthrough probe assemblies (respectively designated "FT4" and "FT5") to hold the two ÷2/÷4 clock chips and interface electrical bias/signal wires through robust high-temperature high-pressure seals were custom-designed and constructed. Ideally, these feedthroughs would relay all electrical signals with excellent fidelity throughout the entire test. In reality however, feedthrough probes (particularly the portions directly exposed to the Venus environmental conditions) employed for the 21-day test were observed to contribute (to increasing degree as the test progressed) significant electrical parasitic effects (including short-circuit failure) [33], [38]. In an attempt to reduce the feedthrough probe assembly electrical degradation and parasitics, a modified feedthrough probe assembly design was implemented for this 60-day test.

Each feedthrough assembly contained a thermocouple residing less than 1 cm away from the IC chip to facilitate close-proximity temperature measurement. As described in [36], each feedthrough assembly also provided a pair of wires that were connected to electrically isolated package leads in order to facilitate periodic independent DC measurement of an "insulation/isolation resistance" of the feedthrough assembly that ideally would have been an infinite resistance open circuit throughout the entire test. Due to the perceived risk of signal shorting/shunting posed by the unproven feedthroughs (that in the end turned out to be well-founded), the unbuffered base clock signal generated on the IC was not connected to a feedthrough and was therefore not directly monitored.

C. ELECTRICAL TESTING – THREE ENVIRONMENTAL TEST PHASES

After the ICs were packaged and mounted in respective feedthrough probe assemblies, three phases of extreme environmental electrical IC testing were conducted in the following sequence: "Phase 1" was conducted by inserting the chip end of the feedthrough assembly into an Earth-air ambient oven. Temperature was increased from 25 °C to 460 °C at a ramp rate of ~3 °C/minute, then held at 460 °C for 50 hours, before cooling back to room temperature at a rate $\leq$ 3 °C/minute. Phase 1 served to

validate the feedthrough probe assembly at high temperature, and also to retire some (but clearly not all) of the previously reported minor IC "burn-in" electrical property changes that occur during early stages of high temperature NASA Glenn JFET IC tests [28]–[32]. The oven was cooled and the feedthrough assemblies were then removed, relocated (after a week or two of unbiased storage in air) and sealed onto GEER for high-pressure "Phase 2" and "Phase 3" testing.

For Phase 2, GEER was prepared as described in [33], filled with dry N_2 gas to a pressure of 3.6 MPa at 25 °C, then heated from 25 °C at a ramp rate near 7 °C/hour until temperature of 460 °C and pressure of 9.3 MPa was achieved. This condition was held for 48 hours, after which the chamber was cooled to 150 °C over the course of 2 days. For Phase 3, the temperature was held at 150 °C and excess nitrogen from Phase 2 was vented. GEER was filled with the Venus gas mixture, then heated at 7 °C/hour. The "Venus time" clock was tracked using standard (Earth) days/hours/seconds time (instead of timescales based on Venus's much different planetary rotational period) and started when GEER stabilized at 460 ± 1 °C and 9.3 ± 0.1 MPa (~92 Earth atmospheres) pressure containing the Venus gas mixture. The test in Venus conditions lasted 60 days, corresponding to both the desired minimum duration of the LLISSE mission concept [34] as well as the time allocated in the GEER facility schedule.

During all 3 testing phases, both ÷2/÷4 clock ICs were powered and operated continuously, except for (1) occasional ~20 second time periods when clock IC power was zeroed to minimize crosstalk noise while feedthrough "open circuit" wire/package isolation resistance measurements were being recorded using DC source/measure units, and (2) power was occasionally removed from one IC for ~10 seconds just before and during waveform capture for the opposite IC in order to avoid measurement signal crosstalk. The SELECT input line of both clock ICs was driven by a 5 kHz, 0 V to −10 V 50 % duty cycle square wave input from a pulse generator instrument, which enabled both ÷2 and ÷4 frequency output modes to be readily observed in a single IC output signal waveform capture. Output signal waveforms were recorded using digitizing oscilloscope with AC-coupled 10 MΩ probes. Output signal frequencies were extracted post-test from the recorded waveforms using standard LabVIEW-based waveform analysis routines. The SELECT input waveform was simultaneously recorded using a dedicated DC-coupled channel to the same digitizing oscilloscope. The clock ICs were powered at all temperatures by $V_{DD} = +25$ V and $V_{SS} = -25$ V.

Due to safety and other considerations, all circuit measurement instruments and control computer resided in a separate (protected) room from GEER. Therefore, all electrical connections between feedthroughs and instruments were made via ~23 m long 2404C 4-conductor cables traversing safety-wall penetrations for Phase 2 and Phase 3 IC testing.

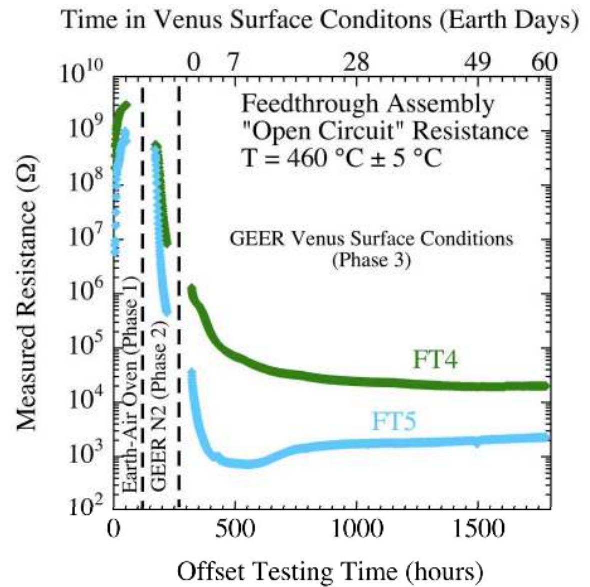

FIGURE 1. Measured "open circuit" resistance of unconnected test wires in the two chip-holding high-pressure feedthrough assemblies (FT4 and FT5) recorded during all three environmental test phases for constant temperature of 460 °C. Electrical isolation of the Venus-environment-exposed feedthrough wiring severely degraded during high-pressure test phases with significant impact to measurement of IC output signal magnitude. Data re-formatted from [36].

III. RESULTS & DISCUSSION

A. FEEDTHROUGH WIRING AND PACKAGING RESULTS

The measured electrical behavior of the feedthroughs and packaging for this 60-day Venus surface environment test are described in [36]. Despite design improvements implemented following the 21-day Venus surface conditions test, the feedthrough probe assemblies for this 60-day Venus conditions test nevertheless exhibited substantial changes in electrical properties that are succinctly summarized here since these property changes affected the IC electrical testing results described in the following Section III-B. Figure 1 (slightly re-formatted from [36]) illustrates the drastically large change in "open circuit" "insulation resistance" measured between the two electrically isolated package leads for both probe assemblies at constant temperature of 460 °C ± 5 °C during all three testing phases. While the insulation resistance is desirably high on the order of giga-ohms for Phase 1 (Earth-air oven), measured insulation resistances dropped orders of magnitude (to the order of kilo-ohms) during high-pressure testing in Phases 2 (N_2) and 3 (Venus gas mixture). As described in [36], insulation resistance decline was ascertained to be predominantly caused by degradation of (i.e., loss of electrical isolation between) fiberglass-insulated wires running inside the Venus-environment side of the feedthrough probe assembly.

B. IC RESULTS IN VENUS SURFACE CONDITIONS

While the degradation of wire-to-wire electrical isolation in the feedthrough probe assemblies affected some quantitative IC measurements, the consequent electrical parasitic effects

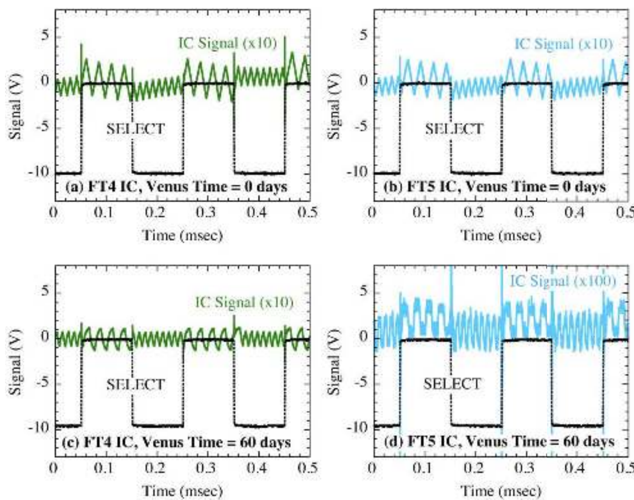

FIGURE 2. ÷2/÷4 clock IC test waveforms measured at the digitizing oscilloscope for FT4 (left, green) and FT5 (right, blue) at the start and end of the 60-days (Earth timescale) of functional testing immersed in chamber reproduction of Venus surface atmospheric conditions. Recorded IC output signals are substantially distorted and attenuated by loading effects (see text). While the IC output signal magnitudes changed due to degradation of feedthrough wiring isolation (Fig. 1), complete IC functionality is conclusively demonstrated by the 2-fold signal frequency modulation of chip-generated periodic signal by the SELECT (black) input signal.

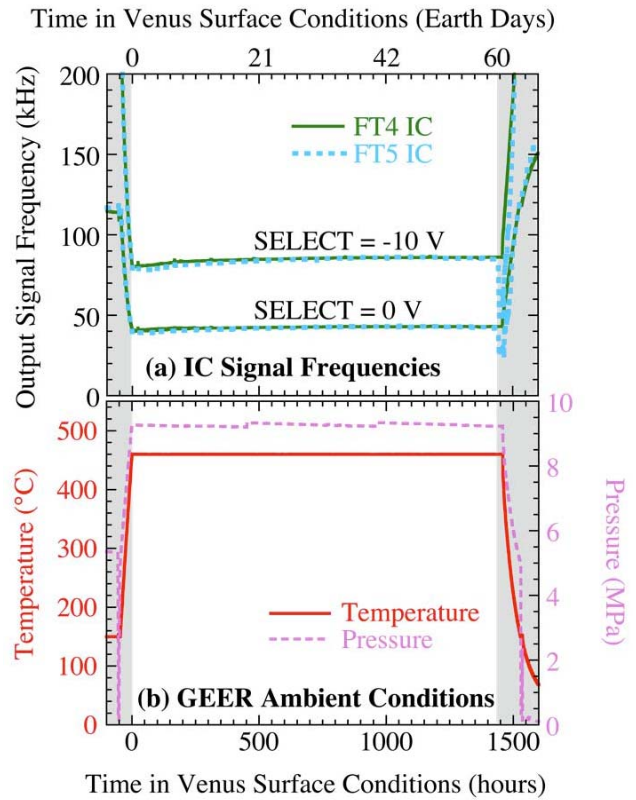

FIGURE 3. Summary of ÷2/÷4 clock IC test data recorded vs. time in Venus surface atmospheric conditions (Phase 3). (a) Measured FT4 (green, solid) and FT5 (blue, dashed) output signal frequencies measured for SELECT inputs of 0 and −10V. (b) Recorded GEER temperature (red, solid) and pressure (purple, dashed).

did not preclude verification of ÷2/÷4 clock IC operation during the test in simulated Venus surface atmospheric conditions. Figure 2 plots the experimentally measured FT4 (left, green) and FT5 (right, blue) clock IC waveforms recorded by the digitizing oscilloscope at the start (top, (a) & (b)) and conclusion (bottom, (c) & (d)) of the 60-day testing time in the chamber under Venus surface conditions during Phase 3 testing. The recorded SELECT 0 V to −10 V input square wave signals are shown in black while the recorded ÷2/÷4 clock IC output signals are plotted as colored traces.

All of the Fig. 2 clock IC output signal amplitudes recorded by the oscilloscope are well below the ∼ 10 V logic swing reported in 500 °C Earth-air oven testing of this same chip design [31], [32], and there are also significant differences evident between starting (0 days) and ending (60 days) amplitudes. These observations are consistent with understood behaviors seen in preceding studies of SiC JFET ring oscillator ICs [26], [27], [30], [33], [39]. It is well known that measurement probe loading effects must be considered when measuring electrical signals using an oscilloscope, especially when measuring circuits with both high output resistance and high frequency signal (as is the case for these clock ICs) [40]. Loading-related distortion/attenuation arises from the combined electrical parasitics of the ceramic package, feedthrough assembly wiring, ∼23 m long cables, and 10 MΩ oscilloscope probes, and is also dependent on IC output signal frequency. Given the drastic temporal changes of feedthrough wiring isolation properties seen in Fig. 1 and [36], as well as substantial differences between FT4 and FT5, conclusions regarding IC operational performance cannot be credibly inferred based upon numerical signal magnitudes measured at the oscilloscope.

Regardless of the inconsistent signal amplitudes reaching the oscilloscope, complete functionality of the ÷2/÷4 clock IC can nevertheless be conclusively ascertained via the 2-fold change in output signal frequency that directly corresponds to the value of the SELECT input control signal. Such output signal functionality is uniquely generated by successful operation of the ÷2/÷4 clock IC, starting from periodic signal generation by the 21-stage ring oscillator through electronically controlled frequency division via multiple flip flop-based logic. Given that clock circuit output frequencies are governed by on-chip signal propagation, these output frequencies are far less affected by off-chip (e.g., changing feedthrough assembly) electrical parasitics so long as adequate electrical input signals reach the ICs (e.g., SELECT, $+V_{DD}$, GND, and $-V_{SS}$ subject to changing parasitic shunt losses in the non-ideal feedthroughs). Therefore, clock chip output frequency data provides relatively simple and direct measure of inherent IC chip electrical performance including operational stability over time.

Fig. 3(a) plots both ÷2 and ÷4 mode output frequencies extracted from recorded FT4 and FT5 IC output

waveforms throughout the 60-day Venus surface conditions test. Fig. 3(b) plots the corresponding GEER chamber temperature and pressure environmental conditions. Data for some of the heat-up and cool-down are also included in the grey-shaded regions at left and right ends of the Fig. 3 graphs. The slight discontinuities in the Fig. 3(b) pressure data near 20 days and 40 days correspond to GEER pressure boosts implemented to offset slow leakage of gas from the chamber during the prolonged test.

As indicated by the nearly time-independent frequencies plotted in the unshaded Fig. 3(a) graph regions, both ICs successfully functioned with less than 13 % frequency change over the course of the 60 days immersed in Venus surface conditions. We note that the majority of the minor frequency increase over time took place during the first 20 days. Such a trend is qualitatively consistent with burn-in data tails of slightly increasing frequency observed in prior T $\geq$ 460 °C JFET IC ring oscillator testing [29]–[32]. As intended, each IC maintained the logic-designed factor of 2 difference in frequency between ÷2 and ÷4 operating modes. Comparing FT4 relative to FT5, the frequency vs. time traces plotted in Fig. 3(a) are nearly identical over the 60-day Venus test. Based on this data, we conclude that both ÷2/÷4 clock demonstration ICs and HTCC packages successfully operated in the test chamber exposed to Venus surface atmospheric conditions without any protection for an unprecedented duration of 60-days while exhibiting minimal changes in IC electrical performance.

It is worth noting that just after the completion the 60-days, the FT5 IC experienced a sudden drop in output frequencies for about 15 hours, but then recovered and remained stable for the remainder of the cool-down. While the cause of this post-test anomaly is not clearly understood at this time, it is conceivable that temperature/time-dependent shunting of power supply signal to the IC might be responsible, especially since we have routinely observed frequency shifting of ring oscillators while making power supply bias adjustments in other experiments. Despite the temporary frequency drop, the logic-designed 2-fold frequency difference was maintained throughout this FT5 post-test anomaly.

C. IC RESULTS IN OTHER ENVIRONMENTAL CONDITIONS

While the main purpose of this work is IC demonstration in Venus surface atmospheric conditions, it is nevertheless worth considering measured IC behavior across the broader range of environmental conditions employed during all the testing phases. It can be noted in Fig. 3 that pressure changes (some as large as ∼ 50 atmospheres before and after Venus conditions) had insignificant impact on IC output frequencies. Figure 4 comparatively plots FT4 ÷2/÷4 clock IC output frequencies as a function of temperature during all three test phases after the initial 50-hour 460 °C Earth-air burn-in stabilization. Colored arrows annotate if data was taken during the heating or subsequent cooling associated with each test phase. The plots reveal minor frequency increase between the three sequential high temperature test phases. Within each high-pressure test phase (2 and 3), each mode frequency during heat-up at a given temperature was slightly lower than the corresponding mode frequency for the same temperature during subsequent cooldown. These observed trends are generally consistent with high temperature burn-in trends previously seen for ring oscillator ICs in which frequency slightly increased over first 1000-2000 hours of high temperature testing [29]–[32]. The observed substantial decrease in frequency with increasing temperature (∼ 4-fold drop from 25 °C to 460 °C) is quantitatively consistent with trends and mechanisms previously reported for this 4H-SiC JFET IC technology [27], [39].

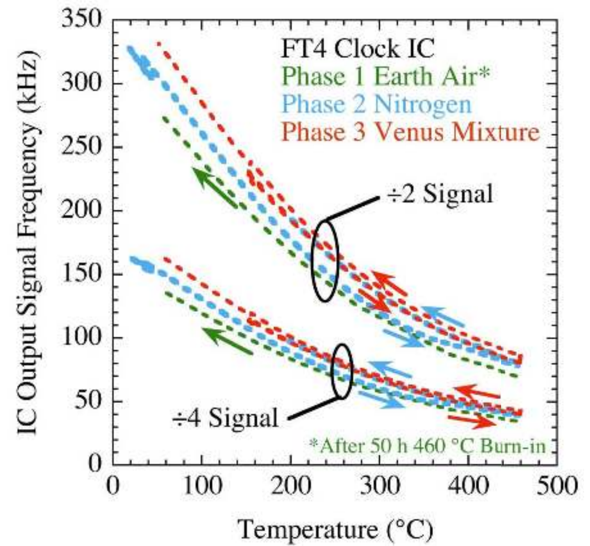

FIGURE 4. Comparison of measured FT4 clock IC signal frequencies as a function of temperature during all three environmental test phases. Arrows indicate where data was taken during temperature ramp-up or ramp-down. For all measurements the IC was powered by V_{DD} = +25 V and V_{SS} = −25 V. The trends shown are consistent with previously reported SiC JFET IC ring oscillator behavior (see text).

Based on Fig. 3 and Fig. 4 data, we conclude that temperature is the predominant environmental variable affecting IC output frequency. Pressure and gas composition had negligible effect on IC performance in this work.

D. POST-TEST IC EXAMINATION

Following its post-test removal from GEER, the FT4 assembly was placed into storage for further operational testing in a future GEER test. The FT5 feedthrough was disassembled and the ceramic package with its ÷2/÷4 clock IC was removed for further study [36].

Fig. 5 compares optical micrographs of a region of the FT5 ÷2/÷4 clock IC (a) prior to packaging, and (b) following Venus-condition testing in GEER and subsequent

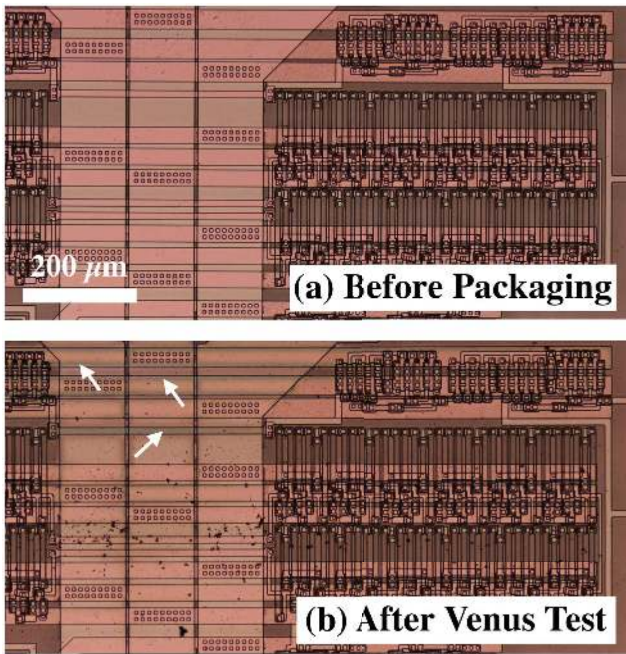

FIGURE 5. Optical micrographs of integrated circuitry on the FT5 ÷2/÷4 clock IC taken (a) before chip packaging and (b) after completion of the 60-day Venus conditions test. Arrows denote three examples of post-test discoloration in horizontally running Metal 2 traces symptomatic of metal reactions facilitated by cracking of the protective overlying dielectric layers. Dark splotches are particulates on the dielectric-coated chip surface.

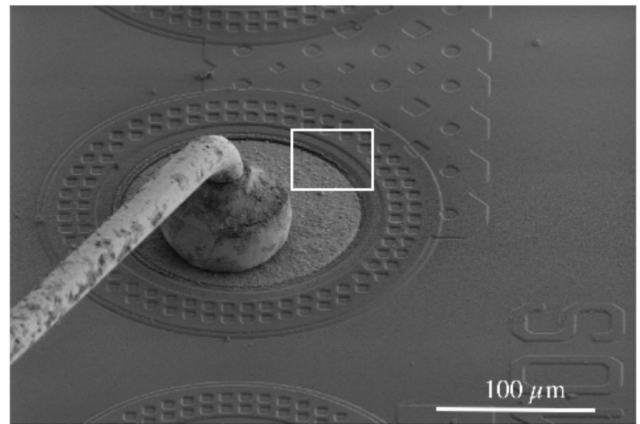

FIGURE 6. Field emission scanning electron microscopy (FESEM) image of the gold wire bond and bond pad metallization following 60 days exposure to simulated Venus surface atmospheric conditions. White square depicts region enlarged in Fig. 7(b). All bond pads remained functional following the 60 days of operation in Venus surface atmospheric conditions.

removal from the feedthrough assembly. The three largest vertical metal traces are the main power buses implemented in Metal 1 (~1 μm thick $TaSi_2$), which are electrically connected by arrays of multiple dielectric vias to narrower horizontal Metal 2 (~ 1 μm thick $TaSi_2$) traces carrying power to various sub-circuits (e.g., ring oscillator) in the images. As described in [31] and [32], the integrated circuitry is protectively overcoated by optically transparent ~2 μm thick multi-layer dielectric (1 μm SiO_2 + 67 nm Si_3N4 +1 μm SiO_2).

The changes in FT5 chip appearance between Fig. 5(a) and Fig. 5(b) fall into two major categories: particulates and metal discoloration. The dark splotches in post-test Fig. 5(b) image are particulates on the chip surface that are rendered electrically harmless by the protective layers of dielectric passivation overcoating the chip circuitry. The three arrow annotations in Fig. 5(b) highlight a few examples of where horizontally oriented Metal 2 traces in the top half of the image have experienced discoloration. However, it is important to note that a number of other horizontally oriented Metal 2 traces in the lower half of the same image exhibit no trace of such discoloration. In our previous studies of ICs tested at T $\geq$ 500 °C in Earth air ambient ovens, such discoloration has been symptomatic of $TaSi_2$ metal trace oxidation and failure occurring where cracks (or networks of multiple cracks often running along metal line topology) formed in the overlying dielectric passivation layers [41], [42]. While the post-test presence of dielectric cracks was confirmed for the discolored metal regions at higher magnification, it is uncertain to what degree cracking and metal reaction/discoloration occurred during each of the three test phases. Experimental studies aimed at further understanding and mitigation of the dielectric cracks are in progress at this time.

The bond pads on the FT5 chip from Wafer 10.1 were also studied after the 60-day test for comparison with 21-day test bond pad findings from Wafer 9.2 [38]. A field emission scanning electron microscope (FESEM) image of the 60-day post-test bond pad with a gold wire attached is shown in Fig. 6. While there are some chamber particulates visible on the gold wire, the wire and the bond pad itself remained functional in the Venus atmosphere, similar to the 21-day test.

Fig. 7 shows a higher-magnification comparison of bond pad rim regions (illustrated by white box in Fig. 6) between the 21-day and 60-day tests. Fig 7(a) shows platinum sulfide (PtS) fibers growing along the 21-day bond pad edge. Such PtS fibers are not evident on the 60-day bond pad shown in Fig. 7(b). In-depth analysis of the bond pad materials and the reactions occurring after the 21-day Venus exposure was detailed in [38]. Those results indicated that wherever Pt was exposed to the Venus atmosphere in the absence of overlying Au (as in the case of the bond pad rims in the 21-day test chip from Wafer 9.2), the Pt would react with the sulfur containing gas species and form PtS fibers. By tightening the tolerances of the photolithography/alignment processing for the Wafer 10.1 bond pads (via slight increase of the Au liftoff pattern diameter), platinum exposure along the bond pad rims was significantly reduced (from roughly 10 μm on Wafer 9.2 to less than 2 μm on Wafer 10.1) which effectively eliminated PtS fibers from bond pad rims following the 60-day test. Direct contact of overlying Au to the oxide was avoided in the bond pad design as a precaution

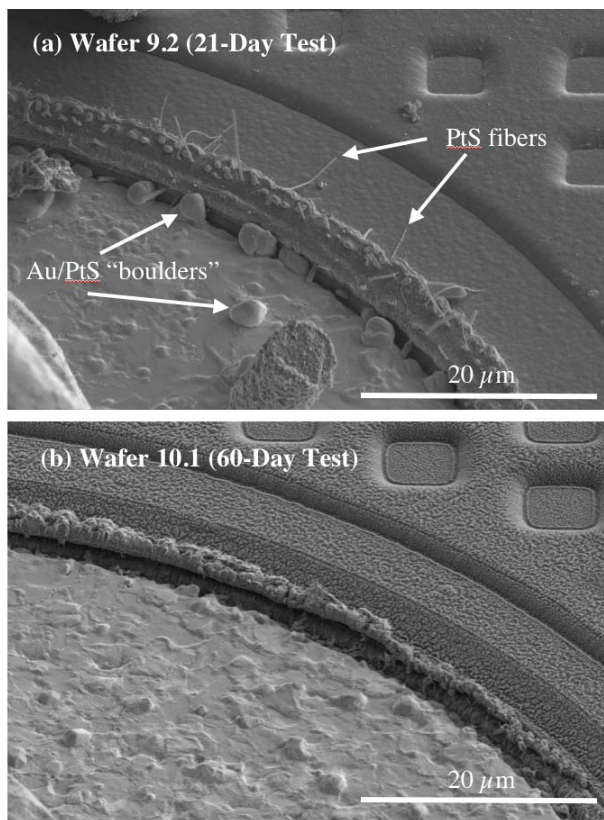

FIGURE 7. FESEM images detailing bond pad rim areas. (a) PtS fibers and Au/PtS "boulder" features identified after the 21-day test of a chip from Wafer 9.2 [38]. (b) Fibers and boulders were minimized in the 60-day exposure after modifications were made in chip processing and die attach for Wafer 10.1 (see text).

against potentially detrimental Au into oxide diffusion during high temperature circuit operation.

Another notable bond pad feature reported in [38] after the 21-day test was the presence of Au/PtS "boulders", such as those denoted by the annotated arrows in Fig. 7(a). The boulders were determined in [38] to be due to mixing of the underlying platinum layer with the top gold layer during an annealing step in the fabrication process. When this intermixed layer was exposed to Venus surface atmospheric conditions for 21 days, the Pt reacted with the sulfur to form PtS and the mixture was expelled to the surface as round boulders composed of separated Au and PtS materials. For the 60-day chips, the higher die-attach anneal temperature (of 600 °C, compared to 500 °C for 21-day chip) is thought to have resulted in more Pt and Au intermixing and hence fewer boulder features after Venus exposure.

Despite these noted surface reaction differences, bond pads on both the 21-day and the 60-day test chips all remained functional following their prolonged exposure to Venus surface atmospheric conditions. The absence of readily observable degradation suggests that the bond pads are capable of operation for much longer duration under these conditions.

IV. SUMMARY DISCUSSION

The successful operation of these two SiC JFET ICs and ceramic packaging for an unprecedented 60 days in Venus surface atmospheric conditions represents a significant advancement in demonstrated state of the art towards electronics needed for realization of long-term Venus lander missions. The result has effectively tripled the longest demonstrated time of operation in such conditions, with ICs over 7-fold more complex (transistor counts). Off-chip/package factors (e.g., feedthrough degradation and GEER facility scheduling) were more limiting to this extreme-environment test than the SiC JFET electronics and packaging. These results also offer promise that much longer SiC IC operation might be accomplished in future Venus-environment tests, and that similar successful results might be achieved as more statistically meaningful quantities of chips are tested.

In order to support a much more comprehensive Venus-environmental testing program, substantial improvements to the high-pressure/high-temperature feedthroughs will be needed. Therefore, on-going efforts seeking to implement more durable feedthroughs with less inter-wire leakage, less signal distortion, and less temporal dependence than presently demonstrated will be continued. Improvements to the testing setup, including remotely controlled instrumentation residing much closer to the GEER chamber, are also anticipated.

In the case that on-going work succeeds in overcoming the IC technology barriers to prolonged Venus missions, it becomes urgent to simultaneously address remaining technical impediments to realizing scientifically useful long-duration Venus landers. For example, a long-duration lander such as LLISSE [34] will also need sensors, energy storage (batteries), antennas, mechanical structure, etc. that are simultaneously low-mass, compact, and can effectively function for months immersed in the Venus surface environment without any cooling. Given startlingly different and unique reactivity we have recently reported for some common aerospace and electronics materials subjected to Venus surface environmental testing in GEER [38], we have concluded that most materials/alloys successfully employed for decades elsewhere in solar system exploration will not work for a long-term Venus surface lander mission. For this reason, parallel development of all mission-critical long-duration Venus lander components, including basic mechanical structures and wiring, is necessary in addition to further upscaling and improvements to IC capability.

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REFERENCES

[1] S. W. Squyres *et al.*, *Vision and Voyages for Planetary Science in the Decade 2013–2022*. Washington, DC, USA: Nat. Acad. Press, 2011, doi: 10.17226/13117.
[2] R. Herrick *et al.*, *Goals, Objectives, and Investigations for Venus Exploration*, Nat. Aeronautics Space Admin., Washington, DC, USA, May 2014. [Online]. Available: http://www.lpi.usra.edu/vexag/reports/GOI-140625.pdf
[3] J. L. Hall *et al.*, *Final Report of the Venus Science and Technology Definition Team, Venus Flagship Mission Study*, NASA Jet Propulsion Lab., Pasadena, CA, USA. Apr. 2009. [Online]. Available: http://vfm.jpl.nasa.gov/files/Venus+Flagship+Mission+Study+090501-compressed.pdf
[4] D. Stevenson *et al.*, *Probing the Interior Structure of Venus*, Keck Inst. Space Stud., Pasadena, CA, USA, Apr. 2015. [Online]. Available: http://www.kiss.caltech.edu/final_reports/Venus_final_report.pdf
[5] E. Kolawa *et al.*, *Extreme Environment Technologies for Future Space Science Missions*, NASA Jet Propulsion Lab., Pasadena, CA, USA, Sep. 2007. [Online]. Available: http://vfm.jpl.nasa.gov/files/EE-Report_FINAL.pdf
[6] E. Kowala, M. Mojarradi, and L. Del Castillo, "Extreme environments in NASA planetary exploration," in *Extreme Environment Electronics*, J. D. Cressler and H. A. Mantooth, Eds. Boca Raton, FL, USA: CRC Press, 2013, Ch. 2, pp. 11–22.
[7] A. T. Basilevsky and J. W. Head, "The surface of Venus," *Rep. Prog. Phys.*, vol. 66, no. 10, pp. 1699–1734, Sep. 2003, doi: 10.1088/0034-4885/66/10/R04.
[8] J. Cutts *et al.*, *Venus Technology Plan*, Nat. Aeronautics Space Admin., Washington, DC, USA, May 2014. [Online]. Available: http://www.lpi.usra.edu/vexag/reports/Venus-Technology-Plan-140617.pdf
[9] M. A. Bullock and D. H. Grinspoon, "The atmosphere and climate of Venus," in *Comparative Climatology of Terrestrial Planets*, S. J. Mackwell, A. A. Simon-Miller, J. W. Harder, and M. A. Bullock, Eds. Tuscon, AZ, USA: Univ. Arizona Press, 2013, pp. 19–54.
[10] P. G. Neudeck, R. S. Okojie, and L.-Y. Chen, "High-temperature electronics—A role for wide bandgap semiconductors?" *Proc. IEEE* vol. 90, no. 6, pp. 1065–1076, Jun. 2002, doi: 10.1109/JPROC.2002.1021571.
[11] J. A. Pellish and L. M. Cohn, "Technology options for extreme environment electronics," in *Extreme Environment Electronics*, J. D. Cressler and H. A. Mantooth, Eds. Boca Raton, FL, USA: CRC Press, 2013, Ch. 6, pp. 49–58.
[12] G. A. Landis, "Robotic exploration of the surface and atmosphere of Venus," *Acta Astronautica*, vol. 59, no. 7, pp. 570–579, Jun. 2006, doi: 10.1016/j.actaastro.2006.04.011.
[13] G. Benigno, K. Hoza, S. Motiwala, G. Landis, and A. Colozza, "A wind-powered rover for a low-cost Venus mission," presented at the 51st AIAA Aerosp. Sci. Meeting, Jan. 2013. [Online]. Available: https://doi.org/10.2514/6.2013-586
[14] C. Wilson, C.-M. Zetterling, W. T. Pike. *Venus Long-Life Surface Package (VL2SP)*. Accessed: Oct. 1, 2018. [Online]. Available: https://arxiv.org/abs/1611.03365
[15] J. E. Tomayko, "Computers in spaceflight: The NASA experience, part II: Computers on board unmanned spacecraft," in *Encyclopedia of Computer Science and Technology*, vol. 13, A. Kent and J. G. Williams, Eds. New York, NY, USA: Marcel Dekker, 1987, pp. 135–204. [Online]. Available: https://history.nasa.gov/computers/Part2.html
[16] P. G. Neudeck, G. M. Beheim, and C. S. Salupo, "600 °C logic gates using silicon carbide JFET's," presented at the Govt. Microcircuit Appl. Conf., Mar. 2000. [Online]. Available: http://ntrs.nasa.gov/search.jsp?R=20000033844
[17] C.-W. Soong, A. C. Patil, S. L. Garverick, X. Fu, and M. Mehregany, "550 °C integrated logic circuits using 6H-SiC JFETs," *IEEE Electron Device Lett.*, vol. 33, no. 10, pp. 1369–1371, Oct. 2012, doi: 10.1109/LED.2012.2206792.
[18] M. Shakir, S. Huo, B. G. Malm, M. Östling, and C.-M. Zetterling, "A 600 °C TTL-based 11-stage ring oscillator in bipolar silicon carbide technology," *IEEE Electron Device Lett.*, vol. 39, no. 10, pp. 1540–1543, Oct. 2018, doi: 10.1109/LED.2018.2864338.
[19] C.-P. Chen *et al.*, "500 °C silicon carbide MOSFET-based integrated circuits," presented at the IMAPS Int. Conf. High Temperature Electron., Jun. 2014, doi: 10.4071/HITEC-TP14.
[20] R. Hedayati *et al.*, "A monolithic, 500 °C operational amplifier in 4H-SiC bipolar technology," *IEEE Electron Device Lett.*, vol. 35, no. 7, pp. 693–695, Jul. 2014, doi: 10.1109/LED.2014.2322335.
[21] P. Alexandrov, X. Li, M. O'Grady, and J. Hostetler, "Analog and logic high temperature integrated circuits based on SiC JFETs," presented at the IMAPS Int. Conf. High Temperature Electron., Jun. 2014, doi: 10.4071/HITEC-TP12.
[22] M. Gaevski, J. Deng, G. Simin, and R. Gaska, "500 °C operation of AlGaN/GaN and AlInN/GaN integrated circuits," presented at the IMAPS Int. Conf. High Temperature Electron., Jun. 2014, doi: 10.4071/HITEC-TP16.
[23] A. M. Francis *et al.*, "High-temperature operation of silicon carbide CMOS circuits for Venus surface application," presented at the IMAPS Int. Conf. High Temperature Electron., Jun. 2016, doi: 10.4071/2016-HITEC-242.
[24] D. J. Spry *et al.*, "Fabrication and testing of 6H-SiC JFETs for prolonged 500 °C operation in air ambient," *Mater. Sci. Forum*, vols. 600–603, pp. 1079–1082, Sep. 2009, doi: 10.4028/www.scientific.net/MSF.600-603.1079.
[25] P. G. Neudeck *et al.*, "Stable electrical operation of 6H-SiC JFETs and ICs for thousands of hours at 500 °C," *IEEE Electron Device Lett.*, vol. 29, no. 5, pp. 456–459, May 2008, doi: 10.1109/LED.2008.919787.
[26] P. G. Neudeck *et al.*, "Extreme temperature 6H-SiC JFET integrated circuit technology," *Phys. Status Solidi A*, vol. 206, no. 10, pp. 2329–2345, Jun. 2009, doi: 10.1002/pssa.200925188.
[27] P. G. Neudeck, M. J. Krasowski, and N. F. Prokop, "Assessment of durable SiC JFET technology for +600 °C to -125 °C integrated circuit operation," *ECS Trans.*, vol. 41, no. 8, pp. 163–176, Nov. 2011, doi: 10.1149/1.3631494.
[28] D. J. Spry *et al.*, "Processing and prolonged 500 °C testing of 4H-SiC JFET integrated circuits with two levels of metal interconnect," *Mater. Sci. Forum*, vol. 858, pp. 908–912, May 2016, doi: 10.4028/www.scientific.net/MSF.858.908.
[29] D. J. Spry *et al.*, "Prolonged 500 °C demonstration of 4H-SiC JFET ICs with two-level interconnect," *IEEE Electron Device Lett.*, vol. 37, no. 5, pp. 625–628, May 2016, doi: 10.1109/LED.2016.2544700.
[30] D. J. Spry *et al.*, "Processing and characterization of thousand-hour 500 °C durable 4H-SiC JFET integrated circuits," presented at the IMAPS Int. Conf. High Temperature Electron., Jun. 2016, doi: 10.4071/2016-HITEC-249.
[31] D. J. Spry *et al.*, "Prolonged 500 °C operation of 100+ transistor silicon carbide integrated circuits," *Mater. Sci. Forum*, vol. 924, pp. 949–952, Jun. 2018, doi: 10.4028/www.scientific.net/MSF.924.949.
[32] P. G. Neudeck *et al.*, "Yearlong 500 °C operational demonstration of up-scaled 4H-SiC JFET integrated circuits," presented at the IMAPS Int. Conf. High Temperature Electron., Jun. 2018. [Online]. Available: https://doi.org/10.4071/2380-4491-2018-HiTEN-0000071
[33] P. G. Neudeck *et al.*, "Prolonged silicon carbide integrated circuit operation in Venus surface atmospheric conditions," *AIP Adv.*, vol. 6, no. 12, Dec. 2016, Art. no. 125119, doi: 10.1063/1.4973429.
[34] T. Kremic *et al.*, "Long-life in-situ solar system explorer (LLISSE) probe concept and enabling high temperature electronics," presented at the 48th Lunar Planetary Sci. Conf., Mar. 2017. [Online]. Available: https://www.hou.usra.edu/meetings/lpsc2017/pdf/2986.pdf
[35] T. Kremic *et al.*, "SAEVe: A concept study for a long duration small sat class Venus lander," presented at the 48th Lunar Planetary Sci. Conf., Mar. 2018. [Online]. Available: https://www.hou.usra.edu/meetings/lpsc2018/pdf/2744.pdf
[36] L. Chen *et al.*, "Sixty earth-days test of a prototype Pt/HTCC alumina package in simulated Venus environment," presented at the IMAPS Int. Conf. High Temperature Electron., Jun. 2018. [Online]. Available: https://doi.org/10.4071/2380-4491-2018-HiTEN-0000015
[37] *GEER*. Accessed: Oct. 1, 2018. [Online]. Available: https://geer.grc.nasa.gov

[38] D. Lucko *et al.*, "Chemical analysis of materials exposed to Venus temperature and surface atmosphere," *Earth Space Sci.*, vol. 5, pp. 270–284, May 2018, doi: 10.1029/2017EA000355.
[39] P. G. Neudeck, D. J. Spry, L. Chen, N. F. Prokop, and M. J. Krasowski, "Demonstration of 4H-SiC digital integrated circuits above 800 °C," *IEEE Electron Device Lett.*, vol. 38, no. 8, pp. 1082–1085, Aug. 2017, doi: 10.1109/LED.2017.2719280.
[40] *ABCs of Probes Primer*, Tektronix, Beaverton, OR, USA, 2016. [Online]. Available: https://info.tek.com/www-abcs-of-probes-primer.html
[41] D. Spry *et al.*, "Experimental durability testing of 4H SiC JFET integrated circuit technology at 727 °C," presented at the SPIE Defense Commercial Sens., Apr. 2016. [Online]. Available: https://doi.org/10.1117/12.2232926
[42] P. G. Neudeck *et al.*, "Experimentally observed electrical durability of 4H-SiC JFET ICs operating from 500 °C to 700 °C," *Mat. Sci. Forum*, vol. 897, pp. 567–570, May 2017, doi: 10.4028/www.scientific.net/MSF.897.567.

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