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# Opportunities and Challenges in Very High Frequency Power Conversion

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## Abstract—

**THIS** paper explores opportunities and challenges in power conversion in the VHF frequency range of 30-300 MHz. The scaling of magnetic component size with frequency is investigated, and it is shown that substantial miniaturization is possible with increased frequencies even considering material and heat transfer limitations. Likewise, dramatic frequency increases are possible with existing and emerging semiconductor devices, but necessitate circuit designs that either compensate for or utilize device parasitics. We outline the characteristics of topologies and control methods that can meet the requirements of VHF power conversion, and present supporting examples from power converters operating at frequencies of up to 110 MHz.

## I. INTRODUCTION

The need for power electronics having greater compactness, better manufacturability, and higher performance motivates pursuit of dramatic increases in switching frequencies. Increases in switching frequency directly reduce the energy-storage requirements of power converters, improving achievable transient performance and — in principle — enabling miniaturization and better integration of the passive components. Realizing these advantages, however, requires devices, passive components, and circuit designs that can operate efficiently at the necessary frequencies.

To achieve dramatic increases in switching frequency, it is typically necessary to mitigate frequency-dependent device loss mechanisms including switching loss and gating loss. Zero-voltage switching (e.g., [1]–[21]) can be used to reduce capacitive discharge loss and voltage/current overlap losses at the switching transitions. Likewise, resonant gating (e.g. [5], [8], [14]–[18], [20]–[24]) can diminish losses resulting from charging and discharging device gates, provided that the gate time constants are short compared to the desired switching transition times. In this paper, we will focus on designs compatible with zero-voltage switching and resonant gating

such that they can be scaled with good efficiency to very high switching frequencies<sup>1</sup>.

Section II of the paper explores frequency scaling of power converters, and examines how the physical sizes of magnetic components change with increasing frequency for different design options. We provide quantitative examples of magnetics scaling, and also point to opportunities in VHF magnetics design. Section III of the paper explores the impacts of frequency scaling on semiconductor devices, circuit topologies, and control methods. We present an overview of the design of power electronics at extreme high frequencies, and explore how device losses and operating requirements influence topology and control. We also point out some of the approaches being taken to develop improved power converters at these frequencies. Section IV of the paper presents experimental examples illustrating the opportunities and tradeoffs in VHF power conversion. A first example compares a resonant boost converter operating at 110 MHz to a conventional PWM converter operating at 500 kHz, while a second example shows how size and performance of a resonant dc-dc converter change when the design frequency is changed. Finally, Section V concludes the paper.

## II. FREQUENCY SCALING OF POWER CONVERTERS

Consider how a power converter could be redesigned to preserve the voltage and current waveform shapes, but with the waveforms scaled in time and amplitude to yield a new frequency and power level. Treating the system as a switched linear network, and defining scaling factors  $k_v$ ,  $k_i$ , and  $k_f$  for circuit voltages, currents, and frequency:

$$\begin{aligned} v_{\text{new}} &= k_v v_{\text{old}} \\ i_{\text{new}} &= k_i i_{\text{old}} \\ f_{\text{new}} &= k_f f_{\text{old}} \end{aligned} \tag{1}$$

<sup>1</sup>We note that in some portions of the design space (e.g., low-voltage, low-power converters [25]–[28]) it is possible to achieve quite high switching frequencies with hard-switched, hard-gated converter designs (e.g., owing to the properties of low-voltage CMOS processes [29]). Nevertheless, for other voltage and power levels of interest, VHF operation typically necessitates resonant switching and/or gating.

then it is straightforward to show that the circuit powers and component values scale as:

$$\begin{aligned} p_{\text{new}} &= k_i k_v p_{\text{old}} \\ C_{\text{new}} &= \frac{k_i}{k_v k_f} C_{\text{old}} \\ L_{\text{new}} &= \frac{k_v}{k_i k_f} L_{\text{old}} \\ R_{\text{new}} &= \frac{k_v}{k_i} R_{\text{old}} \end{aligned} \quad (2)$$

Following this scaling for all circuit elements, the waveform shapes scale as desired in amplitude and time, and circuit efficiency remains unchanged.

For operation at the same voltage and current levels but at a factor  $k_f$  higher in switching frequency, circuit resistances remain unchanged, while capacitor and inductance values scale inversely with frequency (by a factor  $1/k_f$ ). This inverse scaling of passive component values and energy storage with switching frequency, along with the proportionate increase in achievable control bandwidth, clearly motivate use of higher switching frequencies.

What is less clear — and what we examine as part of this work — is how the achievable sizes of the passive components change with frequency when practical constraints are taken into account. We focus on magnetic components, as they are the most challenging to scale to high frequencies and small sizes, and because they typically dominate the size of power electronic systems. Moreover, we restrict our discussion to scaling of ac inductors (e.g., for resonant operation), both because this is representative of scaling in many magnetic components, and because resonant circuit designs using such magnetics are often suited for extreme high frequency operation, as described in Section III.

#### A. Scaling of Magnetics

When inductance values are scaled inversely with switching frequency, the effective impedance levels provided remain unchanged as a design is scaled. How the *size* of an appropriate magnetic component scales, however, is a much more complex question, encompassing the dependence of winding loss [30]–[34], core loss and permeability [33]–[40], and heat transfer [40]–[42] on size and frequency. Size and frequency scaling of magnetic components has been considered in a variety of works: [33] considers how the quality factor of an inductor at a given frequency scales with linear dimension for various loss cases. Reference [34] examines scaling of transformer parameters and performance with size and frequency under heat transfer limits, while [42] shows how achievable transformer size varies with frequency under efficiency and heat transfer limits. Reference [43, Ch. 15] provides a transformer design algorithm including core loss and simplified winding loss, and explores via a design example how transformer size scales with frequency. Reference [40] explores power density limits of inductors vs. frequency, considering core loss and heat transfer limitations. These references reveal that there are often limitations in scaling down the size of magnetic

components, even if frequency is increased arbitrarily. Nevertheless, as illustrated below, considerable reduction in the size of magnetic components is possible through frequency scaling if appropriate materials and designs are employed.

In keeping with the goals of this paper, we examine how the size of ac (e.g., resonant) inductors scale with operating frequency considering both efficiency (e.g., quality factor) and temperature constraints. We focus on single-layer-winding designs, and consider use of high-permeability ferrite materials, low-permeability rf materials, and coreless designs.

1) *Cored Inductor Scaling*: There are two major loss mechanisms associated with a cored resonant inductor, core loss and winding loss. We model core loss  $P_{\text{core}}$  using the classical power law or “Steinmetz” model:

$$P_{\text{core}} = V_{\text{core}} C_M f^\alpha B_{ac}^\beta \quad (3)$$

where  $V_{\text{core}}$  is the core volume,  $f$  is the operating frequency,  $B_{ac}$  is the sinusoidal ac flux density in the core and  $C_M$ ,  $\alpha$  and  $\beta$  are parameters chosen to fit the model to measured loss data. For typical ferrite materials,  $\alpha$  is in the range of 1.4-2.0 and  $\beta$  is in the range of 2.4 - 3.0 where specific parameters may need to be selected for a particular frequency range [44]. For a single-layer winding in the skin-depth limit we use a simple model for winding loss  $P_w$ :

$$P_w = \frac{1}{2} I_{ac}^2 R_{ac} = \frac{1}{2} I_{ac}^2 \frac{\rho l_w}{w_w \delta} = \frac{1}{2} I_{ac}^2 \frac{l_w}{w_w} \sqrt{\pi \rho \mu_0 f} \quad (4)$$

where  $I_{ac}$  is the sinusoidal ac current amplitude,  $\rho$  is conductor resistivity,  $l_w$  is the length of the winding,  $w_w$  is the effective width of the conductor, and  $\delta$  is the skin depth, which is inversely proportional to frequency. In this model, we neglect gap fringing effects [45], [46].

Consider how the achievable size of a resonant inductor scales with frequency when the inductive impedance is held constant and equivalent ac series resistance is held constant. This results in a required inductor quality factor  $Q$  (and loss) that is independent of frequency. In carrying out our scaling experiment, we start with an inductor having an optimized design for a given frequency (winding, core geometry and gap). To scale the design in size, we allow the core geometry to change proportionally in all linear dimensions (keeping the core geometry constant), including the gap, but allow the number of turns to vary (distributed in a single layer in the scaled winding window, thus changing  $w_w$ ). In scaling to a new frequency we seek the smallest design that meets both the impedance and quality factor requirements.

If the size was held constant while frequency was increased by a factor  $k_f$ , the winding loss could be held constant by decreasing the number of turns by a factor  $k_f^{0.25}$ , based on (4). If we adjust the gap to keep the inductive impedance constant, flux density scales down by  $k_f^{0.75}$ . Core loss then scales as  $k_f^{\alpha - 0.75\beta}$ . If  $\alpha < 0.75\beta$ , core loss, and thus total loss, decrease. We can see that it is then possible to reduce the size, which will incur a loss penalty, and return to the original total loss. Ideally the gap length and number of turns would be re-optimized at the same time to maximize the size reduction.

However, if  $\alpha > 0.75\beta$ , core loss increases if frequency is scaled up and impedance and winding loss are held constant. In this case, size needs to be increased in order to maintain the original total loss.

In principle, the size can either scale up or down with frequency, depending on the material parameters. In practice, the values of  $\alpha$  and  $\beta$  that provide a good fit to core-loss data vary as a function of frequency:  $\alpha$  becomes larger at high frequency and  $\beta$  stays approximately constant or decreases [44]. Thus, at sufficiently high frequency, the improvements from scaling frequency cease and then reverse, so there is a limit to the amount that frequency scaling can be used to reduce inductor size.

To demonstrate this effect, we carry out a numerical design experiment. The resonant inductor design to be scaled realizes an impedance of  $62.8 \Omega$  (i.e.  $100 \mu\text{H}$  at  $100 \text{ kHz}$ ) at  $Q = 100$  for  $1 \text{ A}$  ac current. We use a numerical search to optimize designs based on 3F3 core material and scaled RM-type cores. The optimization is based on the assumptions introduced above, but additionally limits core flux density to below  $0.3 \text{ T}$  and considers only integer numbers of turns. The “ $Q$  limited” curve of Fig. 1 shows the numerical optimization results and inductor “box” volume<sup>2</sup> vs. design frequency. The scaled inductor design achieves its minimum size at around  $300 \text{ kHz}$ , and beyond about  $800 \text{ kHz}$  the inductor volume increases drastically, with its minimum volume being approximately  $2.5 \text{ cm}^3$ . Also shown for comparison are results for a separate CAD optimization which uses discrete, standard RM cores, wire sizes and gaps (with 3F3 material), incorporates multi-layer windings, and accounts for skin and proximity effect and core thermal limits. Results from this alternative optimization match well given differences in the design limits, and yield identical conclusions. We note that these results are qualitatively similar to those found for transformers in [42], [43, Chap. 15], underscoring the limitations of frequency scaling in cored designs.

It should be noted that there are also other constraints in miniaturization under frequency scaling. In the previous discussion, it is assumed that the inductor loss budget is the limiting factor for achieving a minimum volume. In addition to meeting a quality factor requirement, imposing a temperature rise limit on a given inductor may further increase its minimum achievable volume. In order to study how the volume of an inductor scales with a temperature rise constraint, a thermal model is first developed. Among the three heat transfer mechanisms (convection, conduction and radiation), the heat flow is proportional to surface area (of which the units are linear dimension squared) for convective and radiative heat transfer, whereas the heat flow through conduction is proportional to linear dimension if the dimensions of all structures are scaled together. To form a conservative estimate at small scales, it is safe to assume that heat flow is at least proportional to

<sup>2</sup>“box volume”, as illustrated in [42], is the volume of the smallest box that the inductor could fit inside.

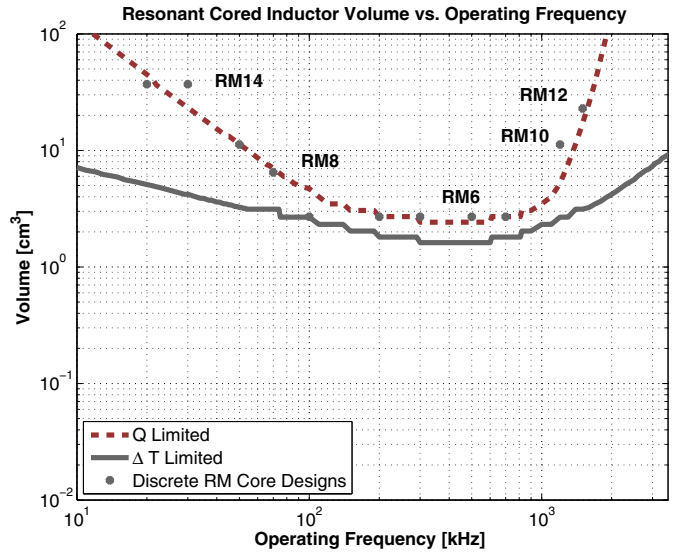


Fig. 1. Numerical optimization results of inductor “box” volume vs. design frequency for an example resonant inductor.

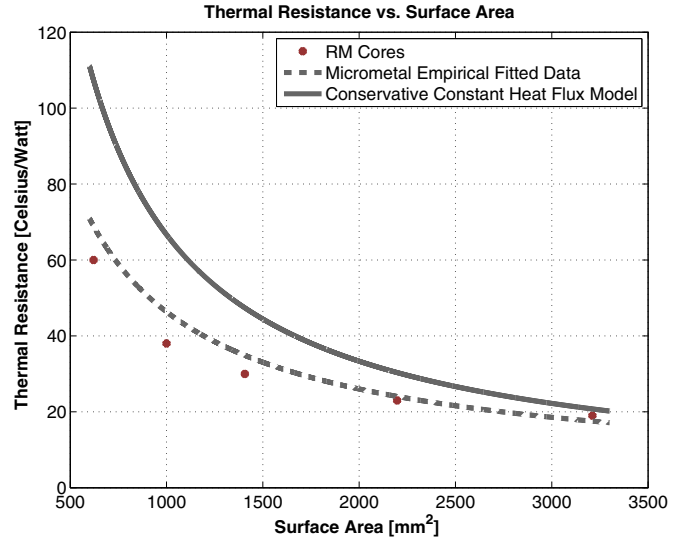


Fig. 2. Thermal resistance vs. surface area for different data and models.

the surface area and temperature rise, which corresponds to a constant heat flux limit for a given temperature rise.

By matching the thermal resistance vs. surface area for this constant heat flux model with discrete data points for RM type ferrite cores and an empirically-fitted curve for toroidal Micrometals cores [47], as shown in Figure 2, we arrive at a heat flux limit of  $6.7 \text{ mW}/(\text{C} \cdot \text{mm}^2)$ . This thus represents a thermal model which is quite conservative at small scales.

With this thermal model, a temperature limit of  $40 \text{ C}$  is imposed on the previous inductor design (i.e.  $62.8 \Omega$  at  $1 \text{ A}$  ac current on a scaled RM core using 3F3 material). This “ $4 \text{ T}$  limited” curve of Fig. 1 plots the minimum size of an inductor that meets this temperature requirement without consideration of  $Q$ . As shown in Fig. 1, the design meets both  $Q$  and thermal requirements and is not limited by the maximum temperature

rise constraint, as the minimum achievable volume for a given temperature rise lies below the constant loss budget curve at all frequencies. In other possible designs, however (e.g., designs in which a lower  $Q$  requirement is imposed), both of these constraints would be important, with an allowed design being on the maximum of the two curves.

As shown in Fig. 1, resonant inductors constructed with conventional high permeability MnZn and NiZn ferrite materials, such as 3F3 and 3F4, are typically effective only up to a few megahertz, beyond which the volume must increase drastically to meet a given quality factor requirement. Introduction of low permeability rf materials (with several examples explored in [48]) extends the frequency range for which cored inductors are useful up to many tens of megahertz. However, core loss still imposes a fundamental frequency limit in minimizing size in resonant cored inductors built with rf materials, and there still exists an optimal frequency beyond which the inductor size increases in order to stay within a loss constraint.

To demonstrate the efficacy of low-permeability RF materials, we simulate and optimize inductor designs for the same requirements (62.8  $\Omega$  inductive impedance, 1 A ac current, a minimum  $Q$  of 100 and a maximum temperature rise of 40  $^{\circ}\text{C}$ ), using toroids of P-type material ( $\mu = 40$ ) from Ferronics. The inductors designs are optimized based on a polynomial fit to the available core loss data [48] for P material and various toroidal core sizes [49]. Figure 3 illustrates that the box volume for inductors designed with P material is minimized near 30 MHz, with an achievable minimum size of

1.5  $\text{cm}^3$ . Unlike the previous case, the minimum size in this example is limited by temperature rise. Figure 3 shows that, compared to designs with a conventional high-permeability material (i.e., 3F3), designs using an RF material (P) enables an approximate 40% reduction in volume to be achieved, along with a reduction of energy storage and increase in frequency by a factor of 100. In other cases (e.g., higher temperature rise designs) the relative advantage of the rf material would be even much larger.

2) *Coreless Inductor Scaling: General Analysis:* Core loss imposes fundamental frequency limits associated with minimizing size in cored resonant inductors. Since winding loss is the only major loss mechanism for a coreless design, coreless designs may offer a much better tradeoff between a given loss budget and volume at higher frequencies.

In general, the inductance of a tightly-coupled magnetic structure can be expressed as being proportional to a linear dimensional scaling factor  $\varepsilon$ :

$$L = \frac{N^2 \mu A_l}{l} \propto N^2 K \varepsilon \quad (5)$$

Consider a single-turn inductor: its inductance is directly proportional to the linear dimension factor  $\varepsilon$  (6), and its dc resistance is inversely proportional to  $\varepsilon$  (7):

$$L = K_1 \varepsilon \quad (6)$$

$$R_{DC} = \frac{\rho l}{A_w} = \frac{K_2}{\varepsilon} \quad (7)$$

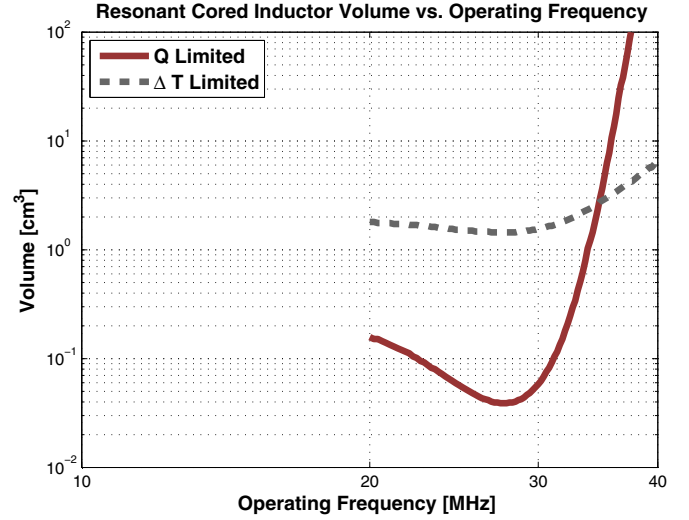


Fig. 3. Resonant inductor volume comparison. The use of the rf material enables a 40% reduction in volume as compared to using 3F3 material for this scaling example.

For ac resistance in the skin depth limit, the dependency on linear dimension is exchanged for a dependence on the square root of frequency:

$$R_{AC} = \frac{d}{\delta} R_{DC} = K_3 \sqrt{f} \quad (8)$$

For a closely-linked N-turn inductor, inductance, dc resistance and ac resistance are all merely scaled by number of turns squared.

$$L = N^2 K_1 \varepsilon \quad (9)$$

$$R_{DC} = \frac{N^2 K_2}{\varepsilon} \quad (10)$$

$$R_{AC} = N^2 K_3 \sqrt{f} \quad (11)$$

In order to scale an inductor design across frequency maintaining constant impedance and constant loss, we can first find the dependence of the quality factor on the linear scaling factor  $\varepsilon$  and on frequency

$$Q = \frac{2\pi f L}{R_{AC}} = \frac{2\pi f N^2 K_1 \varepsilon}{N^2 K_3 \sqrt{f}} = K_4 \varepsilon \sqrt{f} \quad (12)$$

The quality factor is directly proportional to  $\varepsilon$  and to the square root of frequency. Thus, to achieve a given impedance and quality factor as frequency is varied, an inductor's linear dimension can be scaled as  $f^{-1/2}$ , which in turns means that the volume of the inductor scales as  $f^{-3/2}$ .

If quality factor were the only limiting factor, the required volume of a coreless inductor could be continuously reduced as  $f^{-3/2}$  as frequency increases. However, as the inductor volume (and surface area) gets smaller and smaller for a given loss, the inductor will eventually encounter its thermal (temperature rise) limit. From the thermal model developed in the previous section, imposing a temperature limit is equivalent to limiting heat flux through the inductor surface. Under this model, there are two ways through which the temperature

rise can be decreased: reducing the loss and/or increasing the surface area. From (12), the quality factor is shown to be proportional to the linear scaling factor  $\epsilon$ . If the thermal model is combined with (12), the volume of a coreless inductor under a heat flux limit scales with  $f^{-1/2}$ :

$$4 T = k \frac{P_{diss}}{\text{Area}_{\text{Surface}}} = \frac{k}{\text{Area}_{\text{Surface}}} \frac{I_{RMS}^2 Z}{Q} = k_2 \frac{I_{RMS}^2 Z}{\epsilon^3 f} \quad (13)$$

Therefore, even in the heat flux (thermally) limited case, the volume of an air-core inductor can still be made smaller with increasing frequency. Furthermore, the quality factor of the inductor in the heat-flux-limited scaling actually improves as  $f^{1/3}$ . This scaling can be maintained so long as at least one turn or more is required for the desired impedance at the specified scale. (Scaling can still be achieved beyond this point in some cases, but necessitates changes in geometry.)

3) *Coreless Inductor Scaling: Solenoid Example:* For a single layer coreless solenoid inductor, a good empirical model is available based on Medhurst's work [50]–[52], [53, Chapter 6]. In Medhurst's model, quality factor  $Q$  is directly proportional to the diameter of a solenoid, square root of frequency and another factor  $\Psi$ , where  $\Psi$  is a function of length  $l$  to diameter  $D$  of the solenoid and wire diameter to wire spacing:

$$Q \approx 7.5 D \Psi \sqrt{f} \quad (14)$$

$$\Psi_{\text{optimum}} = 0.96 \tanh \left( 0.86 \sqrt{\frac{l}{D}} \right) \quad (15)$$

$$\frac{l}{D} = 5, \Psi_{\text{optimum}} \approx 0.88 \quad (16)$$

To achieve maximum  $Q$  for a solenoid inductor, this model maintains the aspect ratio of the length to diameter of the inductor to be at least 5, which is consistent with our assumption of maintaining an optimal design by holding the relative geometry constant as we scale designs.

A CAD optimization of solenoid inductors based on Medhurst's formulation is shown in Fig. 4 to illustrate how the coreless resonant inductors scale with frequency. The same operating conditions are applied as were used for the cored resonant inductors. Initially, when temperature rise is not a limiting factor, we see that the inductor box volume scales as  $f^{-3/2}$ , and once the temperature rise becomes the major constraint, the inductor volume falls off at a slower rate, with  $f^{-1/2}$ , which is precisely what the previous analysis predicts.

Figure 4 also shows the previous simulation predictions for inductor box volumes with the conventional high permeability magnetic material (Ferroxcube 3F3), and the low permeability RF material (Ferronics P) and a coreless structure under the same operating conditions and constraints. This comparison is somewhat limited by the fact that the solenoid design is magnetically unshielded, while the other two designs are largely shielded. Nevertheless for a given maximum loss budget and temperature rise limit, there is always a frequency beyond which a coreless inductor will outperform any cored inductor. What design strategy is best depends on the design

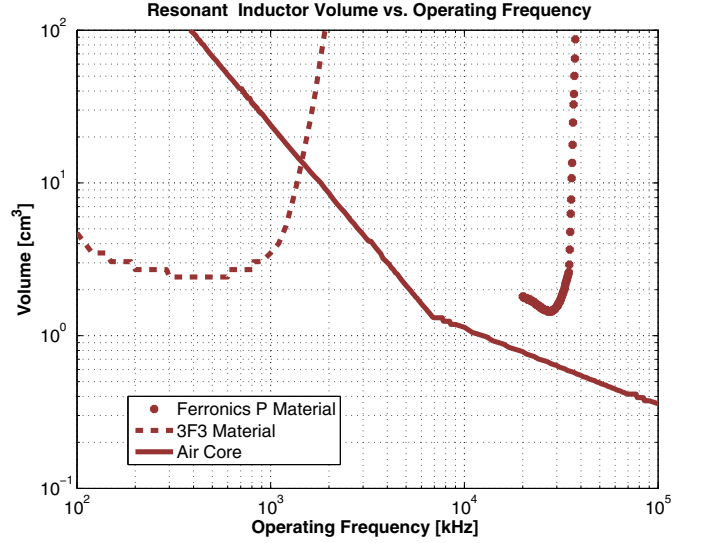


Fig. 4. Comparison between conventional magnetic material (3F3), RF material (P) and coreless inductor volume.

specifics, but it is clear that both low-permeability designs and coreless designs can be advantageous.

4) *Magnetics Analysis: Summary:* From the above analysis, we can see that cored ac inductors always have a frequency limit in terms of achieving miniaturization with increased operating frequency. Nevertheless, it is shown that significant improvements in size can be achieved by moving to VHF frequencies if low-permeability RF magnetic materials are employed. It should be noted that the design of magnetic components with low-permeability RF magnetic materials is relatively poorly understood as compared to design with conventional materials. This represents a significant opportunity for improved designs at VHF frequencies.

Moreover, the above analysis indicates that with coreless designs we can always achieve significant benefits in size, required energy storage, and magnetics loss by scaling up in frequency, provided sufficiently high frequencies can be obtained within other constraints. Likewise, there is opportunity to gain still greater benefits through improved design and fabrication of coreless magnetic structures and with magnetic structures better suited to extreme high frequencies (e.g. [54], [55]).

### III. DEVICES, TOPOLOGIES, AND CONTROL

As described in Section II, frequency scaling offers tremendous opportunities to improve passive component size if losses and other limitations can be dealt with. In this section we show how moving to greatly increased frequencies impacts semiconductor devices, circuit topologies and controls. We first review how frequency scaling impacts device requirements, and outline emerging opportunities in devices for high frequency operation. We then show how these considerations impact the design of power electronics at VHF, and highlight some topology and control approaches for addressing the challenges that arise at these frequencies.



1) *Semiconductor Device Considerations*: In scaling converter switching frequency, two characteristics emerge to dominate device considerations: parasitic resistance and parasitic capacitance. The introduction to Section II posits that for scaling frequency at constant efficiency, circuit resistances should remain constant while capacitances scale inversely with frequency. However, this scaling cannot be maintained at frequencies where device capacitances are important contributors to circuit capacitance, as device resistance and capacitance are not independent. Rather, achieving a desired on-state resistance,  $R_{DS\ on}$ , in a given material system and process requires some minimum device geometry — the effective width, in particular — with a total area that is layout dependent. Associated with this geometry are area- and perimeter-dependent parasitic capacitances that result in net capacitances among all device terminals (e.g.,  $C_{ds}$ ,  $C_{dg}$ , and  $C_{gs}$  in a discrete MOSFET). In some cases, these capacitances can be sufficiently represented by an effective device input capacitance,  $C_{ISS}$ , and output capacitance,  $C_{OSS}$ . Importantly for VHF operation, each of these capacitances also includes some equivalent series resistance. These device parasitic resistances and capacitances result in loss mechanisms that determine device performance at VHF.

To elucidate the device loss behavior in VHF converters under soft switching and gating, we consider how loss scales with operating frequency *for a given semiconductor device*. This is not the same as optimizing the device as a function of frequency, but it does illustrate the loss considerations. For a typical resonant VHF application, achieving soft switching requires controlling the impedance across the switch output port when the switch is off. An external snubbing capacitance  $C_{ext}$  is often placed across the switch (in parallel with the switch output capacitance) to achieve a specified impedance in the circuit design. We assume that the external capacitance is reduced as frequency is increased such that the scaling law of (2) can be followed for the net output capacitance<sup>3</sup>. For the switch input port there is typically no external capacitance. Consequently, we do not precisely follow the scaling of (2) in this regard, but assume that sufficient gate current is provided to maintain the desired (frequency scaled) gate voltage waveform.

Now consider the simplified device model of Fig. 5. It includes the parasitic components that determine loss in a discrete MOSFET where we simplify the physical model by neglecting the details of coupling from the output port back to the input port through  $C_{gd}$ . The resistances,  $R_{DS\ on}$ ,  $R_{OSS}$ , and  $R_G$  correspond to the three important VHF device loss mechanisms: conduction loss, displacement loss, and gating loss.  $C_{ISS}$  and  $C_{OSS}$  are the lumped input and output capacitances, and  $C_{EXT}$  is the snubbing capacitance utilized to obtain the desired drain-source impedance when the switch is off. If we observe the scaling described above — that the

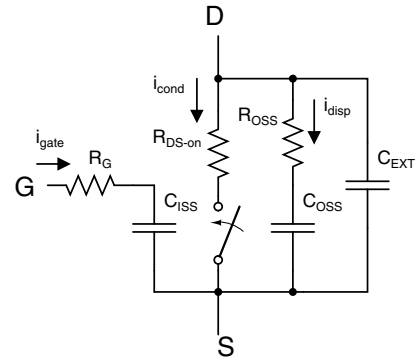


Fig. 5. Simplified device model

TABLE I  
DEPENDENCE OF DEVICE LOSS MECHANISMS ON DEVICE PARAMETERS  
AND FREQUENCY SCALING

Mechanism	Device Dependence	Frequency Dependence
Conduction Loss	$\propto R_{DS\ on}$	Independent
Displacement Loss	$\propto R_{OSS} C_{OSS}^2$	$\propto f_s^2$
Gating Loss	$\propto R_G C_{ISS}^2$	$\propto f_s^2$

desired gate and drain voltage waveform shapes are maintained with frequency scaling — it is straightforward to understand how each loss scales with frequency. First, conduction loss remains independent of frequency because  $R_{DS\ on}$  is not frequency dependent and thus the RMS of  $i_{cond}$  will not change. However, both  $i_{disp}$  and  $i_{gate}$ , the currents associated with displacement loss and gating loss, flow in branches where the impedance is dominated by capacitance. Therefore, as frequency increases the impedance falls and the currents must rise proportionally. We then see that both displacement loss and gating loss rise with the square of frequency<sup>4</sup>. It is also important to note that for a given frequency, scaling the device capacitances causes a linear increase in  $i_{disp}$  and  $i_{gate}$ . Thus displacement and gating loss also have a square-law dependence on capacitance. The loss mechanisms, and their dependence on device parameters and frequency scaling are summarized in table I.

In recognizing that device loss includes terms which depend on the square of frequency and capacitance, it becomes clear that there are significant opportunities for improving VHF power conversion through semiconductor device improvements. A search for devices suitable for VHF power conversion often turns up RF power MOSFETs intended for use in linear power amplifiers (e.g., [14], [56]). While these devices can be successfully employed in VHF power conversion, their optimization criteria (e.g., for linearity) may not realize the best performance for power conversion achievable in the underlying semiconductor process. The same can be said of devices intended for switching converters. Here, the figure of merit has often been driven by considering conduction loss

<sup>3</sup>Above a certain frequency, no external capacitance remains, and one must either operate with more capacitance than desired or reduce device area, thus increasing  $R_{DS\ on}$ . For simplicity, we do not consider this case though it can often occur in practice.

<sup>4</sup>Note that in many hard-gated designs gate loss rises only linearly with switching frequency because the switching transition speed is not scaled up proportionately with switching frequency.

and overlap loss during switching [57]. Yet, in soft-switched designs, switching loss is often insignificant.

Where the interest is in pushing frequency upwards, any optimization must consider displacement and gating loss along with switching and conduction loss. This has been borne out in experiment. In a standard silicon LDMOS process, optimization of the layout and exploitation of safe operating area constraints (made possible by the nature of soft-switched VHF conversion) yielded VHF optimized devices that reduced loss by 57% over reference devices designed conventionally using hard-switched criteria [58]. More aggressive improvements may be possible by refocusing optimization to the process level.

New power devices in material systems other than silicon similarly hold great potential. This is primarily because a reduction in device capacitance gives way to a proportional increase in switching frequency with no loss penalty if parasitic resistance is held constant. RF and power devices in SiC and GaN are both active areas of research and development. Such devices benefit from greatly enhanced carrier mobility. This allows smaller devices at a given  $R_{DS\ on}$ , and in turn, smaller capacitances. Table II compares a representative silicon LDMOS device having excellent VHF performance with a newly developed GaN HEMT. Both share similar  $R_{DS\ on}$ , though  $R_{OSS}$  and  $R_G$  are somewhat higher in the GaN device. We see that the input and output capacitances of the GaN device are substantially smaller, so the  $RC^2$  products are much smaller. Thus, the GaN device can operate at a much higher frequency. Development of GaN devices optimized for VHF switching converter operation could offer even greater improvement.

2) *Design of VHF Power Conversion Systems:* The considerations introduced above impose requirements on circuit topologies for extreme high frequency operation. Because the RC products of the semiconductor devices cannot be arbitrarily reduced, one cannot follow the design scaling in (2) beyond a certain point. To keep conduction losses limited, one is forced to operate with an increasing excess of capacitance as frequency is increased. It is precisely to reduce the losses associated with excess device input and output capacitance that the use of resonant gating and switching become important at high frequencies. More generally, topologies that can effectively absorb substantial device capacitance as part of their operation while maintaining high efficiency are better suited to scaling to high frequencies than topologies that cannot do so. Likewise, for given physical device sizes, interconnect inductances become a higher percentage of the element impedance as frequency is raised. Therefore, topologies that can effectively absorb substantial parasitic inductance as part of their operation are better suited to scaling to high frequencies than those that cannot do so. To be effective at extreme high frequencies, a circuit topology should have both of these characteristics to some degree.

A further consideration in topologies for VHF power conversion relates to the practicality of driving the active switches. Topologies in which switch control ports are referenced to

“flying” circuit nodes are ill-suited to extreme high frequencies, due to the challenges of level shifting and of providing good drive waveforms in the face of parasitic capacitances to the flying nodes. Consequently, circuit topologies having ground-referenced active switches are generally preferred at very high frequencies.

With these considerations in mind, a VHF dc-dc converter topology typically comprises a resonant inverter having common-referenced switches (e.g., [21], [59]–[65]) coupled to a resonant rectifier (e.g., [66]–[68]) as illustrated in Fig. 6. The network interconnecting the two provides some combination of filtering, isolation, and voltage transformation (e.g., via a transformer or matching network [69], [70]). The system is often structured to absorb device, component, and interconnect parasitics. Many such converters dominantly process power through the switching-frequency components of voltage and current, though some designs may transfer power directly at dc (e.g., [17]) and/or at harmonics of the switching frequency.

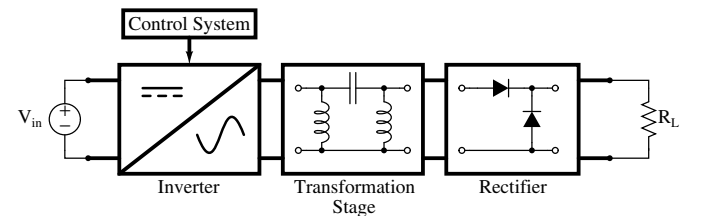


Fig. 6. Structure of a typical VHF dc-dc converter.

While high-frequency resonant dc-dc converters often topologically resemble their hard-switched counterparts (e.g., [7], [10], [17], [19], [20], [56]) many of their practical characteristics can be quite different. One major challenge in the design of VHF power converters is achieving high efficiency over a wide load range. PWM control at the switching frequency is not generally practical, owing to the resonant nature of the power and/or drive stages, so methods such as frequency control and phase-shift control have traditionally been applied. Unfortunately, as illustrated in [1], [3], [4], [10], [11], [13] it is difficult to maintain high efficiency over a wide load range in resonant converters using such techniques alone. This is in part because the losses associated with continuously providing zero-voltage switching opportunities and resonant gating do not scale back with load power, yielding a decline in efficiency at light loads.

A method for addressing this challenge in VHF converters is to separate the energy conversion function from the regulation function of the converter [14]. One approach for doing this is to design the converter for full load power and regulate average delivered power (and consequently output voltage) by modulating the entire converter on and off at a modulation frequency that is far below the switching frequency. In this strategy, which has been successful in a variety of designs [14]–[17], [19], [20], [56], [71], [72], the power stage magnetics are sized for the very high switching frequency, while input and output capacitors and filters are sized for



TABLE II  
COMPARISON BETWEEN SI-LDMOS AND GAN HEMT VHF DEVICES

Part No.	Desc.	$R_{DS}$	$R_G$	$C_{ISS}$	$R_{OSS}$	$C_{OSS}$	$V_{br}$
MRF6S9060	Si LDMOS	175 m $\Omega$	135 m $\Omega$	110 pF	170 m $\Omega$	50 pF	68 V
CGH40045	GaN HEMT	200 m $\Omega$	?	19 pF	1 $\Omega$	8.3 pF	100 V

the lower modulation frequency<sup>5</sup>. Because the power stage only incurs gating and resonating losses when active, converter losses scale more closely with power, yielding good efficiency over a wide load range. Moreover, through partitioning the energy conversion and regulation functions in this manner, one can better optimize the VHF power stage design. Other approaches for addressing the operating and control limitations of very high frequency converters are described in [14], and we anticipate that still better approaches will emerge as technology in this area develops.

A second challenge in the design of VHF power converters is maintaining good performance across wide input and output voltage ranges. This is difficult for two main reasons. First, given constant load impedance, a resonant inverter operating at fixed switching frequency and duty ratio has currents and voltages that each scale proportionally to input voltage and delivers power as the square of the input voltage. Since duty ratio is typically fixed in VHF designs, a wide input voltage range tends to correspond to a wide range of peak current and voltage stresses in the circuit. Thus, the circuit must be sized to deliver the desired power at the minimum input voltage, and still endure the stresses at the maximum input voltage. This does not compare favorably to conventional PWM converters, where duty ratio variations partially compensate the variations in stresses across the input voltage range. Second, the effective ac-side impedance presented by a rectifier tends to vary with output voltage and input power (and hence input voltage) [15], [16]. This can be problematic for wide-voltage-range operation since many RF inverter topologies are highly sensitive to load impedance variations, and may lose soft-switching behavior for large variations.

Some means of addressing the challenges of wide-voltage-range operation are available. First, some resonant inverters (e.g., [73]) can be designed to have good tolerance for load impedance variations. For inverters that are sensitive to load variations, special matching networks — termed resistance compression networks [16] — can be used to greatly reduce the apparent impedance variation seen by the inverter as operating conditions change. Moreover, by careful selection of the nonlinear characteristics of the rectifier impedance in conjunction with the inverter and interconnect network design, power and device stress variations can be at least somewhat reduced over the input and output voltage range. Using these techniques, designs capable of up to 2:1 input voltage and 3:1 output voltage range have been demonstrated [20]. Further-

more, the authors believe that there is substantial opportunity to develop topologies and designs offering still much better characteristics across wide voltage ranges.

A third challenge in the design of VHF power converters is that many existing topologies for high-frequency conversion have relatively high component stresses. The “square wave” PWM topologies often employed at conventional frequencies do have some underlying advantages in this regard. For example, while resonant converters typically process power only through the fundamental components of voltage and current, PWM converters also transfer energy at dc and/or harmonic frequencies, leading to relatively lower component stresses. Nevertheless, many of the perceived limitations of VHF topologies are not fundamental. Rather, VHF conversion has simply received much less attention than more conventional approaches, and many high-frequency designs have been adapted directly from RF communications applications, where considerations such as spectral content are more important than efficiency.

It should be noted that recent developments in high-frequency converter technology are starting to address the component stress limitations of earlier approaches. For example, the inverter topologies of [62], [64], [65], [73], [74] have lower voltage and/or current stress than traditional designs, leading to dc-dc converters having improved performance (e.g., [17], [21], [75]). Moreover, as may be inferred from recent work (e.g., [14], [75]), it is possible to offset the limitations of available topologies and take advantage of the underlying strengths of VHF circuit topologies through development and adoption of appropriate system architectures. These works represent only first steps towards improved operation at VHF frequencies. There is tremendous opportunity to develop new circuit, device, and component technologies that can dramatically improve the performance of power electronics at extreme high frequencies. We conclude that VHF power conversion is currently in its infancy, and with continued research promises levels of miniaturization, integration, and performance that are simply unattainable at lower frequencies.

#### IV. EXAMPLES

##### A. Conventional hard-switched boost vs. VHF resonant design

The previous discussions underscore the potential size and performance advantages of resonant power converters operating at extreme high switching frequencies. To illustrate the opportunities and tradeoffs of this approach, we compare a 110 MHz resonant boost converter [17] with a conventional PWM boost converter operating at 500 kHz. Power stage schematics for the two designs are shown in Fig. 7, and

<sup>5</sup>We note that circuit topologies that do not incorporate bulk magnetics or “chokes” — such as those in [17], [19]–[21], [60], [61], [65], [73] — are particularly well suited to this control approach because of the fast response due to their low energy storage.

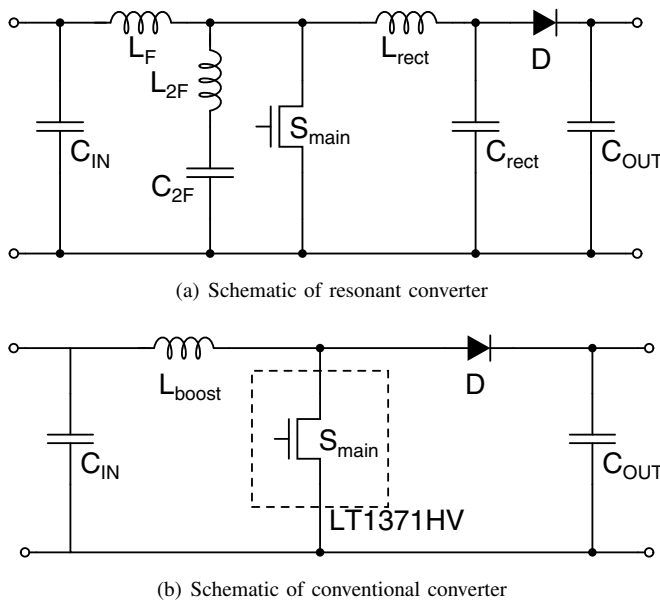


Fig. 7. Schematic drawings of the resonant and conventional boost converters.

key component values and types are listed in Table III. Both converters are designed to regulate a 32.4 V output at up to 18 W load across an input voltage range of 11-16 V. The 110 MHz converter, described in detail in [17], [76], incorporates many of the design approaches described in the previous sections, including resonant ZVS switching and gating, waveform shaping and parasitic absorption, and on-off control of the output voltage. The 500 kHz converter is based on the LT1371HV switching regulator by Linear Technology, and uses an unshielded 10  $\mu$ H inductor (Coilcraft DO3316T-103M). In each case the input capacitance is 22  $\mu$ F and the output capacitance is 75  $\mu$ F<sup>6</sup>.

Figure 8 shows the efficiency for each converter at a nominal input voltage of 15 V. The efficiency of the 110 MHz resonant converter ranges from about 81% to 87% for operation from 5% to full load, while efficiency of the conventional converter ranges from about 74% to 89% over the same load range. It can be seen that the conventional converter is slightly more efficient near full load, while the resonant converter is significantly more efficient at lighter loads, due to its effective use of on-off control. This clearly indicates that the efficiency of very high frequency converters can be competitive with conventional designs, and can maintain good efficiency down to light loads if appropriate design and control methods are used.

Table IV shows the masses and volumes of the passive components of the two converters. It can be seen that while the capacitor volumes of the two circuits are nearly identical, the magnetics volume of the resonant converter is less than one fourth of that of the conventional converter, and the magnetics

<sup>6</sup>For the resonant converter an additional 34 nF of ceramic capacitance was used to suppress the 110 MHz ripple. This was not required for the conventional converter, and was therefore not used in that design. The comparison in table IV includes this additional volume and weight for the resonant converter.

TABLE III  
COMPONENT VALUES FOR BOOST CONVERTER POWER STAGES.

Resonant Design		
Component	Value	Type
$L_F$	33 nH	Coilcraft 1812SMS
$L_{2F}$	12.5 nH	Coilcraft A04TG
$L_{rect}$	22 nH	1812SMS
$C_{2F}$	39 pF	ATC100A
$C_{rect}$	10 pF	ATC100A
$C_{out}$	75 $\mu$ F	Multilayer Ceramics
$C_{in}$	22 $\mu$ F	Multilayer Ceramics
$S_{main}$		Freescale MRF6S9060
$D$		Fairchild S310
Conventional Design		
Component	Value	Type
$L_{boost}$	10 $\mu$ H	Coilcraft D03316T-103ML
$C_{out}$	75 $\mu$ F	Multilayer Ceramics
$C_{in}$	22 $\mu$ F	Multilayer Ceramics
$S_{main}$		LT1371HV
$D$		Fairchild S310

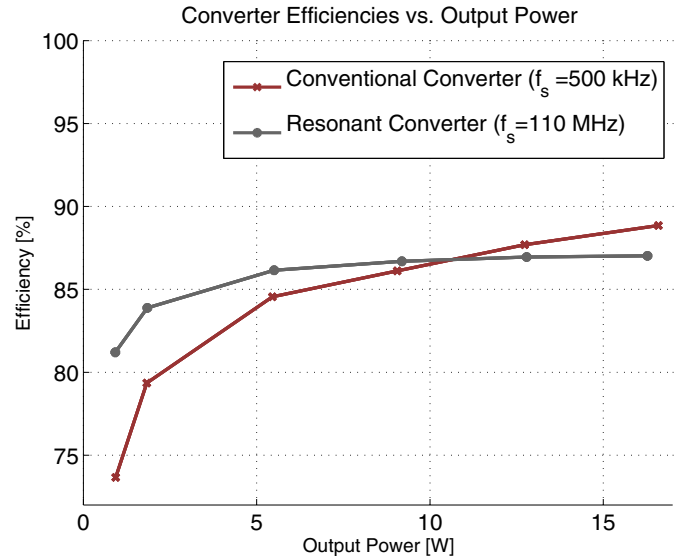


Fig. 8. Plot of efficiency for various power levels for the resonant and conventional converter.  $V_{IN} = 15$  V and  $V_{OUT} = 32$  V for this measurement.

mass is less than one fourth that of the conventional converter. Moreover, because the largest inductor in the resonant converter is only 33 nH and no magnetic materials are required, co-packaging of the passive components appears to be far more feasible for the resonant design.

While the two converters have nearly identical output capacitance, the output voltage ripple magnitudes in steady state are not the same, owing to the different control approaches used. The steady-state output voltage ripple of the conventional converter is 10 mV<sub>p-p</sub>, while the output voltage ripple of the 110 MHz converter (owing to on-off “modulation”) is fixed by the hysteretic controller at 200mV<sub>p-p</sub>. This difference is not surprising, as the PWM converter has its fundamental

TABLE IV  
PASSIVE COMPONENT VOLUME COMPARISON

	Resonant	Conventional
Inductor Box Volume [mm <sup>3</sup> ]	187	831
Inductor Mass [mg]	289	1167
Capacitor Box Volume [mm <sup>3</sup> ]	266	240
Capacitor Mass [mg]	1718	1466
<b>Total Volume [mm<sup>3</sup>]</b>	<b>453</b>	<b>1071</b>
<b>Total Mass [mg]</b>	<b>2007</b>	<b>2633</b>

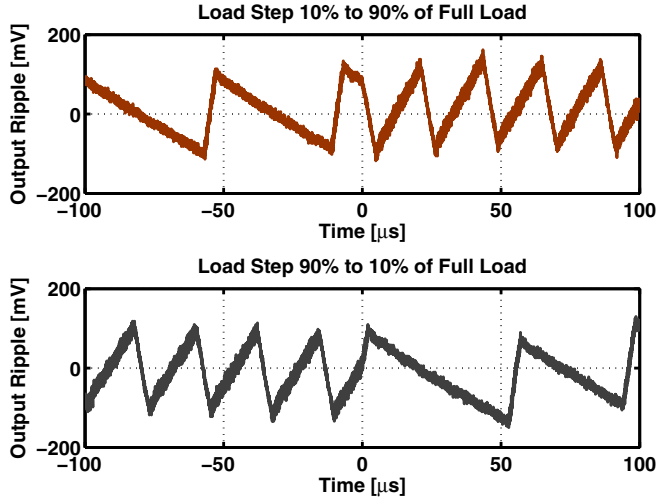


Fig. 9. Output voltage ripple of the resonant converter for load steps between 10 and 90% of full load.

ripple frequency at 500 kHz, while the voltage hysteretic on-off controller of the resonant converter modulates the converter at a load-dependent rate (20 kHz - 50 kHz typical) in order to keep the output voltage within its 200 mV ripple band <sup>7</sup>.

Figure 9 shows the transient responses of the resonant converter for load steps between 10% and 90% of full load (18 W) when operating at an input voltage of 14.4 V. The voltage ripple due to the on-off modulation is clearly observable, as is the effect of the load steps at time = 0. It can be seen that the transient response is essentially instant, and the output voltage never deviates out of its 200 mV hysteresis window. The load step responses for the conventional PWM converter are shown in Fig. 10. While voltage deviation and settling time are on the order of millivolts and microseconds for the resonant converter, they are on the order of volts and milliseconds for the conventional converter. The superior response characteristic of the resonant converter can be ascribed to the far lower values of inductance and energy storage of the resonant converter power stage, owing to its much higher switching frequency.

<sup>7</sup>We did not seek to minimize either capacitance or steady-state voltage ripple in the resonant converter design. As discussed in [76], the required capacitance for the resonant design can be substantially reduced (at constant voltage ripple) for a small efficiency penalty (a factor of 5 reduction in capacitance for 2% reduction in efficiency). Likewise, while it was not tested, it is reasonable to assume that the design could be modified to reduce ripple by the same factor at constant capacitance for a similar efficiency reduction.

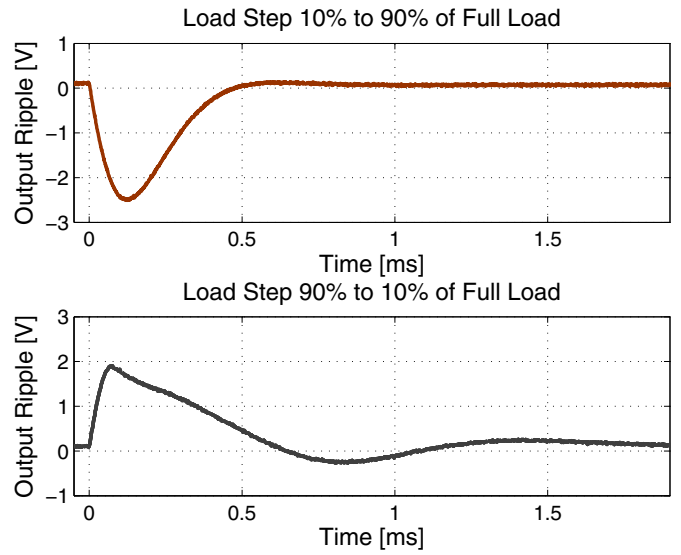


Fig. 10. Output voltage ripple of the conventional converter for load steps between 10 and 90% of full load. Note difference in scale compared to the response of the resonant converter (Figure 9).

As an additional experiment, extra output capacitance was added to the conventional converter in an attempt to achieve a transient response magnitude comparable to that of the resonant converter. Adding an additional 4400  $\mu$ F of additional capacitance (UCC U767D 35 V Electrolytic, volume 13550 mm<sup>3</sup>, much greater than that of the entire converter) still produced a transient voltage deviation that was 2.5 times larger than that of the resonant converter. It is clear from these results and others [18] that VHF resonant converters have a tremendous advantage in applications where transient response is an important consideration in sizing the filter capacitors.

### B. Frequency Scaling: Resonant Designs

To demonstrate how resonant VHF power converters scale in frequency, we present the characteristics and performance of two resonant dc-dc converters designed to closely related (but not quite identical) specifications at different frequencies. Both converters are designed with the same semiconductor switch (the ARF521) using the  $\Phi_2$  inverter topology [73], and are designed for 200 W output capability over a 160 V - 200 V input voltage range. The first dc-dc converter, described in detail in [21], [77], is designed at 30 MHz for a 33 V output. The second dc-dc converter, presented here for the first time, is designed at 10 MHz for a 75 V output. The first converter (at higher frequency and higher conversion ratio) represents a somewhat more challenging specification, but the two designs are otherwise closely linked. Both are designed using the same process, and built on the same circuit board using an identical technology base – custom-wound coreless solenoid magnetics, ceramic and porcelain capacitors, and SiC Schottky diodes (two CSD10030 in parallel). As illustrated in Fig. 11, the main practical difference between the two designs besides frequency is that while the 10 MHz design uses a resonant inductor as part of the rectifier, the 30 MHz design

TABLE V  
COMPONENT VALUES OF THE TWO  $\Phi_2$  DC-DC CONVERTERS

Component	Value		Units
	10 MHz	30 MHz	
$L_F$	805	384	nH
$L_{MR}$	595	414	nH
$C_{MR}$	100.8	16.2	pF
$C_{F,extra}$	245.3	28	pF
$L_S$	722	175	nH
$L_R$	798	78.5	nH
$C_S$	30	4	nF

TABLE VI  
INDUCTOR BOX VOLUME COMPARISON FOR THE 10 MHz AND 30 MHz DESIGNS

Component	Volume [ $mm^3$ ]	
	10 MHz	30 MHz
$L_F$	3281	2620
$L_{MR}$	4342	2850
$L_S$	5285	1688
$L_R$	3149	n.a.
Autotransformer	n.a.	3090
<b>Total:</b>	16057	10248

uses a 1:1 autotransformer for both voltage transformation and as part of the rectifier, owing to its lower output voltage.

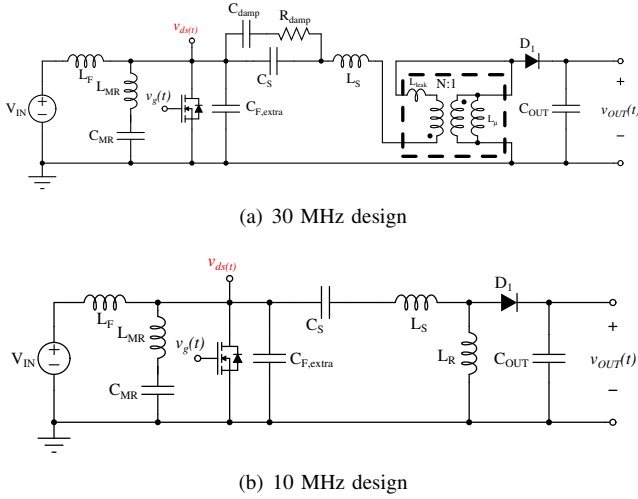


Fig. 11.  $\Phi_2$  based dc-dc converters.

Component values of the two converters are listed in Table V. Note that the external capacitance in parallel with the switch,  $C_{F,EXTRA}$  is much smaller in the 30 MHz design than in the 10 MHz design, in keeping with the frequency scaling implications for semiconductor devices discussed in Section II<sup>8</sup>. For purposes of power stage evaluation and comparison, the gates of the respective ARF521 transistors were driven sinusoidally (with an offset) from a 50  $\Omega$  power amplifier through a 16:1 (in impedance) transmission-line transformer (AVX-M4 from Avtech) to achieve a duty ratio of approximately 0.3 in both cases. It was found that the power amplifier driver was much more capable of maximally enhancing the MOSFET in the 10 MHz design than in the 30 MHz design owing to the reduced input admittance and drain-gate feedback effect at the lower drive frequency, in keeping with the discussion of Section II. (In fact, the design of a suitable resonant gate drive for the 30 MHz converter was found to require a significant effort [21].)

<sup>8</sup>Scaling to frequencies much higher than 30 MHz would yield designs with no extra capacitance, and in which the inverter passive network effectively absorbs the excess device capacitance. The ability to effectively absorb excess device capacitance is a particular advantage of the  $\Phi_2$  inverter topology [21], [73], [77].

Figure 12 shows experimental measurements of  $v_{ds}(t)$  across the ARF521 for the two prototypes. Notice the trapezoidal shape of the drain to source voltage in each case, which is determined by the selection of passive components as explained in [73]. The device voltage stress is greatly reduced as compared to a conventional class E design by this waveshaping, enabling the use of a much lower-voltage transistor.

Figure 13 shows the open-loop power and efficiency achieved by both designs. Both designs provide the required power capability across the input range. The efficiency of the 10 MHz design (not including gating loss here) is 2.5%-6.5% higher than the 30 MHz design owing to multiple factors, including the higher output voltage in the 10 MHz case. Important among these factors, however is the higher displacement loss in the 30 MHz design along with the greater difficulty in fully enhancing the MOSFET at 30 MHz.

Table V shows passive component values and table VI shows a comparison of the box volume occupied by the inductors in both the 10 MHz and the 30 MHz prototypes. It can be seen that the increase in frequency from 10 to 30 MHz affords substantial reduction in several of the passive component values (and corresponding energy storage) providing the potential for significantly faster transient response and smaller closed-loop voltage ripple. The reduction in magnetic volume by 36% is more modest but still quite substantial especially given the more challenging transformation requirements of the 30 MHz design. It may be concluded that aggressive frequency scaling of resonant designs can provide substantial benefits with limited impact on efficiency.

## V. SUMMARY AND CONCLUSION

This paper explores both the opportunities and challenges in power conversion in the VHF frequency range of 30-300 MHz. Frequency scaling of power converters is explored, and we examine how the physical sizes of magnetic components change with increasing frequency. It is shown that considerable reduction in the size of magnetic components is possible through frequency scaling if appropriate materials and designs are employed. The paper also explores the impacts of frequency scaling on semiconductor devices, circuit topologies, and control methods. We describe many of the obstacles in designing efficient and robust power converters at

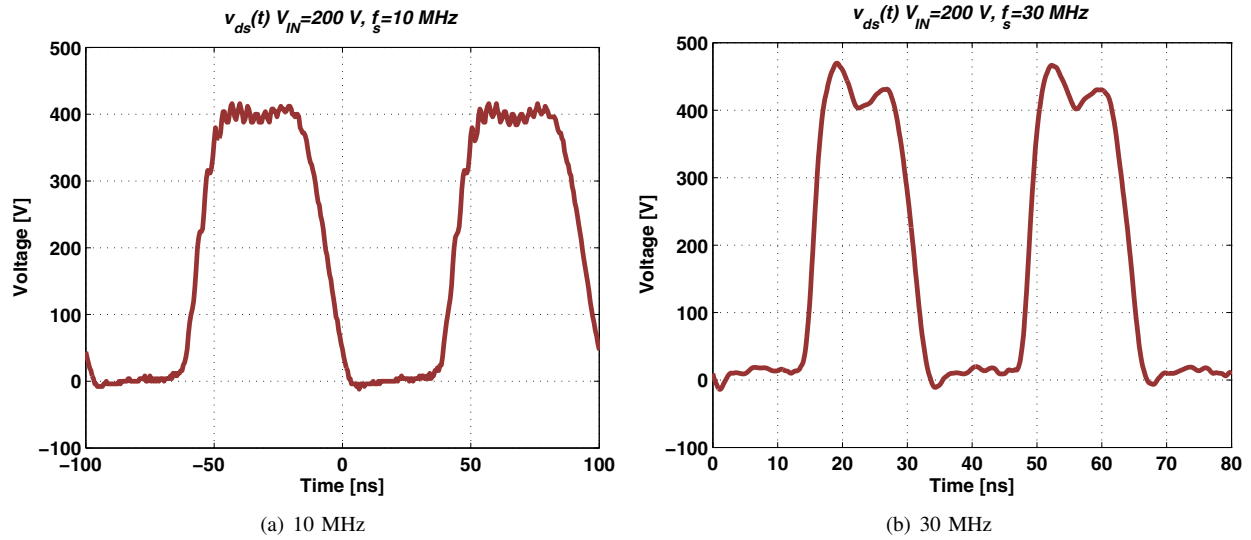


Fig. 12. Experimental measurement of the  $v_{ds}(t)$  for the (a) 10 MHz and (b) 30 MHz dc-dc converters, when  $V_{IN} = 200$  V.

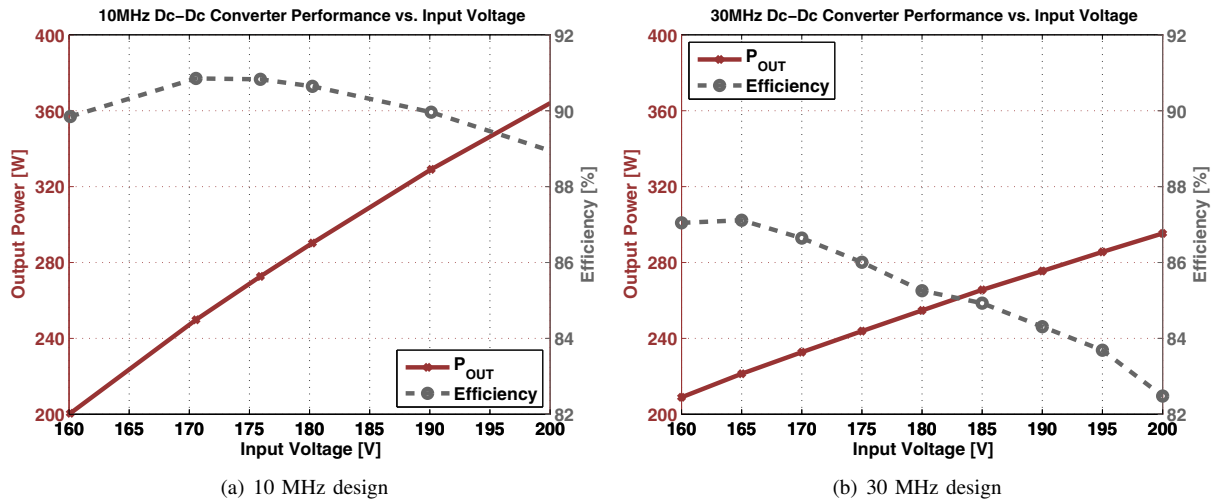


Fig. 13. Performance of the  $\Phi_2$  based dc-dc converters. (a) Shows the performance of the 10 MHz converter (b) Shows the performance of the 30 MHz converter

VHF frequencies, and point out some of the methods being used to overcome these obstacles. Finally, the paper presents experimental examples illustrating the advantages, limitations, and tradeoffs in VHF power conversion. A first example compares a resonant boost converter operating at 110 MHz to a conventional PWM converter operating at 500 kHz, while a second example shows how size and performance of a resonant dc-dc converter change when the design frequency is changed. It may be concluded that VHF power conversion holds great promise for improvements in miniaturization, integration, and bandwidth of power electronic systems.

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