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Opportunities, Challenges and Potential Solutions in the Application of Fast-switching Silicon Carbide (SiC) Power Devices and Converters

Xibo Yuan, *Senior Member, IEEE*, Ian Laird, *Member, IEEE* and Sam Walder

Abstract- **Power devices based on wide-bandgap (WBG) material such as silicon-carbide (SiC) can operate at higher switching speeds, higher voltages and higher temperatures compared to those based on silicon (Si) material. This paper highlights some opportunities brought by SiC devices in existing and emerging applications in terms of efficiency and power density improvement. While the opportunities are clear, there are also design challenges that must be met in order to realize their full potential. For example, the fast switching speeds and high d*v*/d*t* of SiC devices can cause increased electromagnetic interference (EMI), current overshoot, cross-talk effect and have a negative impact on loads such as motors. This paper presents several potential solutions to tackle the application challenges and to fully exploit the superior characteristics of SiC devices and converters while attenuating their negative side-effects. This paper provides an overview of recent SiC device research and development activities based on academic literature, work carried out by the authors and collaborators as well as input from industry. It aims to provide benchmark results and a timely and useful reference to accelerate the adoption and deployment of SiC devices and converters.**

Index Terms **—Silicon carbide (SiC); wide-bandgap; power converters; efficiency; d*v*/d*t*; power density**

I. Introduction

The emergence of wide-bandgap (WBG) material such as silicon-carbide (SiC) and gallium-nitride (GaN) based power devices has brought with it clear opportunities for enabling compact, more efficient power converters, operating at higher voltages, frequencies and temperatures to meet the increasing demand from a range of existing and emerging applications.

Fig.1 shows the properties of three semiconductor materials, i.e. silicon (Si), SiC and GaN [1]. As seen, SiC has a wider bandgap than Si, which enables higher temperature operation. The higher breakdown field of SiC leads to a higher voltage blocking capability with both a practical material thickness and a reasonable on-state voltage drop. Higher thermal conductivity reduces the thermal resistance for better heat (power loss) dissipation.

Although the research into SiC power devices dates back to the 1980s [2], commercially available SiC power devices only started appearing in 2001 with the introduction of SiC Schottky diodes and JFETs [3, 4] and then in 2010 with SiC MOSFETs and BJTs. At the time of writing, 1.7kV/25A discrete SiC Schottky diodes, 1.7kV/72A discrete SiC MOSFETs, 1.7kV/225A SiC MOSFET modules, from CREE/Wolfspeed and 1.7kV/160A SiC BJT modules from GeneSiC represent some of the highest voltage/current rated devices commercially available.

In terms of high-temperature devices, 210°C SiC BJTs (600V/20A) from GeneSiC are commercially available. From the published literature, 15 kV SiC IGBTs, 10 kV SiC Schottky diodes and MOSFETs have been tested in labs [5, 6] as well as 250°C SiC modules [7, 8]. Currently, the voltage ratings of SiC power devices are 650V and higher, mainly targeting applications with a dc-link voltage higher than 400V while the voltage ratings of GaN power devices, e.g. high-electron mobility transistors (HEMTs) are below 650V.

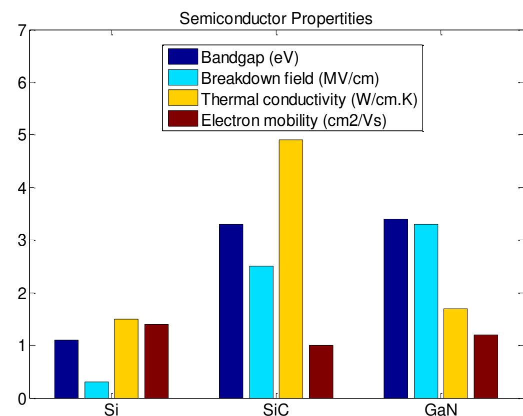

Fig.1. Semiconductor properties of Si, SiC and GaN [1].

At present, the main suppliers of SiC power devices include CREE/Wolfspeed, ROHM, Infineon, STMicroelectronics, GeneSiC and Microsemi. The main suppliers of GaN power devices include GaN systems and EPC.

The high voltage, high switching speed and high temperature capabilities of SiC power devices have the

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potential to bring significant performance improvement to existing systems and enable new applications. For example, in the medium-voltage (3kV~33kV) high-power drive area, the cascaded H-bridge (CHB) converter is one of the most popular structures. And it is probably the only choice when the required output voltage is higher than 6kV due to the voltage limitation of Si IGBTs or IGCTs (normally limited to 6.6kV) if a series connection of power devices is not desired [9, 10]. However, the CHB converter suffers from a low power density due to the requirement of a large input multi-winding transformer. Furthermore, a large dc-link capacitance with a high voltage rating is required to filter out the single-phase low-frequency power ripple in each H-bridge cell, which significantly adds to the system volume and cost while also degrading the reliability. Normally, the capacitors account for around 1/3 of the volume and cost of the converter. With high-voltage 10kV+ SiC MOSFETs and 15kV+ SiC IGBTs [6], a 6kV or 10kV output can be achieved directly with a high-power-density three-level diode neutral-point-clamped (NPC) structure instead of using a cascaded structure or a multilevel modular converter (MMC) [11]. Thus, no large dc-link capacitors or complex input transformers are needed, and the structure is much simpler.

The reduced switching loss of fast-switching SiC devices means the converter switching frequency can be increased. In medium voltage and high power (MW+) applications, the switching frequency can therefore be extended from below 1kHz with Si devices to several kHz with SiC devices [12]. This enables a higher control bandwidth, lower current/voltage ripples which reduces the converter's filtering requirement. Compact and high-efficiency SiC-device-based, medium-voltage power conversion systems can also facilitate the adoption of power-electronics-based power distribution equipment such as solid-state-transformers, where the power density and efficiency have been identified as a bottleneck to them replacing the conventional transformers [13]. The power-electronics-based distribution network can provide significant control advantages, especially for interfacing renewable sources, energy storage as well as for more electrified transportation systems.

In motor drive or power generation applications, in order to reduce the weight and size of electric machines (motor or generator), high speed machines (lower torque for the same power) with a high number of poles are preferred. This results in electric machines with a high fundamental frequency and thus demands power converters with a high switching frequency, which the SiC devices are suited to. High switching frequency also leads to lower dc-link voltage/current ripples, thus reducing the required dc-link capacitance so that a higher power density can be achieved. This also allows film capacitors to replace electrolytic capacitors in the dc-link for a higher reliability in electric vehicle (EV) drive applications given the low capacitance to volume ratio of film capacitors. High-switching-frequency drives can also reduce the switching-harmonics-induced rotor losses, e.g. in permanent magnet machines, where the heat (losses) is more difficult to dissipate from the inner rotor as the liquid cooling is provided through the outer stator.

Another area where SiC power devices will be a key enabler is more electric aircraft (MEA) or full electric aircraft (FEA) with hybrid/full electric propulsion, which requires tens of MW of efficient power conversion with high fundamental frequency (kHz) drives, higher voltage levels (>1kV) as well as higher power density (>20kW/kg) [14]. Similarly, SiC power devices will be key for high-power wireless power transfer systems, where the trend is to push the frequency from tens of kHz to MHz at kW power levels to minimize the coil size and increase the power transfer distance and efficiency [15]. As the frequency of WBG devices gets higher and higher, more and more techniques used for radio frequency (RF) engineering can be used for power electronics such as circuit topologies (e.g. class E/F converters [16]), current/voltage measurement techniques and parasitic analysis.

The high temperature characteristics of SiC devices can reduce the cooling requirement or potentially change the cooling method, e.g. moving from liquid cooling to forced air-cooling. It also enables the devices to operate in harsh, high-temperature environments. However, most of the commercially available SiC discrete devices or modules today still have a maximum junction temperature of 150°C, which is not much higher than the junction temperature of standard Si devices of 125°C. In fact, there are also commercially available 175°C Si IGBT modules. The limitation on the maximum junction temperature is partly due to the lack of reliable and low-cost packaging solutions, where existing packaging solutions for power modules and discrete devices have a temperature limit around 175°C [17]. Also, at higher temperatures, the gate oxide of SiC MOSFETs exhibits reliability issues. Furthermore, the on-state resistance $R_{ds(ON)}$ of SiC MOSFETs increases rapidly with the temperature. For example, for the Wolfspeed C2M0040120D SiC MOSFET, the $R_{ds(ON)}$ at 150 °C is 72 mΩ, 1.8 times of that at 25 °C (40 mΩ) [18]. Thus, the on-state resistance, corresponding voltage drop and conduction losses of a SiC MOSFET at high temperature is another concern. Similarly, for SiC BJTs, the current gain drops with the increase in temperature [19, 20].

Fig.2 shows some application examples that can benefit from high-voltage and high-frequency SiC devices. Transformative improvement can be made for medium voltage power conversion in terms of efficiency and power density, and for MHz frequency power conversion in terms of light-weight passive components such as air-core inductors and ceramic capacitors.

SiC converters are being demonstrated or adopted in applications such as solar inverters [21, 22], railway traction inverters [23], EV/HEV drives [24-26], uninterrupted power supplies (UPS) [27] and high voltage applications [28]. One of the most cited application examples is the adoption of SiC MOSFETs in Tesla Model 3 EVs [24], supplied by STMicroelectronics.

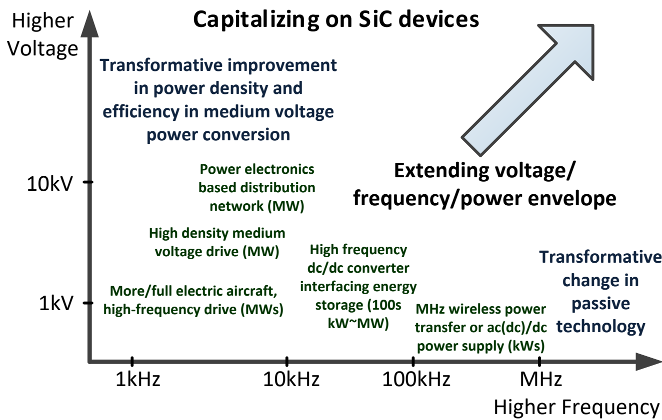


Fig.2. Potential application examples using SiC devices at various voltage and frequency levels.

Although there is literature reviewing WBG power semiconductor devices [1] and their applications [4, 5], there is a lack of review of research aspects at the component and converter level for SiC devices. This paper therefore aims to fill part of this gap and highlight some opportunities, challenges and potential solutions in the application of SiC power devices and converters. The aim is to provide a useful reference for researchers and engineers to better understand these devices and accelerate their wider deployment in various applications and realize their full potential.

The structure of the paper is organized as follows: Section II shows the capabilities of SiC devices, especially relating to fast switching speed, reduced power losses and the resultant higher efficiency and power density. Section III reveals some of the key challenges of using SiC devices, especially those due to high d*v*/d*t*. Section IV provides some solutions to address the challenges given in Section III. Section V concludes the paper.

II. Performance Improvement with SiC Power Devices

One of the earliest adopted SiC devices was the SiC Schottky diode, which has zero reverse-recovery loss. The voltage ratings of Si Schottky diodes are limited to 200V while the SiC ones can reach 10kV. SiC Schottky diodes can be co-paired with Si IGBTs to offer a cost-effective solution. By replacing a Si PN diode with a SiC Schottky diode, the total switching loss may be reduced by 25% [29] as this removes the power loss due to reverse recovery in the diode and IGBT. This leads to either reduced cooling requirements, efficiency improvement or a higher switching frequency. Fig.3 shows the reverse recovery characteristics of a Si PN diode (IXDH20N120D1) and a SiC Schottky diode (GA35XCP12-247) during turn-off [30]. As seen, the SiC Schottky diode has a much smaller negative current due to the removal of the reverse recovery effect. The small negative current of the SiC diode is due to the charging of its junction capacitance. [30] has discussed the EMI benefits of removing the reverse recovery current by using SiC Schottky diodes to replace Si PN diodes. The conclusion is that the EMI reduction is relatively small unless the Si diode has a super-fast (<30ns) reverse recovery current slope (higher harmonics), the removal of which can lead to a clear EMI reduction.

Fig.4 compares the turn-off (reverse recovery) energy of three diodes: a standard Si PN diode (DSEC60-12A), a fast Si PN diode (DSEI12-10A) and a SiC Schottky diode (GA35XCP12). As can be seen, the SiC Schottky diode has the smallest turn-off energy due to the absence of reverse recovery [30].

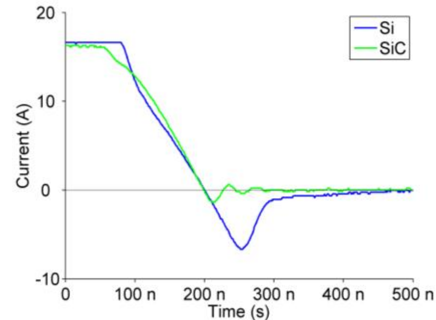


Fig.3. Turn-off current of a Si PN diode (IXDH20N120D1) and a SiC Schottky diode (GA35XCP12-247).

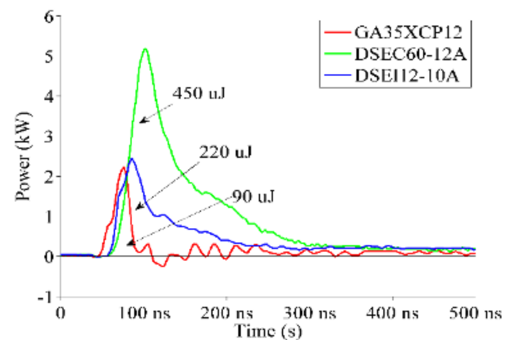


Fig.4. Turn-off (reverse recovery) energy of a Si PN diode (DSEC60-12A), a fast Si PN diode (DSEI12-10A) and a SiC Schottky diode (GA35XCP12).

Regarding fully-controlled SiC switching devices, commercially available ones include MOSFETs, BJTs and JFETs. SiC MOSFETs have the greatest potential to replace Si IGBTs. The SiC MOSFET has a faster switching speed and hence lower switching loss than the Si IGBT. Therefore, it may replace the IGBT to achieve a higher efficiency for the same switching frequency or to achieve a higher switching frequency with a similar efficiency. The voltage ratings of SiC MOSFETs range from 650V to 10kV+, which covers and extends the voltage range of Si IGBTs. Currently, there are SiC MOSFET samples with a voltage rating of 10kV [6] and 15kV [31]. A 10kV, 120A SiC module is demonstrated in [28, 32]. Other SiC devices need special arrangements to be used. The SiC JFET is a normally-ON device, though cascode configuration can be used to make the device normally-OFF. The SiC BJT needs a constant base current to drive and requires an additional anti-parallel diode if used in inverter applications.

From the conduction loss point of view, as a uni-polar device, the SiC MOSFET does not offer much a conduction

loss benefit compared to the Si IGBT as a bi-polar device with conductivity modulation. Also, as mentioned, the on-state resistance ($R_{ds(ON)}$) of SiC MOSFETs increases quickly with temperature. For example, two representative devices are given here for comparison: one is a SiC MOSFET from Wolfspeed (C2M0040120D) and the other one is a Si IGBT from Infineon (IKW40N120T2). Both these two devices are rated 1200V and 40A at around 150°C. From the datasheet, the $R_{ds(ON)}$ of the SiC MOSFET is 84mΩ at 150°C and this translates to a voltage drop of 3.36V at 40A. In contrast, the Si IGBT voltage drop is 2.25V at 40A at 150°C. As seen, in this case, the Si IGBT has even lower voltage drop (conduction loss) than the SiC MOSFET. Fig.5 further shows the forward voltage drop of these two devices. As expected, the SiC MOSFET forward voltage drop has a linear slope, i.e. $R_{ds(ON)}$ within 60A. The Si IGBT forward voltage drop has some initial voltage drop (V_{CE0}) followed by an exponential curve. At low current, the MOSFET has lower voltage drop and at a higher current (>20A), the IGBT has a lower voltage drop. Because the SiC MOSFET does not have the initial voltage drop (V_{CE0}) as in Si IGBTs, at low current (low load) conditions, the SiC MOSFET will have lower losses.

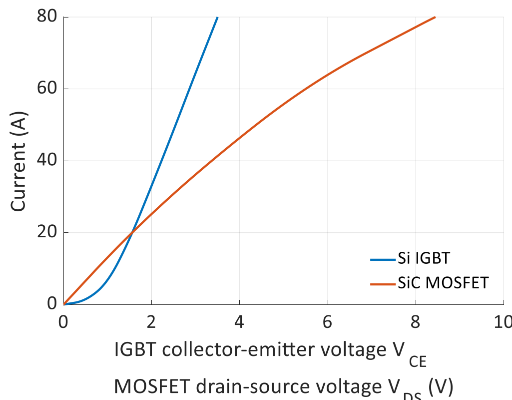


Fig.5. Si IGBT and SiC MOSFET forward voltage drop characteristics.

For the switching loss, with the same gate resistance of 12Ω, the Si IGBT (IKW40N120T2) has a total switching energy loss (turn-on and turn-off) of 5.25mJ while that of the SiC MOSFET (C2M0040120D) is 2.1mJ, which is much lower than the Si IGBT. Therefore, the main benefit of using SiC MOSFETs is on the switching loss reduction.

Fig.6 shows turn-off transient waveforms measured in an experiment of a Si IGBT with a Si diode (All-Si), a Si IGBT with a SiC diode (Si-SiC) and a SiC MOSFET (All-SiC). As seen, the SiC MOSFET switches much faster (within 50ns) than the Si IGBT (500ns). The turn-on speed of a SiC MOSFET is much faster than a Si IGBT as well. This fast switching speed can lead to a significant reduction of the switching loss, and thus improve the efficiency. Note that the turn-on switching loss of a SiC MOSFET is normally higher than the turn-off switching loss due to the higher turn-on current overshoot and no tail-current during turn-off (as in IGBTs), which will be analysed in later sections.

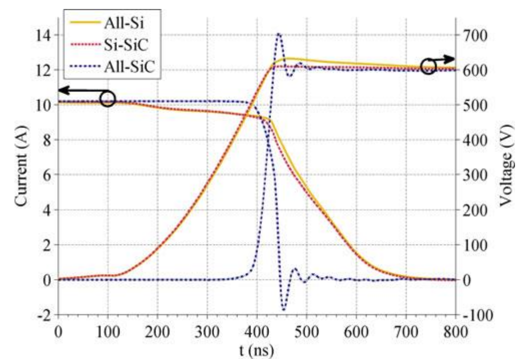


Fig.6. Turn-off transients of a Si IGBT with a Si diode (All-Si), a Si IGBT with a SiC diode (Si-SiC) and a SiC MOSFET (All-SiC) [33].

Fig.7 shows the measured efficiency of a 5kW three-phase two-level SiC MOSFET converter, where both a thermal superposition-based method [34, 35] and an analytical converter power loss model with switching energy obtained through double pulse test (DPT) [35] have been used to obtain the efficiency. In comparison, the efficiency of a Si IGBT converter of the same power rating has been plotted using the analytical converter power loss model with switching energy obtained through DPT. As can be seen, the SiC MOSFET converter has a higher efficiency than the Si IGBT converter. The efficiency of the Si IGBT converter drops to ~98.2% at a 20kHz switching frequency. This is why the switching frequency of a hard switched two-level IGBT converter is normally below 20kHz [36].

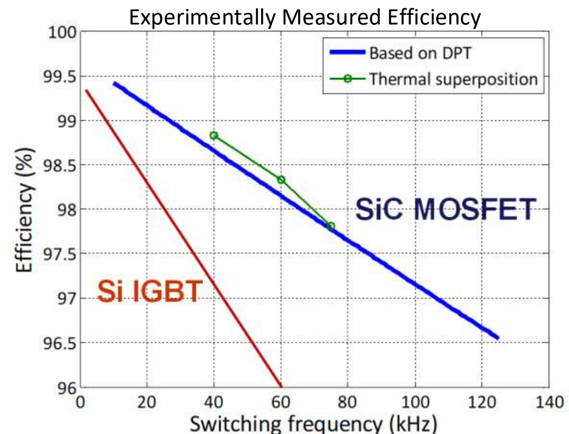


Fig.7. Variation of efficiency with switching frequency of a Si IGBT based converter and a SiC MOSFET based converter (DPT: double pulse test).

In comparison, the switching frequency of the SiC converter can be extended to 60kHz, while still retaining an efficiency above 98%. The ability to increase the switching frequency can lead to a volumetric reduction of passive components, such as filter inductors and capacitors, and hence improve the system power density. High switching frequency operation is also an enabler for high-frequency motor drives, where the fundamental frequency can reach several kHz for multi-pole high-speed electric machines (for the pursuit of volume and weight reduction). On the other hand, with the same switching frequency, the efficiency of the SiC MOSFET converter will be higher than the Si IGBT converter due to the

reduction of the switching loss. The improvement in efficiency can reduce the cooling requirements (heatsink) or enable a step change from liquid cooling to air cooling. Note that, a 1% improvement in efficiency around 98% means a 50% power loss reduction. In other types of converter topologies such as soft-switching topologies and multilevel topologies, the switching frequency can be pushed to an even higher level than the two-level hard-switching converter. For example, Vienna rectifiers can operate at a switching frequency of 50kHz with Si IGBTs [37]. If the IGBTs are replaced with SiC MOSFETs, the switching frequency can be further extended into the 70 to 100kHz range. For single-phase systems, SiC MOSFETs replacing Si IGBTs can also lead to efficiency improvement or achieve a higher switching frequency [38-40].

Fig.8 shows the turn-on and turn-off test results of a high-power (1700V, 300A) SiC MOSFET (CAS300M17BM2) module and a Si IGBT (FF200R17KE3) module with the same voltage and current ratings. The test currents are 120A and 200A, respectively [41]. As seen, the switching transients of the SiC MOSFETs are much faster than the Si IGBTs, noting the long tail current of the Si IGBTs during turn-off on the right in Fig.8(b). The switching transient time of the high-power SiC MOSFET modules is within 100ns.

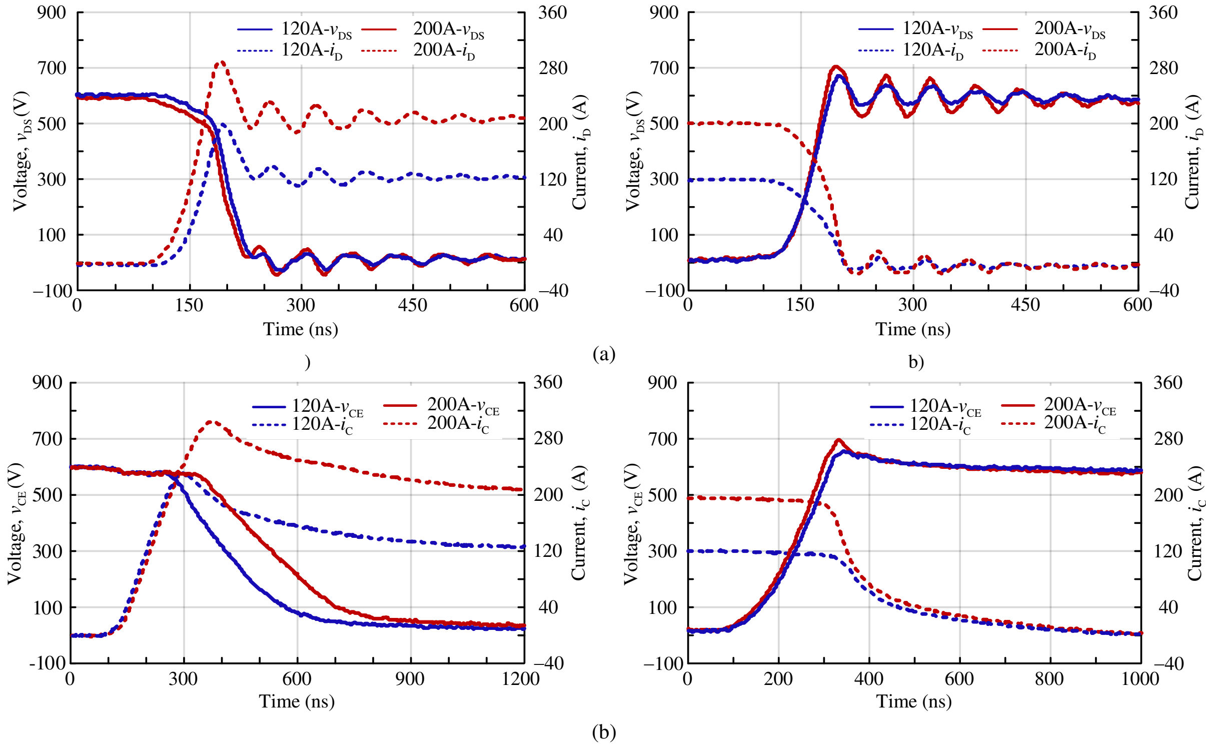


Fig.8. Turn-on and turn-off transients of a SiC MOSFET module and a Si IGBT module: dotted line: current; solid line: voltage. (a) SiC MOSFET switching voltage and current. Left: turn-on waveforms; Right: turn-off waveforms. (b) Si IGBT switching voltage and current. Left: turn-on waveforms; Right: turn-off waveforms.

In regard to the converter power density improvement due to the lower switching loss and higher switching frequency of SiC devices, [35] has shown a holistically optimized design for a 5kW air-cooled three-phase DC/AC converter. By replacing Si power devices with SiC ones, the total converter volume and weight has been reduced from 3.7L to 1.4L and from 8.2kg to 2.2kg for the same efficiency of 98%, respectively as shown in Fig.9. The corresponding switching frequency of the SiC converter is 63kHz in comparison to 6kHz of the Si IGBT converter. The SiC converter has achieved a power density of 3.5kW/L including EMI filters.

Similarly, for DC/DC converters, [42] has shown a weight reduction from 6.9kg to 5kg for a liquid-cooled 50kW DC/DC converter by replacing Si IGBTs with SiC BJTs. The switching frequencies are 75kHz and 25kHz respectively for the SiC converter and Si converter. This achieves a power density of 10kW/kg of the SiC converter. A recent development has further pushed the power density to 15.7 kW/kg and 31.5kW/L for an 80 kW DC/DC converter switching at 115kHz with an efficiency of 96.6% [43]. Fig.10 shows the picture of the 80kW DC/DC converter using SiC MOSFETs.

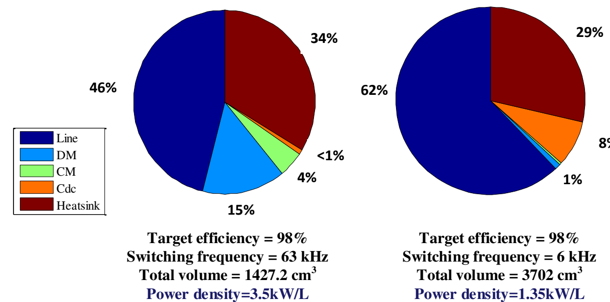


Fig.9. Converter volume split (Left: SiC MOSFET converter, Right: Si IGBT converter). Line: line inductor, DM: differential-mode filters, CM: common-mode filters, Cdc: dc-link capacitor [35].

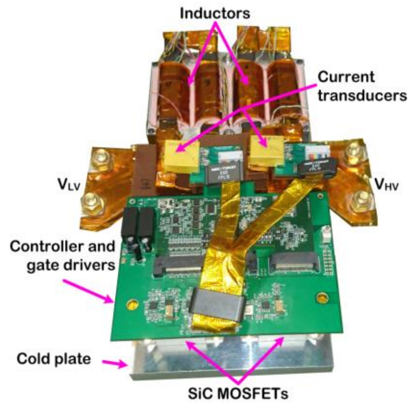


Fig.10. Picture of the 80kW DC/DC converter prototype based on SiC MOSFETs, achieving a power density of 15.7kW/kg and 31.5kW/L [43].

Fig.11 further shows a 500kW forced-air-cooled SiC MOSFET based DC/AC converter that achieves a high-power-density of 1.2kW/L (or 1.2MW/m^3). The converter is formed by five 100kW two-level SiC converters connected in parallel. The DC input voltage is 650V and the AC side output voltage is 380V. The switching frequency is 20kHz. The capability to handle 1.2MW within 1m^3 is significant with forced-air-cooling and will clearly improve the power density of applications such as motor drives, solid-state-transformers and grid-forming converters.

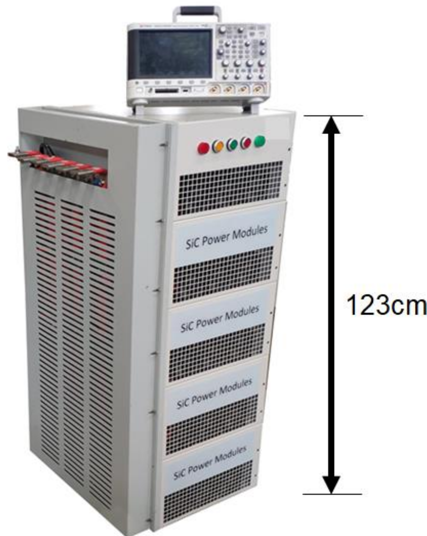


Fig.11. A 500kW forced air cooled three-phase DC/AC converter based on SiC MOSFETs with a power density of 1.2kW/L.

Apart from the SiC MOSFET, another promising SiC power device is the SiC BJT, which does not have the gate oxide reliability issue seen in SiC MOSFETs. This is an advantage when it comes to device and system reliability, especially at high temperatures. As mentioned, there are commercially available 210°C SiC BJTs [19]. However, the SiC BJT needs a constant base drive current to keep the device ON and requires an additional anti-parallel diode for inverter applications. The current gain (h_{FE}) of SiC BJTs is much higher than that of the Si BJTs, e.g. 70 for a SiC BJT vs. 10 for a Si BJT. Therefore, the base current requirement for SiC BJTs is much lower. Also, proportional gate drivers with very low loss can be used for SiC BJTs [44], where the base current is sourced from the main circuit and is proportional to the main (drain) current. An overview of gate drive technologies for SiC BJTs is given in [45].

A like-for-like comparison has been carried out between a 5kW three-phase SiC MOSFET (C2M0040120D) converter as shown in Fig. 12 and a SiC BJT (GA10JT12) converter with proportional gate drivers as shown in Fig.13.

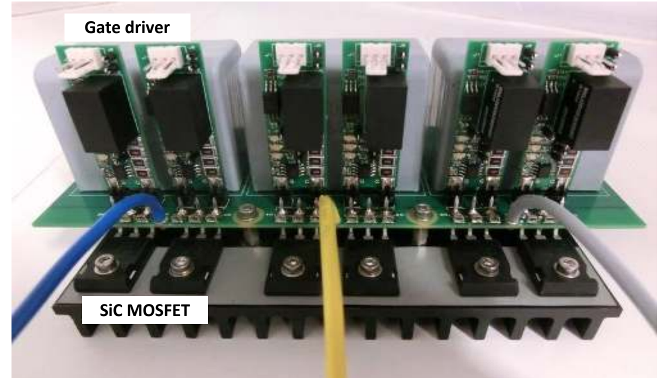


Fig.12. A 5kW three-phase DC/AC SiC MOSFET based converter.

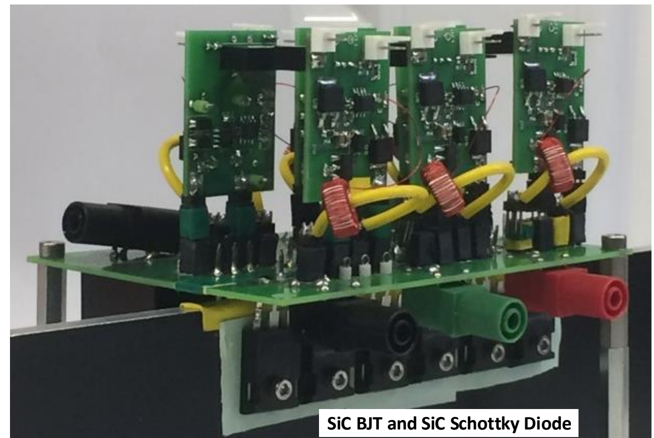


Fig.13. A 5kW three-phase DC/AC SiC BJT based converter.

Fig.14 shows the switching performance of the SiC MOSFET and the SiC BJT converters during both the turn-on and turn-off transients. The SiC MOSFET was tested with various gate resistor values (0Ω to 24Ω) and the gate resistance of 5.1Ω is given in Fig.14 as an example. The SiC BJT is driven by a proportional gate driver [20, 44]. As seen the switching times (overlap between the voltage and current) of these two devices are very similar. The voltage overshoot of the BJT during turn-off is higher than the MOSFET while the current overshoot during turn-on of the BJT is smaller due to the additional (leakage) inductance of the current transformer of the proportional gate driver in the switching loop. The switching transient of the SiC BJT can be further adjusted through the supplied gate current.

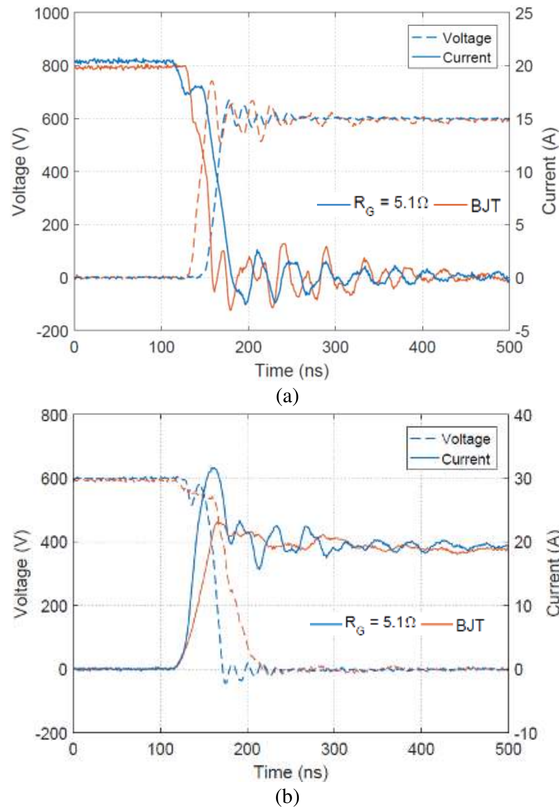


Fig.14. Comparison of switching performance of SiC MOSFETs and SiC BJTs. (a) Turn-off. (b) Turn-on.

The converter efficiency comparison between SiC MOSFETs and SiC BJTs is given in Table I with a switching frequency of 60kHz, where their efficiencies are very close.

TABLE I. EFFICIENCY COMPARISON BETWEEN THE THREE-PHASE SIC MOSFET CONVERTER AND SIC BJT CONVERTER

Parameter	MOSFET	BJT
DC link voltage (V)	599.31	599.59
Input current (A)	6.93	6.95
Input power (kW)	4.15	4.16
Output phase voltage (V)	187.05	187.52
Output phase current (A)	7.23	7.29
Output power (kW)	4.05	4.05
Efficiency (%)	**97.65**	**97.30**

Fig.15 shows the three-phase converter output voltage and currents at 4kW with SiC BJTs [46].

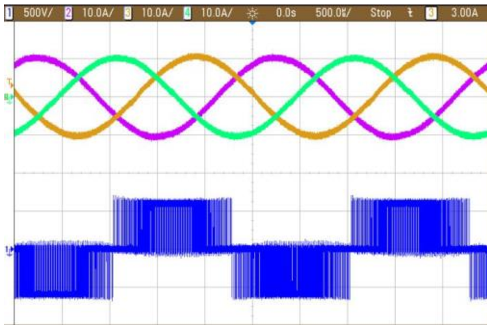


Fig.15. Three-phase SiC BJT converter output waveforms (top: three-phase currents, bottom: line voltage)

A performance comparison between SiC MOSFETs and SiC BJTs used in dc/dc converters can be found in [42] [47], which shows similar results.

Regarding high-voltage capabilities of SiC devices, [6] presented a solid-state transformer demonstrator example.

III. Challenges in the Application of SiC Power Devices and Converters

The main challenges caused by the fast switching speed of SiC devices exisit at both the component level (Section III. A, B, C) and the converter level (Section III. D, E). At the component level, the challeges include the voltage and current oscillations (overshoot, losses), cross-talk effect, parasitic effect, high-speed gate drivers, EMI and passive components. At the converter level, the high d*v*/d*t* can cause negative impact on loads such as motors. Also, the deadtime setting under high switching frequencies, fault-detection and protection and how to increase the converter capacity using exisiting SiC power devices are other converter challenges. These challenges will be presented in detail below.

A. *Current overshoot, ringing, EMI and switching loss*

Though SiC converters can offer clear efficiency and power density improvement, there are also challenges in the design and application of these devices. The high switching speed means high voltage and current slew rates, i.e. d*v*/d*t* and d*i*/d*t*. Fig.16 shows the turn-on voltage and current waveforms of SiC MOSFETs with various values of the gate resistance. The smaller the gate resistance is, the faster the switching speed and the lower the switching energy are. However, as seen in Fig.16, as the switching speed increases, the current overshoots and ringing due to parasitic effects (e.g. parasitic inductance and capacitance in the commutation loop) become larger. The current overshoot is due to the charge of the output capacitance of the complementary MOSFET, parasitic capacitance of the PCB and the load, which will increase the turn-on loss and reduce the expected efficiency. The ringing can create harmonic spikes in the EMI spectrum.

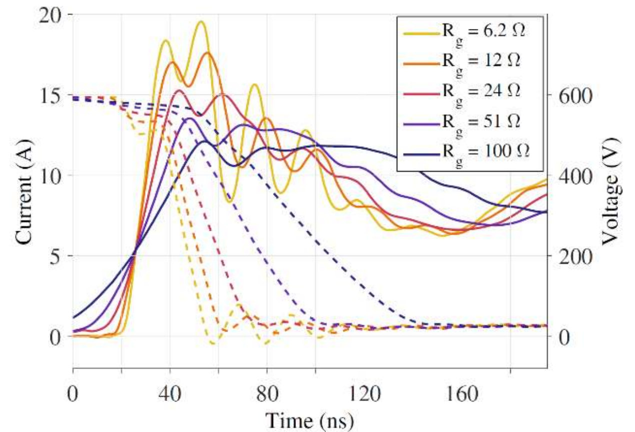


Fig.16. Turn-on switching waveforms of SiC MOSFETs with various gate resistor values.

The increased switching speed (sharper edges) directly leads to higher harmonic contents at higher frequencies, e.g.

MHz+ due to higher voltage/current slew rate. The increase in switching frequency enabled by SiC devices also increases the harmonics in both the low-frequency (switching frequency) and high-frequency regions due to the increased number of switching actions. Therefore, both the increase in switching speed, and switching frequency will increase the harmonics and EMI level.

Fig.17 illustrates the impact of the switching speed (rise time, t_r) and switching frequency on the harmonics. In Fig.17(a), the rise and fall time are assumed to be the same. As seen, the reduction of the rise time (t_r) from 100ns to 50ns causes the harmonics to increase in the MHz+ region. As shown in Fig.17 (b), once the switching frequency is doubled from 20kHz to 40kHz, the harmonics increase in both the switching frequency region (kHz) and MHz+ region, i.e. over the whole frequency range.

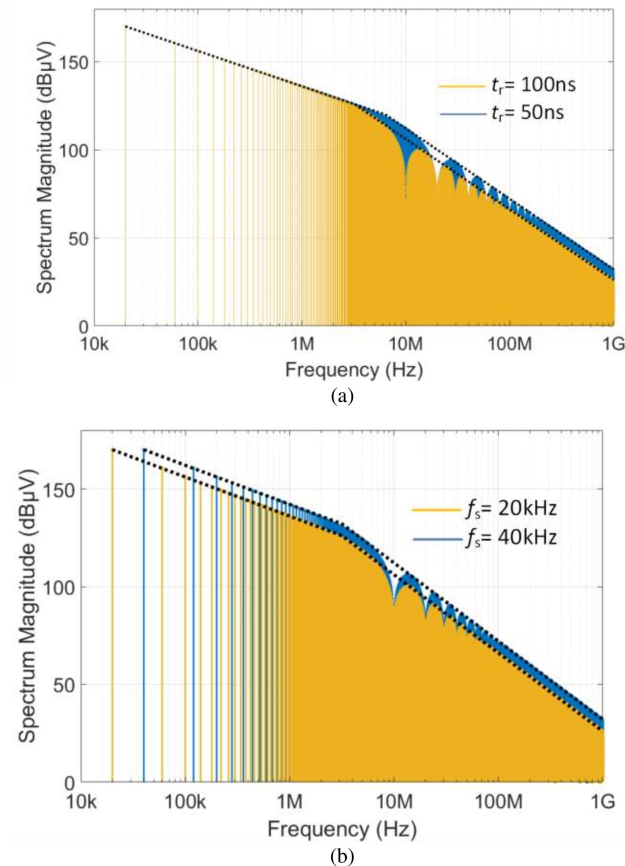


Fig.17. The impact of switching speed (rise time) and switching frequency on the harmonics and EMI. (a) The impact of rise time on harmonics (EMI). (b) The impact of switching frequency on harmonics (EMI).

Fig.18 shows the harmonic analysis of the switching currents in Fig.16. Consistent with the analysis in Fig.17(a), as the switching speed increases (due to smaller gate resistance), the magnitude of harmonics (EMI) increases accordingly, which may result in requiring additional EMI filters. Also, there are clear spikes in the EMI spectra due to the ringing in the time domain waveforms. Designing EMI filters to attenuate the high-frequency harmonics can be challenging as the high-frequency components tend to go through the parasitic elements of the circuit rather than the main circuit.

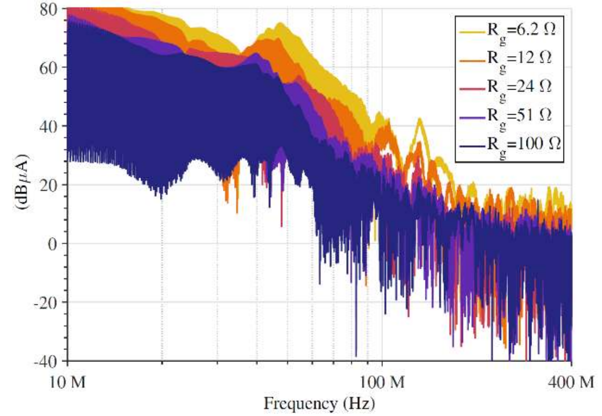


Fig.18. EMI spectra of the switching currents in Fig.16.

Fig.19 shows the trade-off between switching loss and EMI. As the switching speed increases, the switching loss reduces but the EMI level increases. The EMI metric used here was defined in [48].

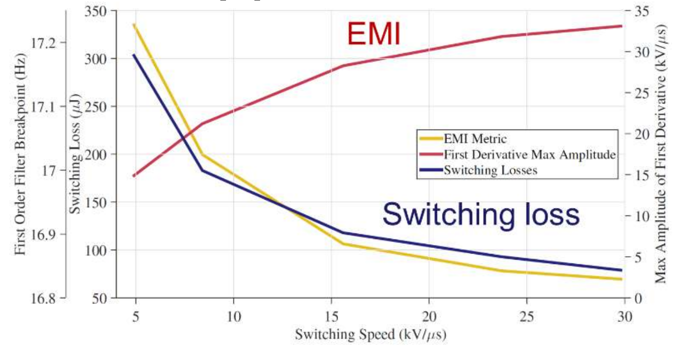


Fig.19. Trade-off between EMI and switching loss in relation to switching speeds.

Note that, the turn-off waveforms (not shown here) are much 'cleaner' than the turn-on waveforms in Fig.16 with less voltage and current overshoot and ringing. Hence, the voltage overshoot during turn-off, which was normally a concern, may not be an issue if the parasitic inductance in the circuit power commutation loop is properly minimized in the design.

In order to investigate the switching loss generation mechanism (especially during turn-on) and further break down the losses, the turn-on and turn-off energies are calculated based on tests with a SiC-MOSFET half-bridge converter circuit. Given the large current overshoot (ringing) during the turn-on transition, the turn-on energy due to the overshoot is calculated separately to that generated by the overlap between the base voltage and current as illustrated in Fig.20 [46].

Fig.21 shows the switching energy at various current levels, where the switching energy has been broken-down into its turn-off energy (blue), turn-on energy base (cyan) and turn-on energy due to the current overshoot/ringing (yellow). There are two observations to note in Fig.21. First, the turn-on energy (base + overshoot) accounts for the majority of the total switching energy (loss) while the turn-off energy (loss) is relatively small. Second, there is clear turn-on energy caused

by the current overshoot. However, this overshoot energy does not change with the magnitude of the current itself, which indicates the overshoot is mainly due to the charge of the parasitic capacitance, i.e. SiC MOSFET output capacitance, PCB capacitance and load capacitance. In the experimental test, the load capacitance has been intentionally minimized. In real applications, the load capacitance can be large, e.g. for electric machines, transformers, filters or power cables. Their impact on switching loss can be much higher than the impact of the MOSFET and PCB capacitance and thus cannot be neglected.

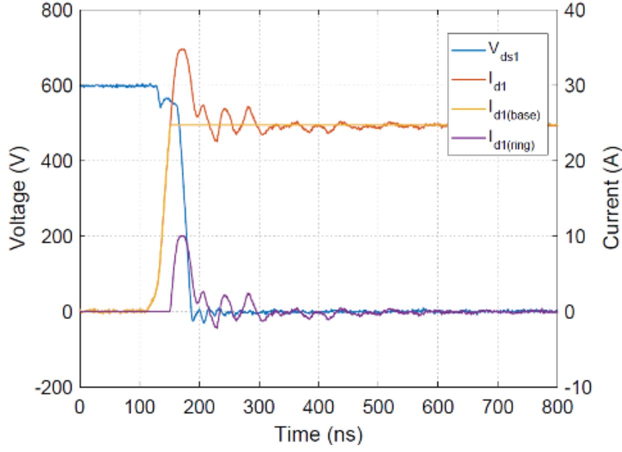


Fig.20. SiC MOSFET turn-on waveforms at 600V, 25A with separated overshoot (ringing) energy calculated (Vds1: drain-source voltage; Id1: drain current; Id1(base): the base (steady state) drain current as illustrated in the figure; Id1(ring): the drain current overshoot as illustrated in the figure).

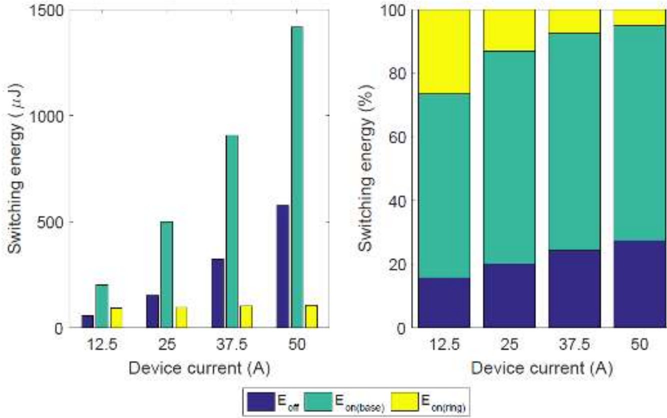


Fig.21. Switching energy: turn-off energy (E_{off}), turn-on energy (base) ($E_{on(base)}$), turn-on energy due to current overshoot/ringing ($E_{on(ring)}$).

The feature that the energy loss due to the overshoot does not change with the magnitude of the current also means the overshoot is not due to the reverse recovery current of the body diode of the SiC MOSFET. Though the body diode of the SiC MOSFET is a PN-type diode, rather than a Schottky diode, from the test results, the body diode has hardly any reverse recovery current. There are some suggestions to use an additional SiC Schottky diode connected in parallel with the SiC MOSFET to minimize the effect of the higher voltage drop of the body diode (~3V) and its reverse recovery issues. From the results in Fig.21, the reverse recovery effect is negligible and the high voltage drop of the body diode during the reverse conduction may not be an issue as synchronous rectification, where the reverse current flows through the MOSFET channel rather than the body diode, is normally used. The body diode only carries the current during the short deadtime period, so the conduction loss is low. Therefore, connecting an additional Schottky diode in parallel with the SiC MOSFET is not necessary from power loss reduction point of view. Also, if a parallel Schottky diode is used, the junction capacitance of the Schottky diode will generate a current overshoot that produces additional losses associated with the main (complementary) switching MOSFET.

B. *Cross-talk effect and gate driver circuit*

Another issue under high switching speeds (dv/dt) is the 'cross-talk' effect [49], where the turn-on transition of one device may increase the voltage at the gate of the complementary device in a bridge-leg structure. If the gate voltage of the complementary device rises above the threshold voltage (e.g. 2V), this may trigger a false turn-on and lead to a shoot-through failure. Fig.22 illustrates the cross-talk effect. The high voltage slew rate (dV_{DS}/dt) is applied across the Miller capacitance (C_{GD}) of the bottom device during the top device M1 turn on. The resulting current (i_{Miller}) causes a voltage drop on the gate resistance (R_g) and internal resistance of the gate driver (R_{driver}), which raises the gate voltage. In order to avoid the false turn-on of the bottom device, a negative gate voltage ($V_{neg\text{-}supply}$) is normally adopted, e.g. -5V during the OFF state.

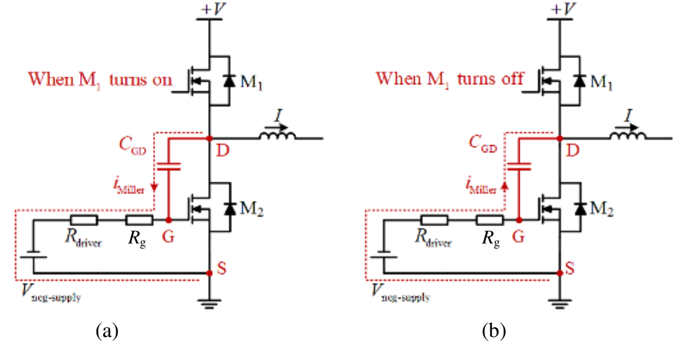


Fig. 22. Cross-talk effect during turn-on and turn-off of the top device. (a) Top device turn-on. (b) Top device turn-off.

The gate voltage V_{GS} can therefore be expressed as in (1) where the Miller current can be calculated by (2) approximately.

$$V_{GS} = i_{Miller} \cdot (R_{driver} + R_g) + V_{neg-supply} \quad (1)$$

$$i_{\mathrm{Miller}} = C_{\mathrm{GD}} \cdot \frac{dV_{\mathrm{DS}}}{dt} \quad (2)$$

where, V_{DS} is the drain-source voltage of the bottom switching device M2.

There is an interesting question associated with the cross-talk effect during the top device turn-on transition. Assuming the gate resistor values are the same for the top and bottom switching devices, as the value of the gate resistor (R_g) gets smaller, the switching speed will get faster which results in

higher dV_{DS}/dt and hence larger i_{Miller}. However, since the gate resistor value is reduced, will the voltage drop on the gate resistor get higher or lower? The combined effect of these two factors on the voltage drop and thus the cross-talk effect needs to be investigated. Fig.23(a) shows the measured gate voltage for various gate resistance values ranging from 2.5Ω to 25Ω. As seen, while the gate voltages rise from -5V but the peaks are all below 0V, and thus there is no false turn-on. The peak voltages are very similar for various gate resistance values. Also, it should be noted that there are clear negative spikes due to the oscillation of the gate circuit, which may exceed the maximum allowable negative voltage of the device which in this case is -10V [50].

Similar to the cross-talk effect during the top device turn-on transition, when the top device turns off, it may cause an undershoot (negative voltage) on the gate voltage of the bottom device as illustrated in Fig.22(b). This negative voltage adds to the -5V of the bottom device gate voltage, which may potentially exceed the minimum allowable gate voltage, i.e. -10V, and affect the gate reliability of the MOSFET. Fig.23(b) shows the gate voltage during the top device turn-off. As the gate resistance gets larger, the negative voltage overshoot gets larger as well, exceeding -10V with gate resistance values of 10Ω and 25Ω. Also, the overshoot is affected by the load current level which has been discussed in [50]. While most of the existing research focuses on the turn-on cross-talk effect, the turn-off cross-talk effect should also receive attention in regards to the gate reliability. It should also be noted that the measured gate voltage may be slightly different to the actual voltage between the MOSFET gate and source due to the parasitic elements in the device packaging such as the source parasitic inductance.

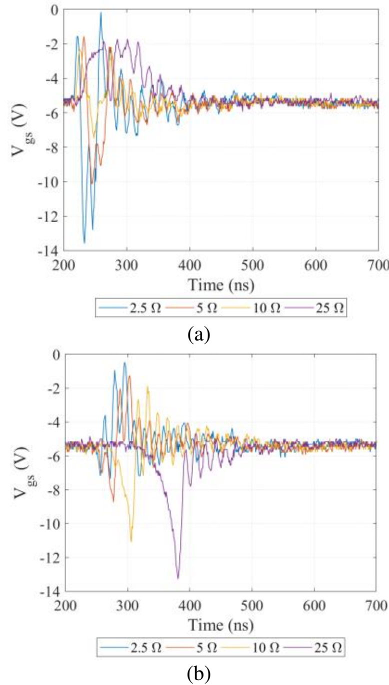


Fig.23. Bottom device (Wolfspeed C2M0040120D SiC MOSFET) gate voltage due to cross-talk effect with a load current of 20A. (a) Bottom device gate voltage during top device turn-on. (b) Bottom device gate voltage during top device turn-off.

As seen in Fig.23, there are clear oscillations in the gate loop which will make its design challenging when applied to the high-speed switching of SiC devices. For example, to turn on a device as fast as possible, the gate voltage has to rise very quickly. Therefore, the gate loop inductance must be minimized to avoid large resonance between the loop inductance (L) and the gate capacitance (C_{GS}) shown in Fig.24. The recommended gate voltage range for SiC MOSFETs is between -5V and +20V and the maximum allowable range is between -10V and +25V, which is likely to be exceeded if the gate loop inductance is high. Fig.25 shows a gate voltage waveform in an experimental test, where the peak of the oscillation has exceeded +25V; well above the 20V reference. Although the gate resistance can be increased to add damping to the gate circuit loop, it will slow down the switching speed.

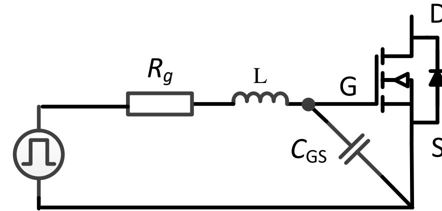


Fig.24. Gate loop equivalent circuit.

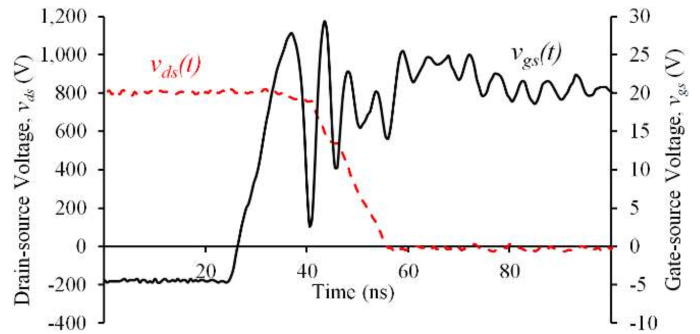


Fig.25. Gate-source voltage during turn-on [51].

Therefore, the gate driver circuit has to be put as close as possible to the MOSFET gate if a high switching speed is to be achieved. As an example, the gate driver boards in Fig.12 and Fig.13 have been arranged perpendicular to the power devices, to be as close as possible to the device pins. Other techniques for high-speed gate driver circuits include using separate source pins for the gate loop and power loop (Kelvin connection) or using resonant type gate drivers [51].

Although there are challenges as mentioned above, with skilled design, very fast switching can be achieved successfully with minimum external gate resistance. For example, [46] has demonstrated switching waveforms of SiC MOSFETs tested with zero (no) external gate resistance. The switching transient can be completed within around 30ns.

Also note that the internal gate resistance of SiC MOSFETs is normally higher than that of Si MOSFETs. The value of the internal gate resistance depends on the sheet resistance of the gate electrode material and the chip size. For a given design, the resistance is higher for smaller chips. For devices with equivalent performance, a SiC-MOSFET chip is smaller

compared with a Si-MOSFET, the internal gate resistance of the SiC MOSFET is therefore higher.

The challenges regarding gate driver design for high-voltage (e.g. 10kV) SiC devices and the use of transformer-based, optical based or wireless based gate drivers can be found in [52-56].

C. High-frequency magnetic components

One of the motivations of using SiC devices is to reduce the volume of passive components such as inductors and capacitors, noting that these passive components take around 30%~50% of the total volume or weight of a typical power electronics converter. Although the increase in frequency can reduce the required value of the inductors and capacitors, it does not necessarily reduce their volume and weight. For example, increasing the switching frequency will increase the high frequency losses in the inductors. Also, reducing the volume of the inductors will lead to a smaller surface area, resulting in a lower thermal dissipation capability. Hence, the volume and weight of the inductor does not reduce in inverse proportion with the increase of frequency. Therefore, an accurate high-frequency core loss and winding loss model is critical for estimating the losses. [57, 58] have shown a loss-map based method to accurately predict the high-frequency winding loss and core loss for high power inductors by considering dc offset, square-type PWM waveforms and varying duty cycles. Also, combined electromagnetic, thermal and mechanical multi-physics design and optimization is needed for accurately sizing the inductors.

Fig.26 illustrates how the magnetic component value and volume/weight varies with frequency. The figure also shows how various techniques can be used to achieve desired switching frequencies such as hard-switched Si IGBT based converters, hard-switched SiC MOSFET based converters, multilevel converters and soft-switching/resonant-switching converters. Note that, with very high frequencies and low inductance values, air-core inductors can be used which avoids high-frequency core-loss and reduces the weight.

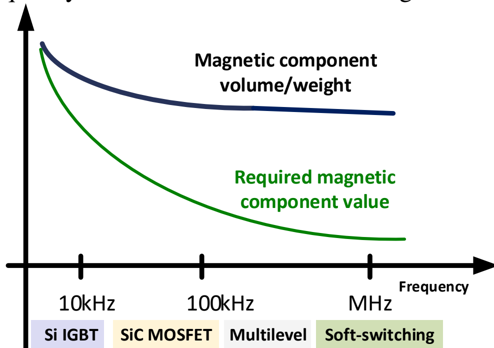


Fig.26. Variation of magnetic component value and volume/weight with (switching) frequency.

For high power, high-frequency magnetic components, candidate magnetic materials include Ferrites, Nanocrystalline laminated/powder material, Amorphous alloy, etc [59]. Table II shows the properties of various magnetic materials, including saturation flux (B_{max}), permeability (μ_e), typical frequency range (f_{typ}) and core loss level.

Also, the parasitic capacitance of components such as inductors must be minimized to reduce the current overshoot, oscillations, etc produced under high dv/dt. [60] has modeled the parasitic capacitance of an inductor and investigated how to reduce an inductor's parasitic capacitance through conductor placement.

TABLE II. SUMMARY OF MAGNETIC MATERIALS

Material	Type	B_{max} (T)	μ_e (–)	Shapes	f_{typ} (kHz)	Core losses
Vitroperm 500F 14–20μm	Nano-crystalline laminated	1.23	22000	Toroids C	<200	Low
Metglas 25 μm	Amorphous laminated	1.56	45000	Toroids C	<100	Medium
Finemet 15-18μm	Nano-crystalline laminated	1.23	30000	Toroids C	<200	Low
Mn-Zn Ni-Zn	Ferrite	0.5	2400	Wide range	>10	Low
MPP Hi-flux X-flux Sendust	Powder core	0.8-1.6	Variable	Wide range	<300	Medium
SWAP	Nano-crystalline powder	1.25	Variable	Toroids	>200	Low
Vacoflux 48	Laminated	2.4	18000	Custom	<100	Medium

D. Converter-load interference

At the converter or system level, one challenge is the impact of the high dv/dt ouput voltage on loads such as electric machines (motors or generators), transformers (for grid-connection), connecting cables, etc. Taking a motor drive application as an example, high dv/dt can lead to an overvoltage (can be doubled or even higher) at the motor terminals due to the cable transmission line effect [61-63] as the dv/dt can normally reach 20kV/μs. With the high switching speed of SiC devices, the critial length of the cable, when significant overvoltage is taking place, will reduce from tens of meters for Si IGBT converters to several meters for SiC converters. Fig.27 shows an experimentally measured SiC converter output voltage and the terminal voltage of an induction motor with a 1.6m cable. As seen, the voltage at the motor terminal has reached 1000V, which is 400V more than the original 600V at the converter output.

This overvoltage will increase the stress on the motor winding insulation, potentially causing partial discharge and insulation failure [64]. Also, under high dv/dt, the majority of the machine terminal voltage will drop on the first or first several turns of the stator winding during transient due to the high-frequency parasitic effect. Hence the insulation stress of the first several turns will be very high, leading to a potential insulation breakdown. Furthermore, research has shown that the gradual ageing of insulation systems take place due to space charge injection into the insulation system [65]. Each voltage transition causes a specific amount of degradation and the high switching frequency of SiC converters means that this

is rapidly repeated and thus leads to a reduced insulation lifetime. Therefore, the insulation degradation must be considered under high d*v*/d*t*, high switching frequency SiC converters.

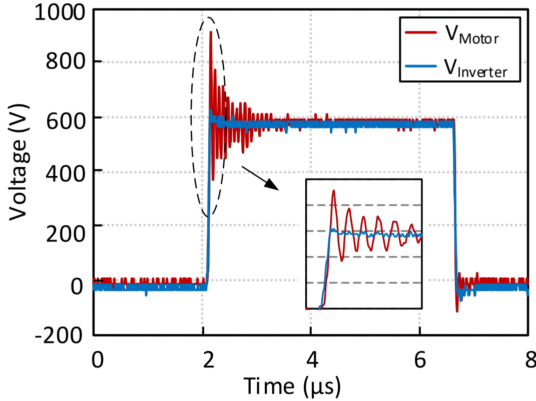


Fig.27. SiC inverter output voltage and overvoltage at the motor terminal. V_{motor}: motor terminal voltage; $V_{inverter}$: inverter output voltage.

A very similar effect happens to the motor bearings under high d*v*/d*t* and high switching frequency. The increased amplitude of the common-mode (CM) voltage and its high changing rate lead to an increased level of capacitive-type bearing charging current and a higher possibility of EDM (Electric Discharge Machining)-type motor bearing current, causing motor bearing degradation. The EDM bearing current is more severe for bearing damage, analogeous to the partial discharge effect for the insulation [66]. Fig. 28 shows an experimentally measured CM voltage, shaft voltage and bearing current (EDM type and *dv/dt* type (capacitive-type)) of an induction motor driven by a SiC converter. The amplitude of the EDM current is higher than the d*v*/d*t* driven capacitive current. Fig.29 shows a comparsion of the motor shaft voltage and the capacitive-type bearing current between a SiC MOSFET converter and a Si IGBT converter. The Si IGBT converter operates at 10kHz with a dc-link voltage of 580V as shown in Fig.29(a). The SiC MOSFET converter operates at 100kHz with a dc-link voltage of 600V as shown in Fig.29(b). As seen, the frequency and amplitude of the capacitive bearing current are higher for the SiC MOSFET converter than for the Si IGBT converter. Whether the d*v*/d*t* driven capacitive-type current becomes another main cause of bearing failure needs further investigation.

The bearing and insulation issues have been observed in IGBT based motor drives. SiC converters, with switching speeds and switching frequencies that are an order of magnitude higher, will aggravate these issues and need to be carefully addressed during the system design.

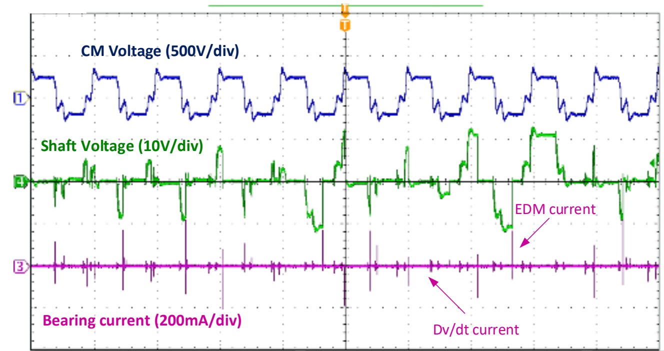
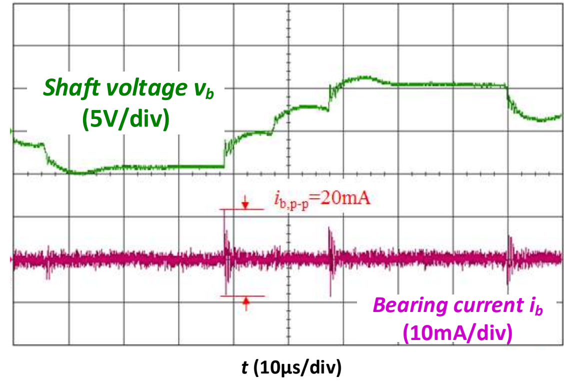
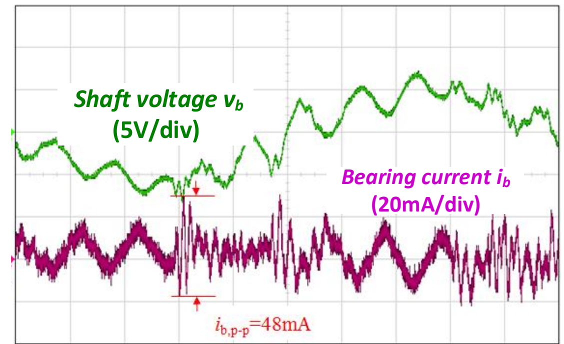


Fig.28. Motor common-mode (CM) voltage (the voltage between motor stator winding neutral and ground), shaft-voltage (the voltage between motor shaft and ground), motor bearing current (including both the dv/dt-driven capacitive current and EDM current).



(a)



(b)

Fig.29. Motor shaft voltage and bearing current with a Si IGBT converter and a SiC MOSFET converter. (a) With a Si IGBT converter, dc-link voltage =580V, switching frequency=10kHz. (b) With a SiC MOSFET converter, dc-link voltage=600V, switching frequency=100kHz.

Another issue that occurs under high d*v*/d*t* is due to the cable capacitance. Fig.30 shows the effect of the cable (e.g. connection between a SiC converter and load) capacitance on the switching device current. When the switching device turns on, it will charge the cable parasitic capacitance. The faster the switching speed is, the larger the charging current will be. In Fig.30, 'Normal' means the converter is connected to a standard load with a small capacitance. 'With cable' means a cable is connected between the converter and the load (e.g. an electric motor). As seen, with the cable connected, the current spike is much higher than the 'Normal' case due to the cable

capacitance. The current spike can increase the switching device turn-on loss and reduce the converter efficiency. Also, the frequency of the oscillation in the current is much lower than the 'Normal' case, which means larger filters may be needed to attenuate the harmonics. The 'with inductor' cases in the figure will be discussed in Section IV of the paper.

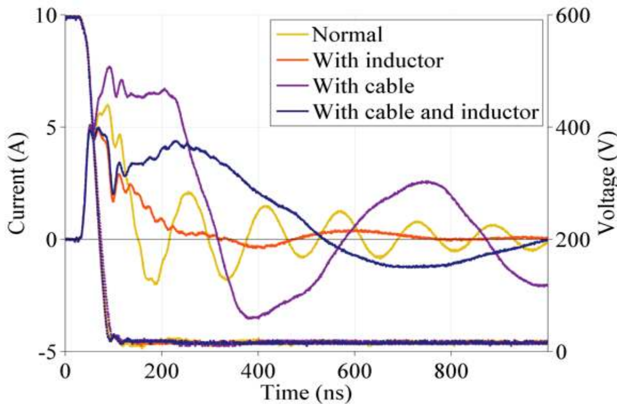


Fig.30. Power device turn-on current under normal loads or with cables [67].

E. *Deadtime, control, fault detection and protection, measurement and converter capacity challenges*

For high-switching-frequency converters, the use of deadtime between the complementary switching devices in a phase leg may cause low-frequency harmonics, voltage drop and additional losses. These deadtime effects become more severe as the switching frequency gets higher, even though the duration of deadtime for SiC MOSFETs can be set much smaller than would be needed for Si IGBTs. Effective deadtime compensation/elimination strategies can be adopted [68] to extend the linear modulation region. [69] has investigated how to set the optimal (minimum) deadtime for SiC converters.

The increased switching frequency of SiC devices can enable higher control bandwidth. There are concerns whether control algorithm can still be completed within each short switching period. Firstly, for a lot of applications such as some motor drives, there is no strong need to increase the control bandwidth (dynamics), and therefore, the control algorithm can be implemented over several switching periods, rather than each switching period. Although the control bandwidth is not increased, the benefit of increasing the switching frequency is the reduction of current/voltage ripple, and hence the harmonic induced losses in motors. On the other hand, if the control does need to be implemented within one switching period to achieve high control bandwidth, e.g. in switching mode power supplies, efforts need to be made to reduce all the delays including calculation, sampling, PWM delay, etc.

The protection of SiC devices and converters also faces challenges due to its limited short-circuit current withstand capability [70, 71]. Typically, Si IGBTs can withstand a short-circuit current for around 10 μs. This gives sufficient time for over-current detection and protection circuits to turn-off the Si IGBTs. For example, in low-cost applications, relatively low bandwidth (10s to 100s of kHz) current sensors, which are already installed for load current measurement for control purposes, can be used for Si IGBT overcurrent detection and protection during load-side short circuit, e.g. in motor drive systems. However, the short-circuit withstand time has been reduced for SiC devices, e.g. to 2μs due to a smaller chip area and device short-circuit characteristics. Therefore, low-bandwidth current sensors may not be quick enough when it comes to detecting and protecting SiC MOSFETs from faults. During short-circuit (shoot-through) failure, the SiC MOSFET current will rise rapidly and the device voltage drop (V_{DS}) will clearly increase as well. Therefore, the widely used desaturation protection method (DESAT) based on the measurement of MOSFET voltage drop can be used. The detailed design of a desaturation based protection circuit can be found in e.g. [72] and it has also been used in commercial SiC MOSFET gate drivers for shoot-through protection such as the CGD15HB62P1 gate driver board from CREE/Wolfspeed. Given a fast protection time under 2μs is normally recommended, the triggering voltage level of the desaturation circuit needs to be carefully selected to respond fast while not mistriggered by noise. There are also other methods being proposed for current measurement and protection for SiC devices such as the Si MOSFET current shunt, embedded Rogowski coils [73-75].

High speed, high bandwidth, non-intrusive current and voltage measurement is another challenge when characterizing the SiC devices, which is even more challenging with GaN devices where the switching time is generally within 10 ns. A detailed comparison of various measurement techniques such as split core current probes, Rogowski coils, co-axial currents shunt and current transformers can be found in [76, 77].

In order to increase the current and voltage capabilities of existing SiC discrete devices and power modules, the parallel and series connection of SiC devices has been used. The current and voltage sharing between the devices under high switching speed is another challenge, especially where more than three devices need to be connected in parallel or in series [78, 79].

IV. POTENTIAL SOLUTIONS FOR HIGH FREQUENCY SIC CONVERTERS

As seen in previous sections, the side-effects of high frequency and high d*v*/d*t* may cause a series of issues at both the component and converter level. There are generally two approaches to tackle these challenges: one is from the source and the other is from the load side or adding filters. Some representative solutions are summarized below.

Firstly, snubber circuits, filters, ferrite beads as well as skilled circuit design, can be used to address some of the above issues. [80] has investigated the DC-link RC snubber design for SiC MOSFET applications to attenuate the turn-off voltage overshoot and oscillations, where the model and optimal parameters of the RC snubber across the dc-link are given. [81, 82] discuss the use of snubber circuits for SiC MOSFETs and the effect of external snubber capacitors for soft-switching operation of SiC MOSFETs. d*v*/d*t* limiters, sin

wave filters or other types of filters such as LCL filters can be used to limit the d*v*/d*t* and filter the switching-frequency harmonics as presented in [67, 83, 84]. This also helps to reduce the impact of high d*v*/d*t* and high-switching frequency on the load. [33] shows the use of ferrite beads in the switching loop to effectively attenuate the oscillations and improve switching stability. The use of larger gate resistances can effectively solve a lot of high-frequency issues at the cost of slower switching speed, hence higher switching losses. From the circuit design point of view, the parasitic inductance in the communtation loop must be minimized. As mentioned, [46] has demonstrated a circuit design which can achieve very fast switching of SiC MOSFETs (<30ns) with no external gate resistance.

Secondly, various topologies can be used to mitigate the d*v*/d*t* effect, cross-talk, EMI issues, etc from the source. For example, the split output topology with embedded inductors can reduce the output d*v*/d*t*, current overshoot, EMI and cross-talk effect [85]. The common-mode (CM) current passing through the system's parasitic capacitance will increase due to the high d*v*/d*t* of SiC devices, which can cause EMI, leakage current and other issues. Various exisiting topology solutions for Si devices can be adoted to tackle the CM EMI for SiC converters [62, 86-90]. Multilevel and soft-switching topologies can reduce the output d*v*/d*t*, EMI and the negative impact on the load due to the smoothed output voltage (soft-switching) [91] and more output voltage steps (multilevel) [92]. [63] has shown a quasi-three-level approach to attenuate motor terminal overvoltage. Furthermore, soft-switching topologies and multilevel topologies can benefit from the use of SiC devices, e.g. to reduce the turn on/off delay or increase the number of switching actions for balancing capacitor voltages, which will be explained in more detail in Section IV. D.

Thirdly, the gate driver plays an important role in controlling the switching profile of SiC MOSFETs. The gate driver circuit needs to be put as close as possible to the gate/source pin of the SiC MOSFET to reduce the parasitic inductance in the gate loop and thus reduce oscillations and voltage overshoot if a very high switching speed is to be achieved. SiC MOSFETs with Kelvin connections have been introduced, where a dedicated Kelvin source pin is created for the gate driver, which can reduce the parasitic inductance in the gate loop [93]. Also, as mentioned, resonant gate drivers can be used to facilitate very fast switching, which is not constrained by the parasitic inductance in the gate loop [51]. The gate voltage for SiC MOSFETs is normally +20V/-5V for ON/OFF states rather than +15V/-5V for Si IGBTs. In order to mitigate the cross-talk effect, special gate drivers can be designed to clamp the gate voltage [49]. Shaping the SiC MOSFET voltage through gate control (active gate drivers) has been extensively investigated recently. A more 'smoothed' device output voltage can reduce oscillations, current/voltage overshoot, cross-talk effect and EMI issues, which will be discussed more in Section IV. C.

In the following, some effective and special approaches related to SiC devices and converters to address the mentioned challenges will be discussed in more detail.

*A. Adding an output inductor (*d*v*/d*t limiter)*

To address the issues related to the converter-load interference experienced under high d*v*/d*t*, a small inductor (one per phase or a three-phase inductor) can be added at the output of the SiC converter to decouple the higher frequency behavior of the converter and the load as shown in Fig.31. The inductor here is only intended to limit the d*v*/d*t* (d*v*/d*t* limiter) seen at the output of the converter, i.e. filtering out the very high frequency component so the inductance value can be small, which can be achieved by an inductor with a small number of winding turns or without a magnetic core (air-core inductor). With this d*v*/d*t* limiter, the SiC device turn-on current overshoot due to the charging of the load (including cable, motor, transformer, etc) parasitic capacitance and the associated ringing can be reduced. For example, as shown in Fig.30, in both 'with inductor' and 'with cable and inductor' the charging current and ringing have been attenuated compared with the cases where no inductors are used, i.e. 'normal' and 'with cable'. The inductor here refers to the d*v*/d*t* limiter. Fig.32 shows the switching device turn-on energy with and without the d*v*/d*t* limiter (inductor). As seen, with the d*v*/d*t* limiter, the switching energy has been reduced from 74μJ to 68μJ and from 102μJ to 85μJ, respectively, correponding to the cases shown in Fig.30. Also, this d*v*/d*t* limiter will mitigate issues mentioned in motor drive applications such as the stress on the electric machine winding insulation, bearing current, etc.

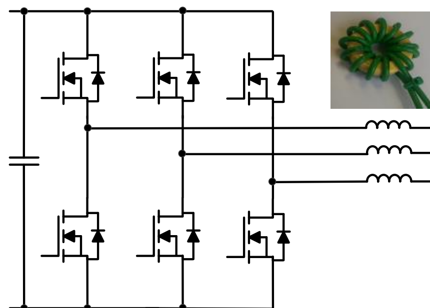


Fig.31. A SiC MOSFET based converter with an output *dv*/d*t* limiter.

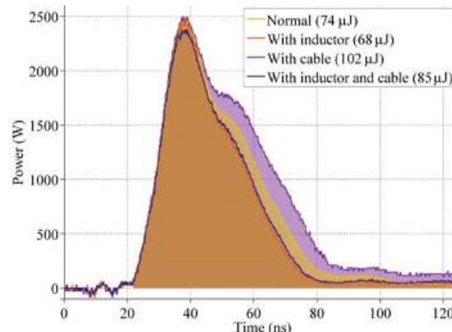


Fig.32. Switching device turn-on energy reduction by adding the d*v*/d*t* limiter.

It should be noted that this output d*v*/d*t* limiter does not help with the converter internal issues caused by the high d*v*/d*t* such as charging the output capacitance of the complementary

switching device and the PCB parasitic capacitance, cross-talk effect, etc.

B. Alternative topologies

Standard converter topologies such as the hard-switched three-phase two-level converter may not be the best to fully exploit the potential of SiC devices due to the side-effects of high d*v*/d*t*. Adjusted topologies or new topologies may be more suitable for SiC devices. Fig.33 shows a split output topology, where each phase has been split by embedded inductors (*L*s1 to *L*s6) [85, 94]. This topology can help to attenuate the current overshoot, ringing and cross-talk effect. The split inductor can also serve as a d*v*/d*t* limiter.

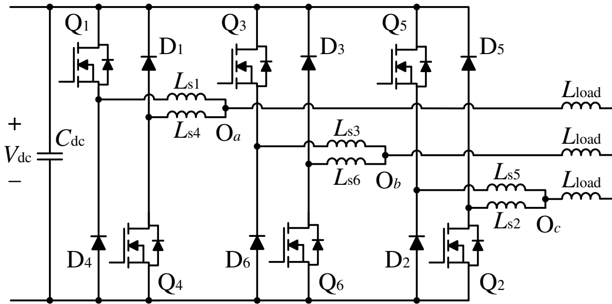


Fig.33. A split output converter topology for SiC power devices.

Fig.34 shows the switching device's gate voltage at the OFF state during the complementary device turn-on transition for a split inductor value of 10μH. As seen, the gate voltage rise is only 1.8V, much smaller than that (3.2V) of a conventional topology as illustrated in Fig.22(a). This means that the cross-talk effect is mitigated.

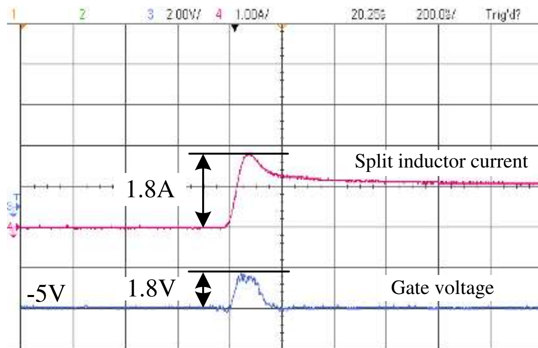
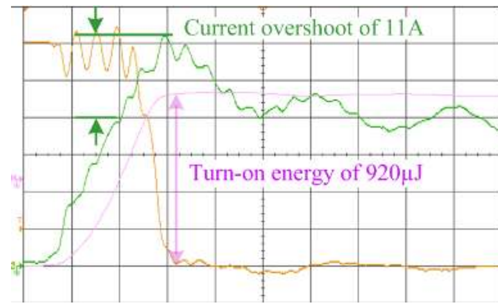
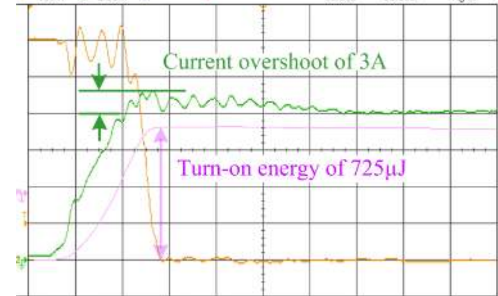


Fig.34. Gate voltage at OFF state during the complementary device turn-on (cross-talk effect) with the split output topology.

Fig.35 shows the switching device turn-on current and energy with and without the split inductors. Without the split inductor (Fig.35(a)), the topology becomes a standard two-level three-phase converter. As seen, the current overshoot and turn-on energy are significantly reduced with the split output structure (Fig.35(b)).



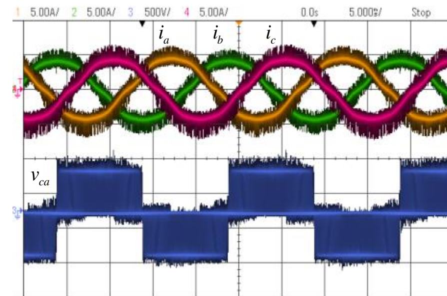
(a)



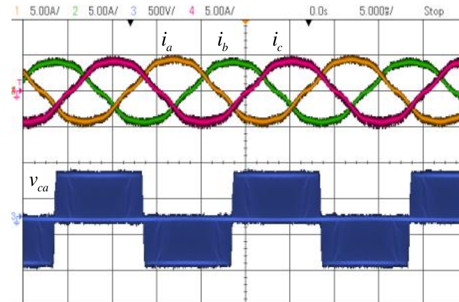
(b)

Fig.35. Switching device turn-on current and energy. (a) Without the split inductor. (b) With the split inductor.

Fig.36 shows the converter output currents and voltages with a standard R-L load. As seen in Fig.36(a), without the split inductor (standard topology), the current and voltage have clear high frequency components due to the charging of the load parasitic capacitance. In comparison, with the split output topology (Fig.36(b)), the current and voltage waveforms are 'clean', which means the split inductor has mitigated the load's parasitic effect that is produced under high d*v*/d*t*.



(a)

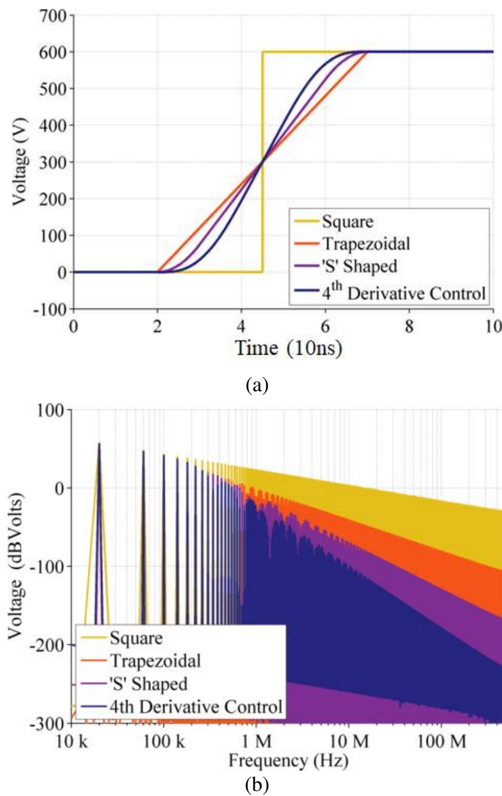


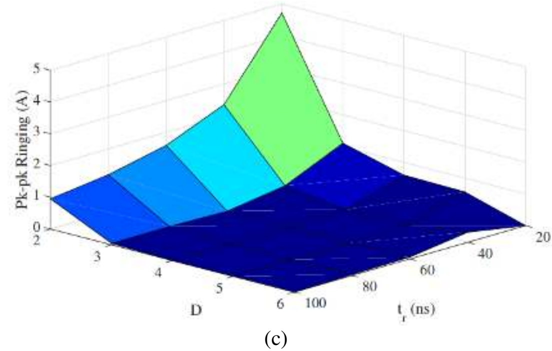
(b)

Fig.36. Converter output current (top) and voltage (bottom). (a) Without the split inductor. (b) With the split inductor.

C. Waveform shaping through gate control

As mentioned before, the sharp edges and corners of fast switching transients can cause an increased level of EMI, current overshoot and ringing, and stress on the load. However, it may be possible to shape the switching waveforms to attenuate the high-frequency components without increasing the switching loss. Fig.37(a) shows four waveforms (square, trapezoidal, 'S' shaped and a more smoothed one with 4th derivative control) [48]. The 'trapezoidal' waveform is a common switching waveform with sharp corners and linear edges. However, if the waveform can be shaped to more smoothed ones such as the 'S' shaped or '4th derivative control', then the high frequency components will be reduced as shown in Fig.37 (b), leading to reduced current overshoot, ringing and EMI. In theory, the three waveforms discussed here (trapezoidal, 'S' shaped, 4th derivative control) should generate the same switching loss due to them having the same switching time. This is more advantageous than simply slowing down the switching speed by using a larger gate resistance which increases the switching losses. Fig.37 (c) further shows the variation of the amplitude of the ringing with the switching time and waveform smoothness. More smoothed waveforms with high derivatives (D) and longer switching time can lead to a reduced amount of ringing. The waveform shaping may be achieved through active gate control or soft-switching circuits.





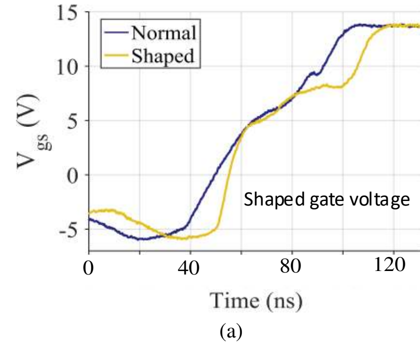
(c)

Fig.37. High frequency attenuation through waveform shaping. (a) Various shaped waveforms. (b) Harmonic spectra of various shaped waveforms. (c) Ringing amplitude under various waveform smoothness and transition time [48].

For example, the gate driving voltage can be shaped/programmed to a specific form that can lead to a smoothed output voltage and current for the switching device. This requires advanced gate drivers with programmable driving impedance/voltage, e.g. by switching on/off a series of gate resistors (switch and resistor arrays), multi-level gate voltage or current source based gate drivers [95-101]. Also, relatively simple passive component based gate drivers can be used for shaping the output voltage with limited resolution [102, 103].

Note that under various (e.g. current, temperature) conditions or with different power devices, the gate voltage required to achieve smoothed waveforms may be different. Therefore, knowing how to adjust the gate voltage pattern according to various conditions is a challenge. Switching-transient based closed-loop waveform-shaping control is very challenging due to the very short switching transient time, typically in the range of tens of ns, which requires a very high sensing and control bandwidth. A more practical method is to use a pre-defined gate-pattern look-up table, which is created and used according to the load current level with a lower control bandwidth requirement.

Fig.38 shows that by using shaped gate voltage (yellow) as in Fig.38(a), the current overshoot in Fig.38(b) can be reduced and the output voltage in Fig.38(c) can be smoothed relative to the 'normal' case.



(a)

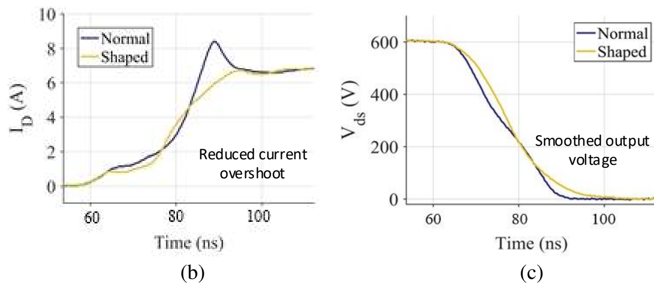


Fig.38. Switching device output voltage and current waveform shaping by using modified gate voltage. (a) Gate voltage. (b) Switching current. (c) Switching voltage.

D. Multilevel and soft-switching techniques for SiC devices

SiC devices achieve lower switching losses by switching faster, however this comes at the cost of increased EMI and negative side-effects generated by high d*v*/d*t*. It is desirable for both the low switching loss (high efficiency) and reduced EMI to be achieved at the same time. Multilevel and soft-switching techniques solve these two aspects simultaneously, albeit at the cost of increasing the number of components. Multilevel converters have lower output harmonics and lower d*v*/d*t* due to more levels (steps) in the output voltage. Multilevel converters also have lower switching losses because each device only needs to switch a portion of the total dc-link voltage as opposed to the full dc-link voltage in a two-level converter. The switching losses can be reduced even further by using SiC devices, with their fast switching speed, in a multilevel converter. Doing so will also reduce the output d*v*/d*t* below that produced by an equivalent two-level converter.

Another opportunity afforded by high voltage SiC devices (e.g. 10kV) is that they can reduce the number of power devices needed for a given number of output voltage levels. For example, for the four-level π-type converter shown in Fig.39 [104], only 6 devices are needed to achieve a four-level output, which is the minimum number of devices. Although the devices in the T1 and T2 positions need to block the whole dc-link voltage, SiC devices with higher voltage ratings can be used in these places. Another issue with simplified topologies, like the one in Fig.39, is that the dc-link capacitor voltages cannot be balanced at high modulation indexes and high power factors with conventional space vector modulation or carrier-based zero-sequence signal injection. This is also the case for four-level or higher level neutral point clamped (NPC) converters or other simplified topologies. The virtual space vector modulation [105] or redundant level modulation [106] however can achieve dc-link capacitor voltage balancing at the cost of an increased number of switching actions and consequent increased switching loss. Given that wide-bandgap (e.g. SiC) devices have very low switching energy, the switching loss due to the increased switching actions may not increase by much. Hence, there is a great opportunity for SiC devices in multilevel converters with simplified topologies and balanced dc-link capacitor voltages.

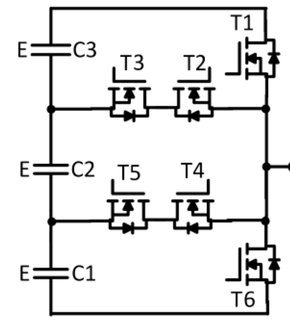


Fig.39. A four-level π-type converter based on SiC MOSFETs.

Since wide-bandgap devices have low switching losses, they can be used at a high switching frequency. There is a question whether soft-switching techniques are still needed for wide-bandgap devices to reduce the switching loss by decoupling the voltage and current switching transitions (zero voltage/current switching). On one hand, to achieve very high-switching frequencies (e.g. MHz+), soft-switching is still needed for wide-bandgap devices. Furthermore, since the soft-switching converter works in a resonant mode, the output voltage is smoothed so that the high frequency harmonic components are attenuated [107]. Therefore, using SiC devices in soft-switching converters can achieve both lower switching loss and EMI at the same time. Also, compared with Si IGBTs, SiC MOSFETs have a much smaller turn-on delay and no tail current. SiC MOSFET based soft-switching converters can achieve ideal soft-switching waveforms [108]. If a shorter switching transition time is needed for SiC soft-switching converters, the required size of resonant components, such as auxiliary inductors and capacitors, can also be reduced. This will help to improve the system power density. Fig. 40 shows the experimental waveforms of a soft-switching auxiliary resonant commutated pole inverter (ARCPI) using either SiC MOSFETs or Si IGBTs. As seen, with SiC MOSFETs the device current (i_{s4}) and resonant current (i_{Lr}) is reduced due to a smaller turn-on delay, which can reduce the losses in the components.

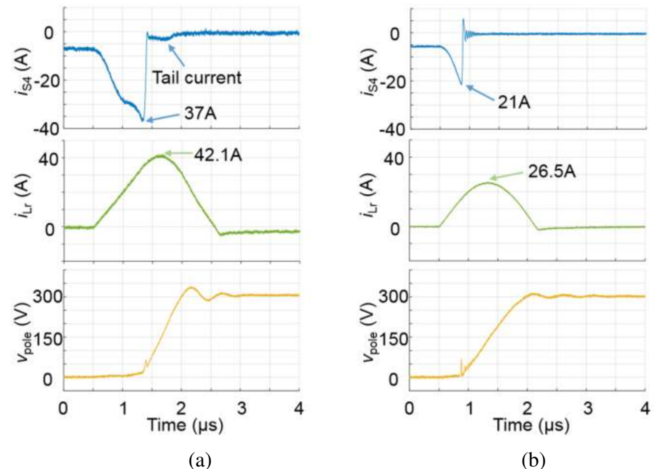


Fig.40. Switching waveforms of the auxiliary resonant commented pole inverter (ARCPI): i_{s4} main switching device current, i_{Lr} auxiliary inductor current, v_{pole} converter output voltage. (a) with Si IGBTs. (b) with SiC MOSFETs.

In addition, with soft-switching, the output voltage rise time can be actively controlled to produce a longer transition time that will reduce the voltage overshoot at the motor terminals by mitigating the long cable effect [91]. This will help reduce the motor insulation stress and bearing stress. The reduced d*v*/d*t* of multilevel converters can also achieve similar effects.

E. Holistic Design Optimization

The best system-level benefits that come from using SiC devices can only be achieved if a holistic design optimization approach is used, where various component models are linked together to evaluate the design trade-offs for various design objectives such as efficiency, power density, reliability. For example, in regards to power density, increasing the switching frequency can reduce the required size of the line filters such as the line inductors and capacitors, but it will increase the switching loss, hence the required size of heatsink while also increasing the EMI level and the size of corresponding EMI filters. These trade-offs need to be evaluated during the design. SiC converters have allowed the switching frequency to reach ~100kHz with hard-switching, and the optimal switching frequency to achieve the maximum efficiency, power density, etc. within this range can only be identified if a holistic optimization approach is used. [35, 109] presented such a holistic design optimization tool. This tool can also be used to evaluate the impact of various topologies (e.g. two-level vs. multilevel) and the junction temperature limit (e.g. 125°C with Si devices vs. 150/175/225 °C with SiC devices) on the optimal system design and the component and parameter selection [110]. A holistic design optimization tool, such as this, is therefore needed to achieve the overall optimal design for SiC-based converters.

F. Packaging and Thermal Management

There are two main areas that research have been done for the packaging for SiC devices. The first is to optimize the packaging for reducing parasitics for high speed switching. The second area is improved packaging for better heat dissipation, thermal management, integration and high temperature operation.

Surface mounted SiC MOSFETs have been introduced to reduce the device footprint, parasitic inductance due to less pin connections and enable a more automated soldering process [111]. A low-cost QFN package for a SiC half-bridge module has been made to reduce the parasitic inductance [112]. For these surface mounted packages, heat is dissipated through PCB copper vias, metal core or AlN inlay, and a heatsink is mounted on the other side of the board to extract the heat. Presspack packages have been used for SiC MOSFETs to reduce parasitic inductance or eliminate wire-bonding and die-attach and can be used for high power and high temperature applications [113-116]. High temperature packaging solutions, e.g. using AlN substrate to enable high-temperature operation capability of SiC devices up to 500°C has been presented in [7, 117].

Regarding thermal management and integration, various mechanical, embeded structures have been proposed for integrated converter systems such as ‘converter in package’ to capitalise on the high frequency operation of SiC devices [118-120]. A 3D packaging structure has been created with heatsinks on both sides to better dissipate the heat [121]. [122] presents the performance of a loop thermosyphon-based thermal management system (TMS) for SiC converters. The TMS can extract a large amount of heat from the device junction and is able to maintain a low junction temperature frequency ripple resulting in an increase in the module’s lifetime. [123] examines the thermal impact the chip thickness and heatsinking has on various WBG and ultra WBG (UWBG) materials. Thermal conductivities considered range from 11 W/mK for β-Ga_2O_3 to 2200 W/mK for diamond. Above 400 W/mK the effect of the device’s thermal conductivity is negligible compared to the effect of the packaging and heatsink. [124] provides an overview on SiC device reliability issues relating to thermal, packaging and other aspects.

V. CONCLUSIONS

SiC power devices with their fast switching speeds can significantly improve the system efficiency and power density. For example, they can enable a 1.2MW/m^3 power conversion capability using only forced-air cooling. However, the high d*v*/d*t* and high switching frequencies that they are typically operated at have a series of challenges that need to be overcome in order to realize their full potential. Some solutions have been pointed out in this paper that help tackle these challenges and thus can accelerate the adoption and application of SiC devices and converters. It is expected that this tutorial paper will be a useful reference for power electronics engineers when it comes to designing SiC converters.

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