Optical interferometric logic gates based on metal slot waveguide network realizing whole fundamental logic operations

Deng Pan,[1] Hong Wei,[1] and Hongxing Xu[1,2,3,*]

[1]*Beijing National Laboratory for Condensed Matter Physics and Institute of Physics, Chinese Academy of Sciences, Box 603-146, Beijing 100190, China*

[2]*School of Physics and Technology, Wuhan University, Wuhan 430072, China*

[3]*Division of Solid State Physics/The Nanometer Structure Consortium, Lund University, Box 118, SE-22100 Lund, Sweden*

[*]*hxxu@iphy.ac.cn*

Abstract: Optical interferometric logic gates in metal slot waveguide network are designed and investigated by electromagnetic simulations. The designed logic gates can realize all fundamental logic operations. A single Y-shaped junction can work as logic gate for four logic functions: AND, NOT, OR and XOR. By cascading two Y-shaped junctions, NAND, NOR and XNOR can be realized. The working principle is analyzed in detail. In the simulations, these gates show large intensity contrast for the Boolean logic states of the output. These results can be useful for future integrated optical computing.

OCIS codes: (250.5403) Plasmonics; (230.7370) Waveguides; (200.4660) Optical logic.

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#184170 - $15.00 USD Received 24 Jan 2013; revised 13 Mar 2013; accepted 13 Mar 2013; published 10 Apr 2013

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1. Introduction

As is known, semiconductor-based electronic devices will reach their limit in near future. Photonic devices and circuits have been proposed to break this limitation, benefiting from the fast speed and low heat producing properties of photons [1]. The elementary units of electronic circuits are transistor based Boolean logic gates. In photonics circuits, logic functions can be realized by linear interferences [2–4] or by nonlinear optical processes [5,6]. For linear optical logic gates, the constructive or destructive interference of the input signals yields corresponding logic operation results, which show merits of good stability and extensibility.

The integration of the photonic devices is limited by diffraction of light. Surface plasmon polaritons (SPPs), which are localized surface electromagnetic waves at the interface of metal and dielectric, can be applied to overcome this limitation. Many kinds of plasmonic waveguides [7–10] and devices [11–16] have been proposed. We recently in experiment realized optical Boolean logic gates based on propagating plasmons on silver nanowires, and showed the integration potential by realizing NOR gate through cascading OR and NOT gates [15,16]. Compared with silver nanowires, the metal slot waveguides show good field confinement, and can be easily integrated to complex structures and networks. Therefore, slot-waveguide-based plasmonic devices have large potential to be employed for on-chip integration. Recently, optical logic gates in metal slot waveguides have been proposed [17]. However, the working principle of this kind logic gates has not yet been discussed in detail.

In this paper, we realize the whole set of fundamental logic gates using two kinds of structures formed by metal slot waveguides. A single Y-shaped waveguide structure can work as AND, OR, NOT and XOR logic gates. By using two cascaded Y-shaped structure, with one port for inputting control beam, NAND, NOR and XNOR can be realized. The working principle is discussed in detail and the working efficiency is verified by simulation. The metal slot waveguide based logic gates show small size and intensity contrast as high as 16dB. These gates are good candidates for constructing future optical computing chips.

2. Logic gates with two input ports

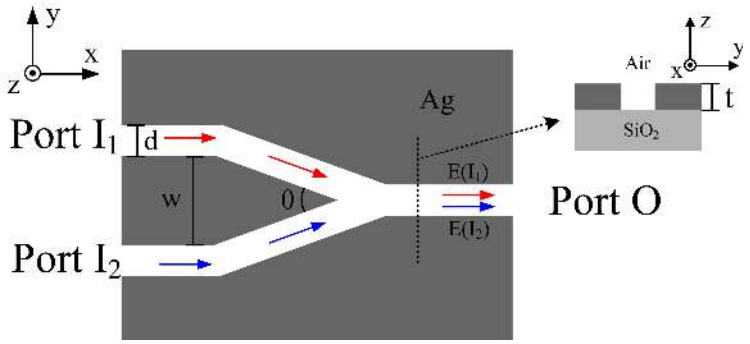

Fig. 1. Sketch of two input port logic gate based on slots in Ag film.

The proposed logic gates are composed by three metal slot waveguides with a Y-shape junction as shown in Fig. 1. The structure is fabricated in sliver film coated on SiO_2 substrate. In the device, the two ports denoted by I_1 and I_2 are taken as channels for input signals. The remainder port denoted by O is used as the fan-out of the logic gate. The input and output are all encoded by their intensities. Two signals are transmitted to the junction from the input ports and then reach the output port. The amplitudes of transmitted powers for the two signals

#184170 - $15.00 USD Received 24 Jan 2013; revised 13 Mar 2013; accepted 13 Mar 2013; published 10 Apr 2013

are $E(I_1)$ and $E(I_2)$.The constructive or destructive interference of $E(I_1)$ and $E(I_2)$, which is determined by the phases of the input signals, result in the output intensity I_o. By defining the value of the threshold intensity, the three port device can realize the logic operations of AND, OR, NOT and XOR gates.

Table 1. Illustration of the working principle of two input ports gates

Constructive			Destructive		
Input $\{E(I_1),E(I_2)\}$	Output amplitude	Output intensity	Input $\{E(I_1),E(I_2)\}$	Output amplitude	Output intensity
{0,0}	0	0	{0,0}	0	0
{E,0}	E	$\|E\|^2$	{E,0}	E	$\|E\|^2$
{0,E}	E	$\|E\|^2$	{0,-E}	-E	$\|E\|^2$
{E,E}	2E	$4\|E\|^2$	{E,-E}	0	0
OR ($I_t<\|E\|^2$) or AND ($\|E\|^2<I_t<4\|E\|^2$)			XOR ($I_t<\|E\|^2$) or NOT ($E(I_2)$ as control signal, $I_t<\|E\|^2$)		

The working principle for the logic operations is illustrated in Table 1. The input is expressed as $\{E(I_1),E(I_2)\}$, using the amplitudes of transmitted powers. The input power at ports I_1 and I_2 is selected to be equal. For the inputs, "on" and "off" states correspond to "1" and "0", respectively. For the output, the Boolean value is determined by the threshold intensity I_t. If the output intensity I_o is larger than the threshold I_t, the output value is "1". If $I_o<I_t$, the output is "0". For constructive interference, the complex amplitudes of the output for individual input $E(I_1)$ and $E(I_2)$ are set to be E. The output intensity I_o is $|E|^2$ for inputs {E,0} and {0,E}, and $4|E|^2$ for input {E,E}. When choosing I_t below $|E|^2$, the output state is "1" for input {E,0}, {0,E} and {E,E}, realizing OR logic function. When I_t is chosen above $|E|^2$ and below $4|E|^2$, the output is "1" only for {E,E} input, corresponding to the AND logic operations. For destructive interference, the complex amplitudes of the output for individual input $E(I_1)$ and $E(I_2)$ are E or –E, respectively. Because of the symmetry of gate structure, complete destructive interference can be realized at port O, resulting in a large interference visibility. The output intensity I_o is $|E|^2$ for inputs {E,0} and {0,-E}, and 0 for {E, -E}. Choosing I_t below $|E|^2$ results in an XOR gate. If the signal at port I_2 is used as control signal, for the input 0 and E at the I_1 port, i.e. {0,-E} and {E, -E}, the output state is just opposite to the input state, which leads to the function of NOT gate.

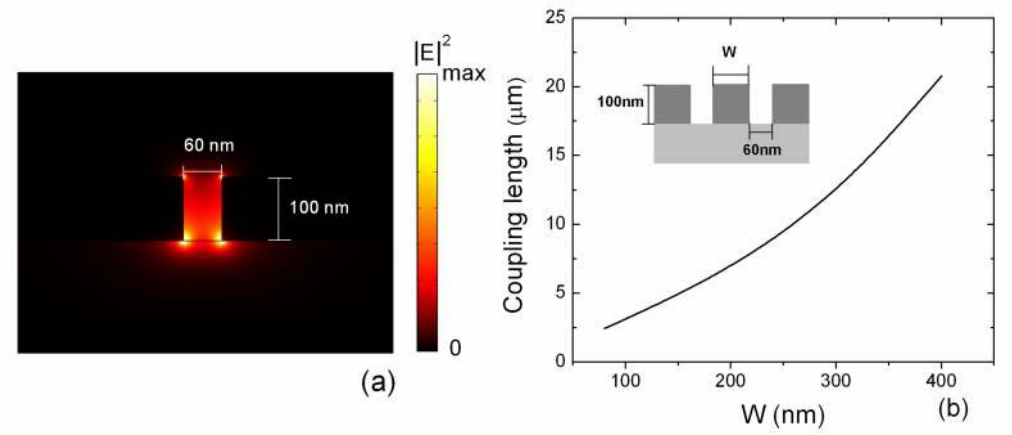

Fig. 2. (a) Distribution of field intensity $|E|^2$ of fundamental mode in the simulated metal slot waveguide. (b) Coupling length of two parallel slot waveguide as a function of separation w.

To verify the functions of the logic gate, simulations based on finite element method are performed. In simulation, we pay attention to the wavelength of 632.8 nm, with the corresponding permittivity of silver −18.36 + 0.48i, interpolated from experimental data [18]. The permittivity value of SiO_2 used here is 2.13. To obtain good confinement and acceptable

#184170 - $15.00 USD Received 24 Jan 2013; revised 13 Mar 2013; accepted 13 Mar 2013; published 10 Apr 2013

loss, the thickness t and width of waveguide d is set to be: t = 100nm and d = 60nm. The corresponding fundamental mode distribution is shown in Fig. 2(a). As can be seen the electric field is mainly confined in the slot. At the wavelength, the slot waveguide also have a considerable propagation length of 5.33μm. Here, the propagation length is defined as the length over which the power in the direction of propagation decays to 1/e of its original value due to material losses. In the gate structure, the input light propagating to the output port O will suffer strong loss at the junction. To decrease the energy loss at the junction, small angle between the two input waveguide θ is preferred. But too small θ will decrease the separation between the two input waveguide w, leading to the cross talk. To determine the appropriate value of the separation w, coupling length of two parallel slot waveguides for different separations is calculated, as shown in Fig. 2(b). Here the coupling length is defined as the propagating distance over which the power coupled from one waveguide to the other reaches the maximum. After overall consideration, θ is chosen to be 30°, and w is 300 nm. In the simulations, all the bends in the structures are used as sharp corners. In practical experiment, these corners have round shapes, which is beneficial for decreasing the bending loss.

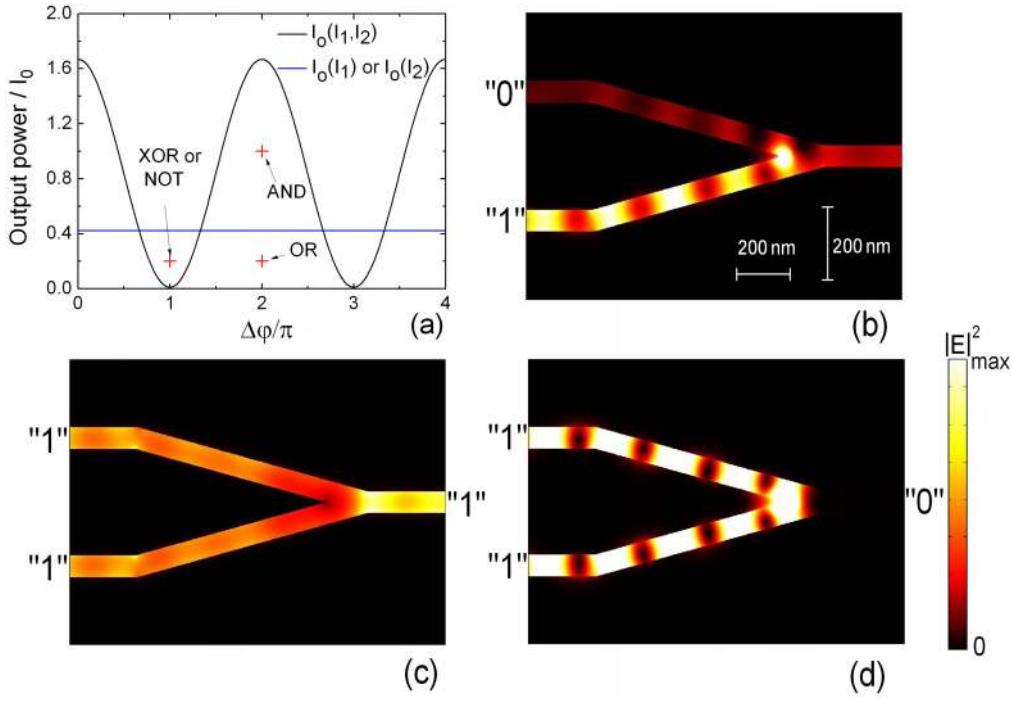

Fig. 3. Simulation results for the working performance of two input port logic gate. (a) The output power at port O as a function of phase difference between two input signals. The power of two input signals is both I_0. (b-d) Distribution of field intensity $|E|^2$ for individual inputs. (b) only one input at port 2; (c) two input signals with $\Delta\varphi = 2\pi$; (d) two input signals with $\Delta\varphi = \pi$.

In the simulation, the power of signals on both input port I_1 and I_2 is I_0, but the initial phase differences Δφ of the two signals is adjustable. The Fig. 3(a) shows the output power, $I_o(I_1,I_2)$, for different Δφ. $I_o(I_1,I_2)$ shows an ideal interference of the two input light signals, which is well described by cosine function. The complete interference can be attributed to the single mode characteristic of the waveguide and the symmetry of the gate structure. The output powers for individual input $I_o(I_1)$ and $I_o(I_2)$ are shown as the blue line. Our designed logic functions can be realized at different values of Δφ by defining corresponding threshold intensity. For $\Delta\varphi = \pi$ and threshold value of $0.2I_0$, XOR or NOT operations can be realized. For $\Delta\varphi = 2\pi$ and threshold value of $0.2I_0$, the device functions as an OR gate. If the threshold

#184170 - $15.00 USD Received 24 Jan 2013; revised 13 Mar 2013; accepted 13 Mar 2013; published 10 Apr 2013

is increased to I_0, the AND logic gate is realized. Figures 3(b)-3(d) show the field intensity distribution in the device for single input and both inputs with different Δφ. It is noteworthy that the intensity contrast for the output value "1" and "0" is high, for example, the intensity contrast is about 16dB for XOR, NOT and OR operations, and about 6dB for AND operations. It should also be noted that the choice of the threshold intensity and the phase difference can be quite flexible. For a given threshold intensity, these logic operations can be realized in a wide range of Δφ, which makes the devices have large tolerance.

3. Logic gates with three input ports

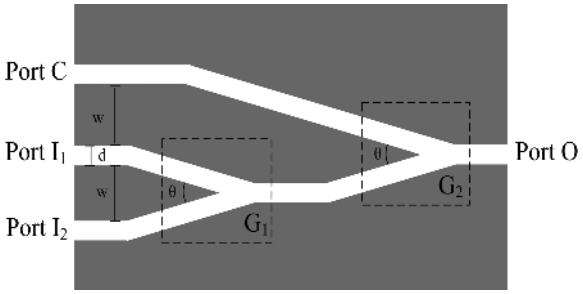

Fig. 4. Sketch of three input ports logic gate

For logic gates NOR, NAND and NXOR, the output is "1" when both input ports are empty, so additional input of the logic gate is needed to work as control signal. From another point of view, these logic functions are composite operations of the former functions, and their gates can be realized by cascading NOT gate and OR, AND, XOR, respectively [16]. The sketched structure of the logic gate with three input ports is shown in Fig. 4. In the structure, two input ports, I_1 and I_2, are connected to a Y-shape junction G_1, which can independently operate as a logic gate. The output of G_1 and another input port C are connected, forming a second independent gate, named G_2. The output port of G_2 is denoted as port O. In this design, the output of the first operation in G_1 is used as the input signal of G_2. Thus cascaded logic gates can be realized in such structure. The ports I_1 and I_2 are used for input signals, while the port C is used for control signal. Port O is the fan-out of the whole structure. All the parameters are denoted similar as in last section. The complex amplitude of light in port O transmitted from port C is denoted as E(C). For further extension of the device to realize more complex functions, the geometries of the basic gates, for instance G_1 and G_2, are exactly the same.

Table 2. Illustration of the working principle of the three input ports gates

Input {E(I1),E(I2)}	Control E(C)	Output amplitude	Output intensity	Control E(C)	Output amplitude	Output intensity
{0,0}	-E	-E	$\|E\|^2$	–2E	–2E	$4\|E\|^2$
{E,0}	-E	0	0	–2E	-E	$\|E\|^2$
{0,E}	-E	0	0	–2E	-E	$\|E\|^2$
{E,E}	-E	E	$\|E\|^2$	–2E	0	0
	XNOR ($I_t<\|E\|^2$)			NOR($\|E\|^2<I_t<4\|E\|^2$) or NAND($I_t<\|E\|^2$)		

The working principle of the gate is analyzed as shown in Table 2. For operations OR and AND, the two input signals from port I_1 and I_2 are in phase (Fig. 3(a) and Table 1). An out-phase control signal from port C can inverse the output of G_1. Here the second gate G_2 operates as a NOT gate. As shown in Table 2, when E(C) is twice as $E(I_1)$ and $E(I_2)$ ($E(I_1) = E(I_2) = E$), with a phase difference of π, NOR and NAND operations can be obtained. For a threshold value I_t above $|E|^2$ and below $4|E|^2$, the output correspond to NOR logic operation. For a threshold value I_t below $|E|^2$, the logic function of the whole structure is NAND. The

#184170 - $15.00 USD Received 24 Jan 2013; revised 13 Mar 2013; accepted 13 Mar 2013; published 10 Apr 2013

cascade approach for constructing NOR and NAND is not applicable for XNOR. For XOR operation, the output for input patterns {E,0} and {0,-E} are out phase. An additional control signal will lead to different output result for the two input patterns. However, the XNOR operation can still be realized in the structure with three input ports. Table 2 shows that, when $E(I_1) = E(I_2) = E$ and the control signal is out-phase with $E(C) = -E$, the outputs correspond to XNOR operation for a threshold value below $|E|^2$.

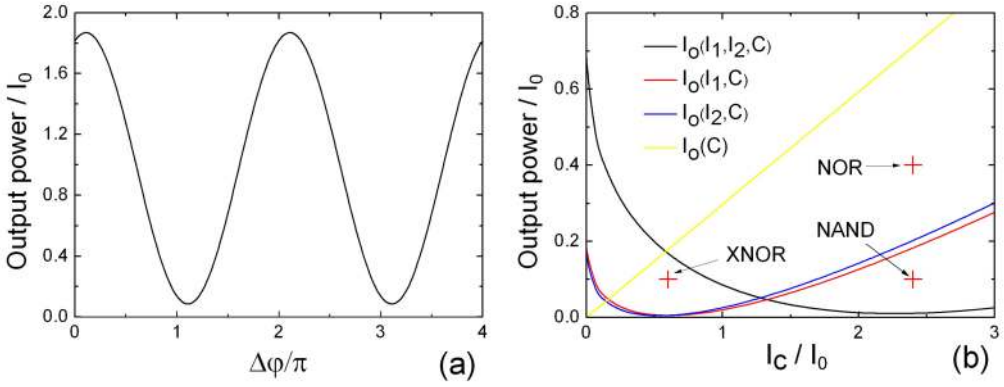

Fig. 5. (a) Output power for various phase difference between control beam and signals. (b) Output power for different input power of control beam. In (b), the red crosses correspond to working states for different operations.

Electromagnetic calculations were performed to quantitatively investigate the outputs of the device. For ports I_1 and I_2, their equal distance to port O produces no additional phase difference. So the two input signals are set to be with equal phase at the two ports. By setting the input power at port I_1, I_2 and C equal to I_0, the output intensity at port O is calculated for varying phase difference between the control signal and the input signals, as shown in Fig. 5(a). The minimum of the output power, corresponding to destructive interference at port O, occurs at $\Delta\varphi = 1.1\pi$, which is determined by the difference of the distances travelled by the control signal and the input signals. This phase difference is fixed for latter simulations. Figure 5(b) shows the variation of the output power at port O for different inputs when the power of control signal I_C is increased. The red crosses mark the corresponding area and power threshold for the three logic functions. As an example of the three logic functions, the distribution of field intensity for operating XNOR gate is shown in Fig. 6, with the power of control beam I_C to be $0.58I_0$. This XNOR logic gate shows a high intensity contrast of the output states "1" and "0" as about 16dB.

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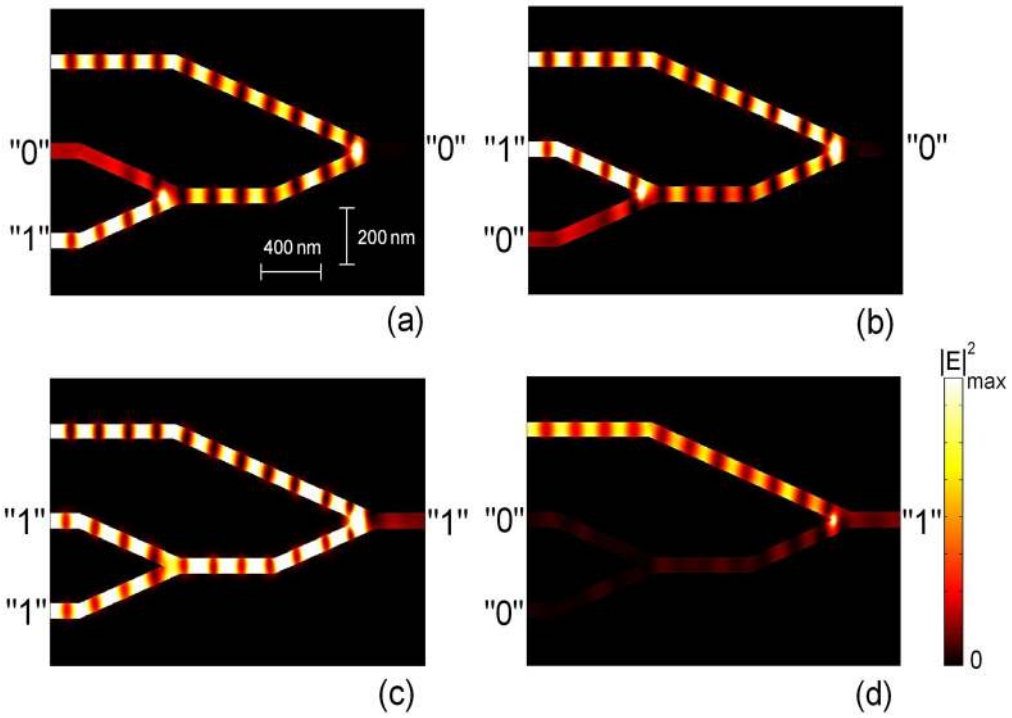

Fig. 6. Distribution of field intensity $|E|^2$ for XNOR logic operations. (a), (b), (c) and (d) correspond to different input patterns, and are in same color coordinate.

4. Conclusion

In this paper, we realize the whole set of fundamental logic operations in devices formed by metal slot waveguides. We show a single Y-shaped waveguide junction can work as AND, OR, NOT and XOR logic gates. By using two cascaded Y-shaped junction, with one port for control signal, NAND, NOR and XNOR gates can be realized. The working principle is discussed in detail and the working efficiency is verified by electromagnetic simulations. The metal slot waveguide based logic gates show small sizes and high intensity contrasts for the output states "1" and "0". Assembles of these gates can realize more complicated functions and construct future optical computing chip.

Acknowledgments

This work was supported by MOST Grants (No. 2009CB930700), NSFC Grants (Nos. 11004237, 11134013, 11227407) and "Knowledge Innovation Project" (KJCX2-EW-W04) of CAS.

#184170 - $15.00 USD Received 24 Jan 2013; revised 13 Mar 2013; accepted 13 Mar 2013; published 10 Apr 2013