Optical network on chip: design of wavelength routed optical ring architecture

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ABSTRACT

Network on chip (NoC) technology has now achieved a mature stage of development as a result of their use as a key component in many successful commercial devices. As multiprocessors continue to scale, these ship based electronic networks are more challenging to meet their power budget communication requirements. Innovative technology is emerging with the aim of offering shorter latencies and greater bandwidth with lower power consumption. Ring topology provides superior results among the all wavelength routed topologies in the chip optical network. In this paper, we proposed an optical ring network-on-chip (ORNoC) architecture which is contention free. Communication matrix is used to assign a single waveguide/wavelength pair to implement simultaneous communications. The design constraints for the proposed architecture will be wavelength reused on a single waveguide for multiple communications. We imply automatic wavelength/waveguide assignment for effective design and will prove that the proposed architecture can connect more number of nodes and less wavelengths per waveguide.

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1. INTRODUCTION

In digital electronic systems the first available chip containing single core with no memory, it has changed completely over the previous 40 years, now include dedicated hardware with dozens of cores. Ultra deep submicron technology which provides billions of transistors that allow hundreds of cores to be integrated onto a single chip. The performance of this core is decided by the interconnection and cores operating at high clock frequency and high bandwidth. Using traditional electrical interconnect for designing a system provides a major challenge because of propagation delay, interconnect noise, capacitive and inductive coupling. Due to increase in propagation delay, the performance of the system is reduced with low data rate and bandwidth is limited. Different interconnect architectures are developed to solve this problem. ie., using pipelined global interconnect and using repeaters on interconnect. Large number of pipelined registers are required in pipeline interconnect so delay and power consumption are increased because of additional registers and high operating frequency. Therefore, it is desirable to have a new on chip interconnecting technology that can rectify electrical interconnect issues.

When technology increases, processors and memories become quicker, smaller and more energy efficient, making it possible for computer architects to combine more of them into one chip. The moor's law reaches its limit; it replicates easy core to continue improving efficiency while minimizing production costs. Efficiency now confronts a limitation in chip element connectivity as well as computational power and memory access. Interconnection networks have appeared in this context to replace buses as the prevalent alternative for quick, cost effective and scalable communications. Both multi processors chips (which consist of dozens of identical cores) and heterogeneous system on chip is key to achieving future digital systems. Over the past decade, comprehensive study has been undertaken to optimize networks on chip from low level physical elements to system level problems.

In the next generation of multicore devices, increase in energy consumption and bandwidth scalability, optical networks on chip (ONoCs) which is gaining popularity has been used [1]. The use of ONoCs offers considerably enhanced bandwidth, reduced latency, increased immunity to electromagnetic noise and reduced power. Although some traditional network on chip (NoC) ideas are still suitable, the fundamental construction blocks and design difficulties for ONoCs are completely different. The implementation of an optical network requires several devices: waveguides, microring resonators, modulators and photodetectors. In wavelength division multiplexing (WDM) several wavelengths can travel simultaneously within a single waveguide, carrying several information streams. Microring resonators are located next to another waveguide it is in the form of ring. For converting the electrical signal into an optical signal modulator is used and for the reverse process, photo detectors were used. How much power the laser source has to pump into the waveguides to successfully transfer information can be calculated by adding losses along a specific path.

Defining new architectures using optical interconnect is a key challenge for designers today. New specific constraints are chosen for design methodologies in optical interconnect. The primary benefit of optical interconnection is its bit-rate transparent property [2]. This property promotes very high bandwidth transmission in optical networks. The energy wasted on a photonic connection is independent of the transmission range on a chip scale due to ultra low loss in optical waveguides. The message travels 2 mm or 2 cm apart, the energy dissipation is same between two cores [3]. In addition to that, for boosting the optical bandwidth of communication to a greater extent [4] several multiple optical signals, which is having different wavelengths can be transferred within the same waveguide without getting interfered with WDM.

In this paper, we propose a high throughput, low latency contention free optical ring network-onchip (ORNoC) novel architecture. The design constraint of this architecture is on a single waveguide a wavelength is reused for multiple communications. Therefore, limited waveguides are needed and the scalability is facilitated. The rest of the paper is organized as follows. Section 2 briefly presents related works. Section 3 introduces our proposed ONoC architecture. Section 4 discusses the performance evaluation. Conclusion and future work are presented in section 5.

The optical ring is the preferred option among all routed topologies of wavelength, providing low latency communication and decreased energy consumption. Grani and Bartolini [5] presented an extensive exploration of the design space for optical rings and demonstrated excellent results in power reduction and efficiency results over conventional electronic topologies. Their versatile implementation was a unique characteristic of optical rings, opening up possibilities for optimizing and customizing complex interconnection requirements. By adjusting the number of wavelengths and waveguides while maintaining the same connectivity requirements, the ring model can be tweaked to provide endless versions with extremely diverse power consumption values. Literature on the design space exploration and automation of optical rings is extremely poor to the best of our understanding. Beux et al. [6] suggest the first ring communication matrices algorithm. Their primary objective was to develop a design methodology, which can materialize ring models that fulfill the system's connectivity demands. A approach employing electrical links for information flow control and optical interconnections for data flow was proposed by Shacham et al. [7] to reserve the optical path, the electrical signal comes before the optical one. Therefore, optical communications can be delayed until an optical path is available, leading to a delay in contention. This type of network is therefore not a free of contention. References [8], [9] was proposed the similar observation for mesh ONoC and fat tree architecture. Electrical interconnections manage local communication while global communication is the responsibility of an optical communication proposed by Pasricha and Dutt [10]. Single write multiple read (SWMR) uses a single wavelength flow through the architecture and avoids the multiple communications through the same wavelength. The ONoC performance was affected severely by the abovementioned method. Our proposed ORNoC architecture does not experience from this inconvenient because we reuse wavelengths on the same waveguide at the same time for multiple communication.

The corona architecture follows an application of multi-write-single-read which involves arbitration to handle write conflict [11]. Reservation assisted SWMR bus is proposed in firefly architecture by Pan *et al.* [12], [13]. Compared to the SWMR method, extra latency is required and network throughput

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reduces quickly with token round trip latency. This is the drawback. This drawback is overcome by Flexishare architecture proposed by the same author, in which each cycle new token is injected. Koohi and Hessabi [14] proposed contention free optical NoC for on chip routing of optical packets but the complexity reduction technique is not considered. Assay for transposase-accessible chromatin (ATAC) processor [15] is similar to the proposed ORNoC architecture. The contention free property is based on wavelength reuse and WDM. One source multiple communication is not possible in ATAC except the same message is broadcast [16].

2. METHOD

Architecture of ONoC consists of three blocks [17], [18] as shown in Figure 1: i) transmitter, input from the generic NoC protocol converter is converted into optical signal in the transmitter. The main components in the transmitter are directly modulated laser source, driver circuit and demultiplexers; ii) wavelength router, router comprises of 2^{nd} order 2×2 micro resonator for routing the information between system on chip components; and iii) receiver, the receiver converts optical signal in to an electrical signal. It includes photodetector and trans-impedance amplifier. The development of ONoC is heterogeneous, consisting of active and passive optical components and integrated analog/digital circuits [19], [20]. The router has four input ports and four output ports called it as initiators (I) and targets (T) shown in Figure 2.



Figure 1. Architecture for optical NoC

Figure 2. Router architecture N×N(N=4)

Optical signal switching is taking place in any one of the output ports depends on the input wavelength. Different switching steps are bar state, cross state and cumulative state. The resonant wavelength is pumped into the filter and routed through the port in bar state. Cross state happens when injecting and dropping out non-resonant wavelengths into the filter. In cumulative state, the resonator routed or drops the resonant and non resonant wavelengths using WDM technique [21]–[25].

2.1. Ring based ONoC

The optical part integrates the ORNoC network whereas the electrical part consists of a number of computing devices connected via a NoC. Data transfer within the electrical layer/cluster nodes is called intra layer/intra cluster communications otherwise it is called as inter layer/cluster communications. The ORNoC is example for later case. This communication includes a three-stage routing, electrical, optical routing then electrical routing. The receiver communication begins when an optical network interface (ONI) receives a data and a destination identification (ID). The data is serialized and the current flowing through the micro resonator is then modulated with the suitable complementary metal–oxide–semiconductor (CMOS) driver circuit. The intensity of light emission is modulated according to the data bit values to achieve the electro optical transformation. The signal reaches the ORNoC, is rounded in it, and is lastly obtained through the ONI of a receiver. The photodetector initiates the opto-electronic transformation in the receiver ONI by converting a photon stream into a photocurrent. CMOS receiver circuit receives the analog signal which transforms the analog signal into a digital signal which is deserialized and transferred to the destination node.

Cyclic waveguides are used by ring-based ONoC to connect all the ONIs in a multi-cluster and assign various wavelengths for inter-cluster communiction. The ORNoC architecture and its design principle is illustrated in Figure 3, for interconnecting 8 clusters if cluster {A} to cluster {H}. ORNoC's physical design is easy to interconnect with two linear optical interconnections in different directions as shown in Figure 4. The utilisation of at least six wavelengths and the allocation of wavelengths in the optical

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interconnection in clockwise and counterclockwise directions are necessary for non-blocking communication between each pair in the ORNoC are illustrated in Figures 5 and 6 respectively.

Due to technological restrictions, there is a maximum number of wavelengths that can be multiplexed in WDM. Therefore, we may meet the technological constraints that restrict the number of wavelengths and waveguides by using several waveguides and various rotational directions to offer a sufficient number of communication channels. The contention free property of ORNoC is created possible by using various wavelengths, both in the context of WDM and reuse of wavelengths. The number of wavelengths is technologically restricted, which may limit the scalability of the architecture. ORNoC promotes the use of multiple rings to facilitate architecture on large scale. It is possible to reuse the same set of wavelengths for each ring because each ring is independent. The multi ring topology design allows lower power losses due to the lack of waveguide crossings.



Figure 3. Ring based ORNoC

В С D Е

1 3

_

4 _

1 2

_ _

_ _

А

_

_

А

В

С

D _

Е 5

F

G 3

Η 1 2 F

_

4

_

5

_

3 1

> 1 2 -_

_ 1 3 _ 2

_ _ 1

_ _ G Η

_ _

_

1



Figure 4. Logical interconnection of an ORNoC



Figure 5. Wavelength allocation and routing matrix for clockwise optical interconnect

	А	В	С	D	Е	F	G	Η
А	-	-	-	-	-4	-	-2	-1
В	-1	-	-	-	-	-5	-	-3
С	-2	-1	-	-	-	-	-	-
D	-	-3	-1	-	-	-	-	-
Е	-4	-	-2	-1	-	-	-	-
F	-	-5	-	-3	-1	-	-	-
G	-	-	-	-	-2	-1	-	-
Η	-	-	-	-	-	-3	-1	-



Figure 6. Wavelength allocation and routing matrix for anti clockwise optical interconnect

2.2. Optical ring matrices generation

To communicate with any number of components over an optical ring, we suggest an optimal approach. Multiple communications can be implemented using a wavelength, and the wavelengths can be assigned in both clockwise and counterclockwise directions on the same waveguide. Our goal is to minimize the number of wavelengths and waveguides required for contention free communications.

The proposed algorithm calculates the optical ring metrices and calculates the network power to communicate any number of components in the ring architecture. We do not place any restrictions on the architecture and the elements interact may be simple core, big cluster or other components. In addition, the communications to be implemented (connectivity matrix) can be introduced as an input, allowing the use of the algorithm for more complicated architectures.

The inputs to the algorithm are number of waveguides, wavelength and connectivity matrix. Waveguide matrix and wavelength matrix are the outputs. For a given number of waveguides with minimum wavelengths the algorithm generates the ring design based on place and route constraints.

The algorithm first attempts to create the connection between two nodes on the minimum path for each communication to be implemented in the ring and reuse the wavelength. If this is not possible because some of the necessary ring parts are not free in any waveguide with any of the wavelengths, a new wavelength is added to set the communication. The algorithm will try to set the communication on the non minimal path in the other direction around the ring, if maximum number of wavelengths is reached. If this cannot be achieved either, the algorithm must complete its execution and cannot generate the ring design with the given input.

The difference between exiting algorithm and proposed is that we set the number of wavelengths to be used and use them all in the same waveguide. This concept has the advantage that the technology gives the number of wavelengths that can be multiplexed in the same waveguide. The drawback of existing algorithm is it uses the minimal paths for several communications therefore propagation loss and number of crossings is increased. The proposed algorithm fixes the number of waveguides of the ring to overcome this issue and reuse the same wavelength then find the shortest path for communication. The algorithms input enables us to run it multiple times to get distinct communication matrices for a specified number of waveguides and reduces the number of wavelengths. The proposed algorithm can create architecture design first without limiting the number of wavelengths that will have only minimal routes and then try to reduce the maximum number of wavelengths, resulting in less power.

3. RESULTS AND DISCUSSION

3.1. Simulation tool

The object-oriented modular discrete event network simulation framework OMNeT⁺⁺ was used to develop a simulator for the subject under investigation. OMNeT⁺⁺ was chosen because it is open source and has a great API for creating scalable event-driven simulations. Although there are other simulators, only OMNeT⁺⁺ has a low entry barrier, is free for academic use, and can be used with high performance computing (HPC) clusters, which is critical for achieving high accuracy.

Optical routers are constructed in the simulator with the same parameter values. Each wavelength channel has a bandwidth of 10 Gbps for all optical devices, including E-O&O-E converters and routers. Because of the physical implementations in many-core processors, each packet has a fixed size of 64 bits, and a big data block can be transmitted in several packets. To evaluate router performance delay is calculated. The communication delay is defined as the time interval between source and destination for end-to-end packet transfer. Because of the high-speed optical transmission and non-blocking wavelength-based routing, any packet passing through the router has the same delay.

Figure 7 shows that the delay in ns with a variation in data rate. From the simulation it is observed that the proposed scheme has a lowest delay and large saturation data rate. When the average data rate is observed to be low, the packet delay in every ONoC scheme is very low, as most of the packets have not experienced queuing delays. Because of the rising contentions in electronic routers or gateways, the average end-to-end packet latency increases as the average data rate increases.

Figure 8 shows that the throughput versus rate of data. As, the throughput capacity is greater than the average rate of data, the average throughput of all these schemes increases linearly with the average data rate when the average data rate is low. The achieved average throughput cannot increase any further when the average rate of data exceeds the throughput capacity.



Figure 7. Delay vs data rate



Figure 8. Throughput vs data rate

3.2. Power analysis

From the laser source laser distribution network takes the power and distributes it to all nodes. We must use splitters for sending the same wavelengths simultaneously to several paths. The power needed for each node was determined from the insertion loss. To minimize the wastage of power, set the correct splitting ratio then only the necessary optical energy reaches each node. The proposed algorithm finds the minimal paths to avoid the power loss in the laser distribution network. As per the order of path length, it uses the same wavelength before assigning a new one. This reduces the power waste.

We have determined for each ring configuration, the number of wavelengths and waveguides along with the power it has absorbed and has recognized the several significant trade-offs which is shown in Figure 9. As predicted, more wavelengths and waveguides are needed to incorporate all communications while increasing the number of nodes to communicate. The power distribution network distributes the power

in long path communications and short path communications in clockwise direction shown in Table 1. Single waveguide consumes more power and needs a high wavelength. In comparison with the long and shorter path variants, we find that the algorithm can create the first configuration where only minimal paths exist. The shorter path has been observed as always better with longer paths, since it has less wavelengths and less power consumption.



Figure 9. Number of wavelengths required to execute all optical ring communications with different number of waveguides in systems with increasing number of nodes

Table 1. Power distribution									
Wayaguida	Long path co	mmunication	Short path communication						
waveguide	Wavelength	Power(mW)	Wavelength	Power(mW)					
3	35-28	175-178	39-25	175-178					
5	17-15	177-185	20-15	176-178					
7	13-11	183-185	13-11	183-182					
9	10	186-190	10	187-186					

4. CONCLUSION

The ORNoC architecture efficiency was evaluated and the automated design methodology was applied. Maximum number of wavelengths per waveguide with different node architecture was studied. We have presented a method for generating ring communication matrices for maximizing power efficiency with a minimum number of wave guides and wavelengths. The proposed algorithm can generate ring designs for any number of nodes with fewer wave guides and/or wavelengths. Using ORNoC architecture and design methodology, more number of processing elements can be connected. From the results it is absorbed that the proposed architecture was capable of connecting 64 nodes with 26 waveguides. Future study will involve power loss modelling and estimation for the ORNoC, as well as an investigation of the impact of optical interconnect defects on overall system reliability.

REFERENCES

- S. Werner, J. Navaridas, and M. Luján, "A survey on optical network-on-chip architectures," ACM Computing Surveys, vol. 50, no. 6, pp. 1–37, Nov. 2018, doi: 10.1145/3131346.
- [2] Rajiv Ramaswami, K. Sivarajan, and G. Sasaki, *Optical networks a practical perspective*, 3rd ed. Burlington: Morgan Kaufmann, 2012.
- [3] A. Shacham, K. Bergman, and L. P. Carloni, "On the design of a photonic network-on-chip," in *First International Symposium on Networks-on-Chip (NOCS'07)*, 2007, pp. 53–64, doi: 10.1109/NOCS.2007.35.

- [4] S. Xiao, M. H. Khan, H. Shen, and M. Qi, "Multiple-channel silicon micro-resonator based filters for WDM applications," *Optics Express*, vol. 15, no. 12, pp. 7489–7498, Jan. 2007, doi: 10.1364/OE.15.007489.
- [5] P. Grani and S. Bartolini, "Design options for optical ring interconnect in future client devices," ACM Journal on Emerging Technologies in Computing Systems, vol. 10, no. 4, pp. 1–25, May 2014, doi: 10.1145/2602155.
- [6] S. L. Beux, J. Trajkovic, I. O'Connor, G. Nicolescu, G. Bois, and P. Paulin, "Optical ring network on-chip (ORNoC): Architecture and design methodology," in 2011 Design, Automation & Test in Europe, 2011, pp. 1–6, doi: 10.1109/DATE.2011.5763134.
- [7] A. Shacham, K. Bergman, and L. P. Carloni, "Photonic networks-on-chip for generations of chip multiprocessors," *IEEE Transactions on Computers*, vol. 57, no. 9, pp. 1246–1260, Sep. 2008, doi: 10.1109/TC.2008.78.
- [8] H. Gu, J. Xu, and Z. Wang, "A novel optical mesh network on- chip for gigascale systems on chip," in APCCAS 2008 2008 IEEE Asia Pacific Conference on Circuits and Systems, 2008, pp. 1728–1731, doi: 10.1109/APCCAS.2008.4746373.
- H. Gu, J. Xu, and W. Zhang, "A low-power fat tree-based optical network-on-chip for multiprocessor system-on-chip," in 2009 Design, Automation & Test in Europe Conference & Exhibition, 2009, pp. 3–8, doi: 10.1109/DATE.2009.5090624.
- [10] S. Pasricha and N. Dutt, "ORB: An on-chip optical ring bus communication architecture for multi-processor systems-on-chip," in 2008 Asia and South Pacific Design Automation Conference, 2008, pp. 789–794, doi: 10.1109/ASPDAC.2008.4484059.
- [11] L. Zhu, K. Wang, D. Zhou, L. Liu, and H. Gu, "optimization algorithm to build low congestion multi-ring topology for optical network-on-chip," *IEICE Transactions on Information and Systems*, vol. E101.D, no. 7, pp. 1835–1842, Jul. 2018, doi: 10.1587/transinf.2017EDP7330.
- [12] Y. Pan, P. Kumar, J. Kim, G. Memik, Y. Zhang, and A. Choudhary, "Firefly: Illuminating future network-on-chip with nanophotonics," in *Proceedings of the 36th annual international symposium on Computer architecture - ISCA '09*, 2009, pp. 429– 440, doi: 10.1145/1555754.1555808.
- [13] Y. Pan, J. Kim, and G. Memik, "Flexishare: Channel sharing for an energy-efficient nanophotonic crossbar," in HPCA 16 2010 The Sixteenth International Symposium on High-Performance Computer Architecture, 2010, pp. 1–12, doi: 10.1109/HPCA.2010.5416626.
- [14] S. Koohi and S. Hessabi, "Scalable architecture for a contention-free optical network on-chip," *Journal of Parallel and Distributed Computing*, vol. 72, no. 11, pp. 1493–1506, Nov. 2012, doi: 10.1016/j.jpdc.2012.02.003.
- [15] J. Psota et al., "ATAC: Improving performance and programmability with on-chip optical networks," in Proceedings of 2010 IEEE International Symposium on Circuits and Systems, 2010, pp. 3325–3328, doi: 10.1109/ISCAS.2010.5537892.
- [16] R. Karimi, S. Koohi, M. Tinati, and S. Hessabi, "A thermally-resilient all-optical network-on-chip," *Microelectronics Reliability*, vol. 99, pp. 74–86, Aug. 2019, doi: 10.1016/j.microrel.2019.05.017.
- [17] A. Jedidi, "Crosstalk noise aware system for WDM-based optical network on chip," International Journal of Electronics and Telecommunications, vol. 65, no. 3, pp. 497–505, 2019, doi: 10.24425/ijet.2019.129805.
- [18] T.-M. Tseng, A. Truppel, M. Li, M. Nikdast, and U. Schlichtmann, "Wavelength-routed optical NoCs: design and EDA—state of the art and future directions," in 2019 IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2019, pp. 1–6, doi: 10.1109/ICCAD45719.2019.8942092.
- [19] M. R. Yahya, N. Wu, Z. A. Ali, and Y. Khizar, "Optical versus electrical: Performance evaluation of network on-chip topologies for UWASN many core processors," *Wireless Personal Communications*, vol. 116, no. 2, pp. 963–991, Jan. 2021, doi: 10.1007/s11277-019-06630-5.
- [20] X.-P. Yang *et al.*, "A novel algorithm for routing paths selection in mesh-based optical networks-on-chips," *Micromachines*, vol. 11, no. 11, pp. 1–14, Nov. 2020, doi: 10.3390/mi1110996.
- [21] H. Zhang *et al.*, "An optical neural chip for implementing complex-valued neural network," *Nature Communications*, vol. 12, no. 1, p. 457, Dec. 2021, doi: 10.1038/s41467-020-20719-7.
- [22] M. Balti and A. Jemai, "Performance survey of classic and optic network-on-chip," *IET Circuits, Devices & Systems*, vol. 15, no. 4, pp. 393–402, Jul. 2021, doi: 10.1049/cds2.12025.
- [23] M. Bahadori and K. Bergman, "Low-power optical interconnects based on resonant silicon photonic devices: Recent advances and challenges," in *Proceedings of the 2018 on Great Lakes Symposium on VLSI*, 2018, pp. 305–310, doi: 10.1145/3194554.3194606.
- [24] I. A. Young et al., "Optical I/O technology for tera-scale computing," IEEE Journal of Solid-State Circuits, vol. 45, no. 1, pp. 235–248, Jan. 2010, doi: 10.1109/JSSC.2009.2034444.
- [25] G. P. Agrawal, Fiber-optic communication systems, 2nd ed. Hoboken, NJ: John Wiley & Sons, 1997.

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