Optical Static RAM Cell

Nikos Pleros, Dimitrios Apostolopoulos, Dimitrios Petrantonakis, Christos Stamatiadis, and Hercules Avramopoulos

***Abstract*—We demonstrate an optical static random access memory cell that provides read and write functionality at 5 Gb/s. The circuit comprises a hybridly integrated semiconductor optical amplifier—Mach-Zehnder inteferometer (SOA-MZI) flip-flop serving as the memory unit and two additional SOA-based cross-gain modulation switches for controlling access to the memory cell.**

***Index Terms*—Integrated Mach-Zehnder inteferometer, optical flip-flop, optical memory, optical random access memory (RAM), optical signal processing, semiconductor optical amplifier (SOA).**

I. Introduction

DESPITE the proven high-speed capabilities of optical signal processing circuitry, photonic processing devices still experience several difficulties in being convincing about their functional potential. Although the recent progress in photonic integration technologies has revived expectations for enhancing functionality by deploying multiple optical elements on a single chip [1], [2], the absence of a reliable optical random access memory (RAM) remains the primal processing bottleneck that will continue to hard limit the functional capacity of photonic circuitry. Optical data processing processes are compelled either to be performed on-the-fly or to rely on optoelectronic conversion stages with subsequent electronic data storage when no high-speed optical buffering capabilities are available.

However, optical memory has to overcome innate limitations enforced by the neutral charge of light particles that impedes their storage and makes it impossible to mimic the respective electronic memory modules. As such, optical buffering has so far mainly relied on feedback/feedforward schemes using fiber-delay lines [3], or fiber-loop configurations [4] with limited functional potential. Optical bit-level storage has been only recently demonstrated by means of memory elements relying on coupled semiconductor lasers [5], [6] or coupled interferometric switches [7]. However, photonic storage with true random access characteristics has been presented so far only by parallelized electronic RAM configurations [8], [9], requiring optoelectronic conversion and demultiplexing of the incoming optical data into lower rate signals. An all-optical RAM design being capable of providing on-demand storage and retrieval of high-speed optical data has not been addressed so far.

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N. Pleros is with the Department of Informatics, Aristotle University of Thessaloniki, 54124 Thessaloniki, Greece (e-mail: npleros@csd.auth.gr).

D. Apostolopoulos, D. Petrantonakis, C. Stamatiadis, and H. Avramopoulos are with the School of Electrical and Computer Engineering, National Technical University of Athens, Zografou, GR 15773 Athens, Greece (e-mail: apostold@mail.ntua.gr; petranto@mail.ntua.gr@mail.ntua.gr; cstamat@mail.ntua.gr; hav@mail.ntua.gr).

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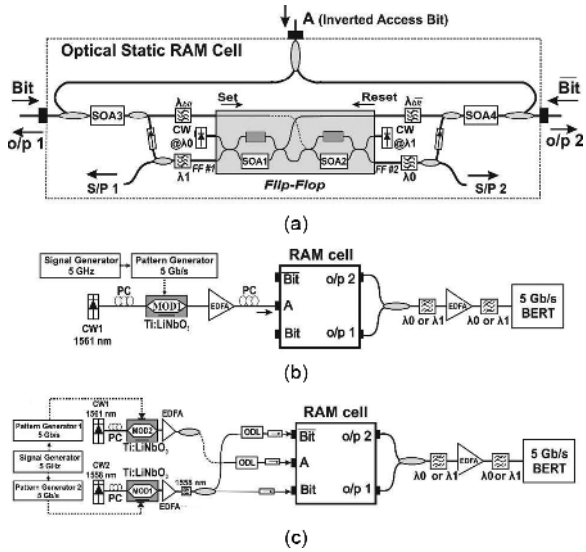

Fig. 1. (a) Experimental layout of the optical static RAM cell. (b) Read mode experimental setup. (c) Write mode experimental setup.

In this letter, we demonstrate what we believe to be the first all-optical static RAM cell with true random access read/write functionality. The proposed configuration comprises two semiconductor optical amplifiers (SOAs) and a hybridly integrated optical flip-flop that consists of two coupled semiconductor optical amplifier—Mach-Zehnder inteferometers (SOA-MZIs) [7]. The optical flip-flop serves as the single-bit memory element utilizing the wavelength dimension and the coupling mechanism between the two SOA-MZIs for determining the memory content, whereas the two SOAs operate as XGM switches controlling access to the flip-flop configuration. Error-free read and write functionality with true random access properties at 5 Gb/s are demonstrated directly in the optical domain.

II. Experimental Setup

Fig. 1(a) depicts the experimental configuration of the optical static RAM cell. It consists of two SOAs and an optical flip-flop that employs two coupled SOA-MZIs powered by two external continuous-wave (CW) input signals at $\lambda 0$ (1559 nm) and $\lambda 1$ (1556 nm). The flip-flop output signals emerge at FF#1 and FF#2 ports and the logical value of the memory cell is determined by the wavelength of the dominant CW signal [7]. The logical "1" state corresponds to $\lambda 0$ being the dominant flip-flop signal, whereas the logical "0" state is obtained when $\lambda 1$ dominates the optical flip-flop. Switching between the two memory states is achieved via an external optical pulse injected through the set or reset branches [7].

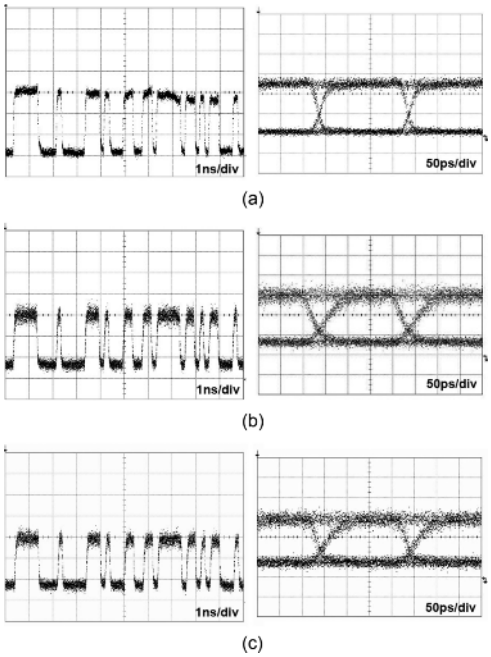

Fig. 2. Read mode operation pulse traces and eye diagrams: (a) inverted access bit, (b) read output at o/p2, and (c) read output at o/p1.

Random access operation of the RAM cell is provided by means of SOA3 and SOA4 that serve as XGM-based ON–OFF switches controlled by the inverted access bit. An inverted access bit of logical "1" value saturates both SOA3 and SOA4 blocking the transition of additional optical signals through these SOAs, prohibiting in this way communication between the memory cell and the outer world. To this end, neither read nor write functionality can be obtained and the RAM cell preserves its content. Access to the memory cell is enabled only when the inverted access bit becomes "0".

Read mode operation is accomplished when a "0" inverted access bit enters the cell and both Bit and $\overline{\text{Bit}}$ input signals equal zero. In that case, the $\lambda 0$ or $\lambda 1$ memory content propagates through SOA4 or SOA3 and emerges at o/p2 or o/p1 ports, respectively.

When the inverted access bit has a "0" logical value and write mode operation is targeted, the incoming Bit and $\overline{\text{Bit}}$ streams enter the RAM cell via SOA3 and SOA4, respectively, and are inserted into the flip-flop acting as the corresponding set and reset signals. In this way, a "1" value forces $\lambda 0$ to become the flip-flop dominant signal irrespective of the previous flip-flop state, whereas a "1" $\overline{\text{Bit}}$ value results to a flip-flop state dominated by $\lambda 1$. To this end, successful storage of the new incoming binary value into the RAM cell is achieved and the memory content and its inverted value are recorded at the State ports S/P2 and S/P1, respectively.

Fig. 1(b) shows the experimental setup used for the performance analysis of the RAM cell when operating in read mode. A CW signal at 1561 nm was launched into a Ti : LiNbO3 modulator (MOD1) driven by a pseudo-random bit sequence (PRBS) pattern generator, yielding a 5-Gb/s 2^9-1 nonreturn-to-zero (NRZ) data sequence at its output that was used as the inverted access bit signal into the RAM cell. Fig. 1(c) depicts the experimental setup used when write operation is intended. The inverted access bit signal was generated in a way similar to Fig. 1(b). For the Bit and $\overline{\text{Bit}}$ signal generation, a CW signal at 1558 nm entered an additional Ti : LiNbO3 modulator (MOD2) that was driven again by a 2^9-1 PRBS generator, to obtain a 5-Gb/s NRZ data signal with successive 500-bit long data parts of inverted logical values. This signal was then split into two fiber branches that induced a 500-bit differential delay between the two optical signal parts, and these two signals were injected as the Bit and $\overline{\text{Bit}}$ sequences into the RAM cell.

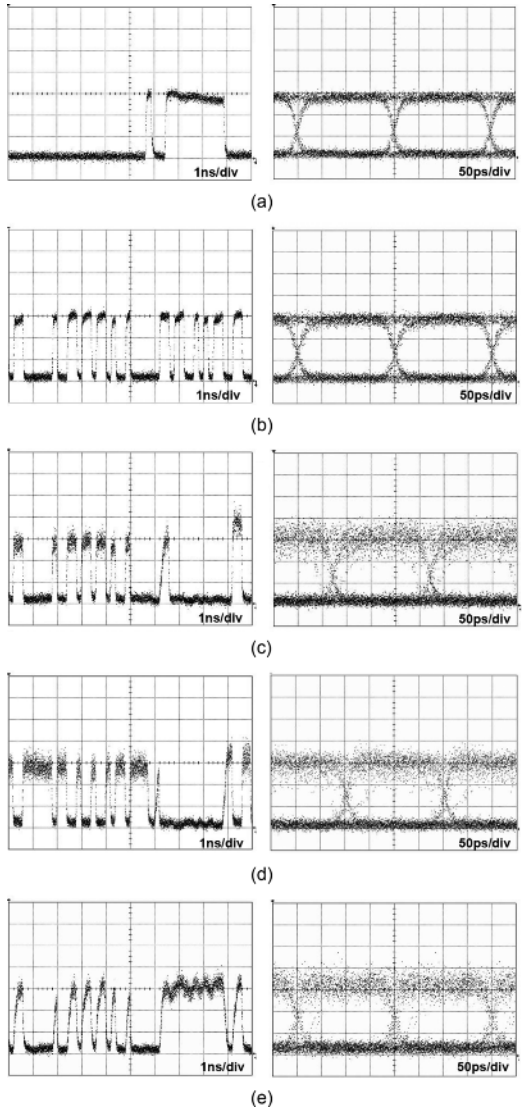

Fig. 3. Pulse trace and eye diagrams in write mode operation: (a) inverted access bit, (b) incoming bit, (c) set signal, (d) reset signal, and (e) RAM cell memory content recorded at S/P2 ($\lambda 0$).

III. Results and Discussion

Fig. 2 shows the experimental results obtained when the RAM cell operates in read mode at 5 Gb/s. Fig. 2(a) shows the pulse trace and the eye diagram of the inverted access bit entering the RAM cell, whereas Figs. 2(b) and 2(c) depict the respective read output signals obtained at o/p2 and o/p1 for the two different flip-flop states corresponding to $\lambda 0$ and $\lambda 1$ dominant wavelengths, respectively. Successful read operation in both flip-flop states can be confirmed by the complementary values of the corresponding read output signal and the inverted access bit stream.

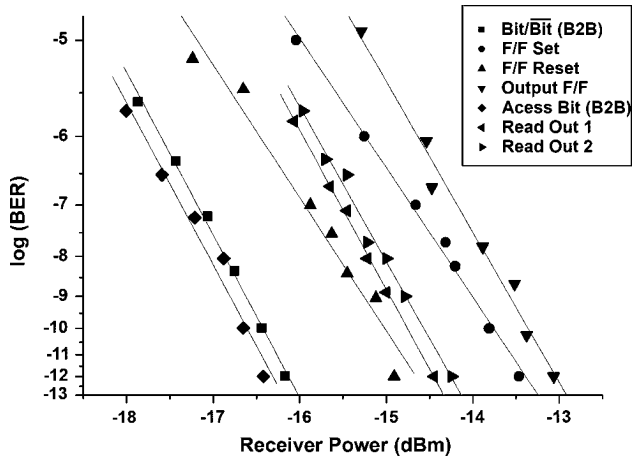

Fig. 4. BER measurements at 5 Gb/s for read and write mode operation.

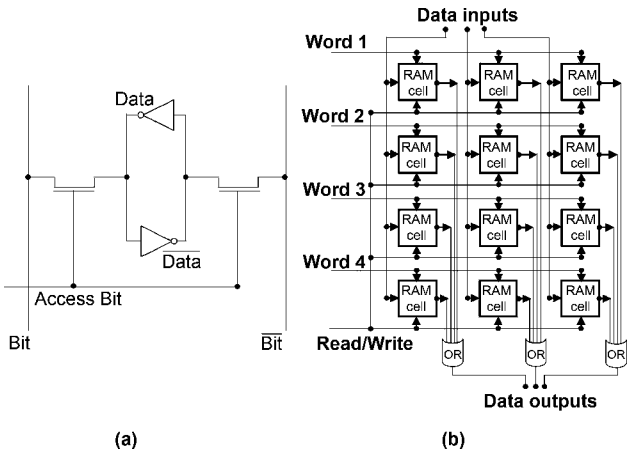

Fig. 5. (a) Electronic static RAM cell. (b) A 4 × 3-bit multicell RAM.

Write mode operation is verified by the pulse traces and eye diagrams shown in Fig. 3(a)–(e). Fig. 3(a) depicts the inverted access bit, whereas Fig. 3(b) illustrates the Bit sequence that enters the RAM cell. Fig. 3(c) and (d) shows the corresponding set and reset signals, respectively, as they are obtained at the output of SOA3 and SOA4, whereas Fig. 3(e) illustrates the corresponding RAM memory content as it is imprinted at $\lambda 0$ and recorded at the S/P2 port. Whenever a "0" inverted access bit enters the RAM cell, the set and reset signals are identical to the incoming Bit and $\overline{\text{Bit}}$ streams since the latter pass unaffected through SOA3 and SOA4, respectively. In this case, the $\lambda 0$ memory content follows the pattern of the set signal leading to successful storage of the respective incoming Bit sequence, as shown by Fig. 3(e). When the inverted access bit value becomes a logical "1", then both SOA3 and SOA4 operate in their OFF-switching state blocking the incoming Bit and $\overline{\text{Bit}}$ pulses. As such, both the set and reset signals equal zero irrespective of the incoming Bit and $\overline{\text{Bit}}$ streams and the memory content remains unaltered retaining its last value.

Fig. 4 shows the bit-error rate (BER) curves obtained at every stage of the optical static RAM cell at 5 Gb/s. Error-free operation was obtained for both read and write functionalities with a power penalty of less than 2 and 3 dB, respectively. Operating conditions for the optical flip-flop were 1 and 5.5 dBm average optical power for the two CW signals and 6.5 and 8.8 dBm peak power for the set and reset signals, respectively.

The proposed optical RAM cell can be utilized for asynchronous and variable-length data packet processing functionalities, enhancing packet-format transparent operation of one-bit optical flip-flops [10]. Its architectural analogy to the respective electronic static RAM cell [9] depicted in Fig. 5(a) could, in principle, also enable the implementation of multicell optical RAM devices, by exploiting multi-element SOA integration techniques [1] or alternatively silicon-based switching structures instead of SOAs for increased integration densities [2]. Fig. 5(b) illustrates a 4 × 3 multicell RAM layout comprising 12 independently controlled memory cells in a 2-D array structure, with each row storing a 3-bit word. A read/write input signal dictates the operational mode, while access to the RAM cells of a single row is allowed only when the respective "word" input has a "1" logical value. The realization of an optical RAM bank even with small buffering capacity could presumably open totally new perspectives in the field of optical header processing in all-optical label switched networks and in optical high-speed computer interconnects.

IV. Conclusion

We have presented an all-optical static RAM cell providing error-free read/write functionality with true random access characteristics at 5 Gb/s. The proposed design employs two SOAs and a hybridly integrated SOA-MZI optical flip-flop.

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