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*Total number of authors:*  
24

*Published in:*  
Proceedings of SPIE

*Link to article, DOI:*  
[10.1117/12.2290258](https://doi.org/10.1117/12.2290258)

*Publication date:*  
2018

*Document Version*  
Publisher's PDF, also known as Version of record

[Link back to DTU Orbit](#)

### *Citation (APA):*

Katopodis, V., Tsokos, C., De Felipe, D., Spyropoulou, M., Konczykowska, A., Aimone, A., Groumas, P., Dupuy, J. Y., Jorge, F., Mardoyan, H., Rios-Müller, R., Renaudier, J., Jennevé, P., Boitier, F., Pagano, A., Quagliotti, M., Roccatto, D., Johansen, T. K., Tienforti, M., ... Kouloumentas, C. (2018). Optical terabit transmitter and receiver based on passive polymer and InP technology for high-speed optical connectivity between datacenters. In *Proceedings of SPIE* (Vol. 10561). [1056107] SPIE - International Society for Optical Engineering. Proceedings of SPIE, the International Society for Optical Engineering Vol. 10561 <https://doi.org/10.1117/12.2290258>

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**SPIE.**

Event: SPIE OPTO, 2018, San Francisco, California, United States

# Optical Terabit Transmitter and Receiver Based on Passive Polymer and InP Technology for High-Speed Optical Connectivity Between Datacenters

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## ABSTRACT

We demonstrate the hybrid integration of a multi-format tunable transmitter and a coherent optical receiver based on optical polymers and InP electronics and photonics for next generation metro and core optical networks. The transmitter comprises an array of two InP Mach-Zehnder modulators (MZMs) with 42 GHz bandwidth and two passive PolyBoards at the back- and front-end of the device. The back-end PolyBoard integrates an InP gain chip, a Bragg grating and a phase section on the polymer substrate capable of 22 nm wavelength tunability inside the C-band and optical waveguides that guide the light to the inputs of the two InP MZMs. The front-end PolyBoard provides the optical waveguides for combing the In-phase and Quadrature-phase modulated signals via an integrated thermo-optic phase shifter for applying the  $\pi/2$  phase-shift at the lower arm and a 3-dB optical coupler at the output. Two InP-double heterojunction bipolar transistor (InP-DHBT) 3-bit power digital-to-analog converters (DACs) are hybridly integrated at either side of the MZM array chip in order to drive the IQ transmitter with QPSK, 16-QAM and 64-QAM encoded signals. The coherent receiver is based on the other side on a PolyBoard, which integrates an InP gain chip and a monolithic Bragg grating for the formation of the local oscillator laser, and a monolithic 90° optical hybrid. This PolyBoard is further integrated with a 4-fold InP photodiode array chip with more than 80 GHz bandwidth and two high-speed InP-DHBT transimpedance amplifiers (TIAs) with automatic gain control. The transmitter and the receiver have been experimentally evaluated at 25Gbaud over 100 km for mQAM modulation showing bit-error-rate (BER) performance below FEC limit.

**Keywords:** photonic integration, multi-format transmitter, passive polymer technology, InP Mach-Zehnder modulators, InP-DHBT electronics, InP Photodiodes, coherent optical receiver

## 1. INTRODUCTION

The global annual IP traffic is expected to overcome the barrier of 20% compound annual growth rate (CAGR) before 2020 [1] driven by the explosive growth of the cloud computing and Internet of Things (IoT) applications. This tremendous evolution of the internet applications demands even more bandwidth from intra- and inter-datacenter (DC) networks. To fulfil this goal, high bandwidth, energy efficient and low cost optical transceivers operating at 100 Gb/s or beyond are needed. For intra-DC connectivity, short-reach optical interconnects over distances up to 2 km and with bit rates up to 100 Gb/s are based on direct detection schemes with either non-return-to-zero on-off keying (NRZ-OOK) or higher-order modulation formats [2-3]. The first class comprises both multi-lane solutions with 10 or 25 Gb/s per lane, and single-lane solutions operating directly at 100 Gb/s [4-5]. Scaling the latter solution to a dual-lane solution, a 200 Gb/s transmitter has been also demonstrated [6]. The second class comprises on the other hand transmitters with

different types of modulation elements and modulation formats, like for example pulse amplitude modulation-4 (PAM-4) [7]-[9], PAM-8 [10]-[12], or discrete multi-tone (DMT) modulation [13]-[14].

Regarding inter-datacenter (DC) systems, current 100 Gb/s optical interfaces seem to be already outdated. These interfaces are based on coherent optical systems using dual-polarization (DP) Quadrature Phase Shift Keying (QPSK) modulation and operating at 28/32 Gbaud [15]. Efforts to extend the capacity to 200 Gb/s are based on the use of dual polarization in combination with Quadrature Amplitude Modulation (QAM), and 16-QAM in specific. Further extension to higher capacities (400 Gb/s and 1 Tb/s) [16] require higher symbol rates, higher order mQAM constellations, and/or additional number of optical subcarriers, leading to the next generation of scalable products and networks.

In order to cope with the new capacity demands in a flexible, energy efficient and low-cost fashion, 400 Gb/s and 1 Tb/s links for inter-datacenter connectivity should be based on Photonic Integration Circuit (PIC) technology [17]-[19]. Optical multi-format [20], multi-carrier [21]-[22] and multi-flow [23] transmitters have been already demonstrated on various photonic platforms such as silicon [24]-[25] and InP [26]-[27] based on monolithic integration. Moreover, co-packaging of optical transmitters with high speed electrical integrated circuits (ICs), such as digital-to-analog converters (DACs) or drivers relying on complementary metal-oxide semiconductor (CMOS) [28]-[30] or InP [31]-[32] technology, has been demonstrated in order to enhance performance, compactness and flexibility, facilitating various types of mQAM modulation in either single-polarization (SP) or dual polarization (DP) operation.

Segmented transmitters are examples of this category, usually relying on hybrid integration of the optical MZM chip with dedicated drivers on CMOS technology to generate mQAM ( $m=4, 16, 64$ ) modulation formats. More specifically, segmented MZM designs were reported on the silicon platform [24] and recently on the InP platform [30] for NRZ signals. Higher order modulation formats generated by segmented modulators were also reported such as PAM-4 in [33]-[34] and 64-QAM in [35]-[37]. On the other hand, a multi-flow transmitter implementation based on passive polymer platform (PolyBoard) allowing for optical carrier management and polarization handling of up to two optical flows on a single chip in combination with bulk IQ modulators and high-speed electrical drivers has been proposed in [23] revealing high data throughput with 28 Gbaud QPSK signals and flexibility in terms of scalability to larger numbers of supported flows, multi-format and multi-rate schemes and polarization multiplexing. For multi-carrier integrated transmitters, the generation of flexible optical superchannels offer the potential to add and remove bandwidth via the adjustment of the number of optically modulated carriers [22] and the variable selection of baud rate and modulation format [21]. Regarding the detection side, SP or DP coherent receiver PIC designs were reported on silicon [38] and InP platform [39], while co-packaged receivers with high speed BiCMOS electronics responsible for the amplification stage were demonstrated in [40]-[41] for 28 Gbaud QPSK and 16QAM signals.

In this work, we introduce a packaged multi-format SP-IQ transmitter with wavelength tunability and a coherent receiver that both rely on the hybrid integration of two different photonic platforms (PolyBoard and InP) with high speed InP electronics with operation potential up to 64 Gbaud. While the wavelength tunability in the C-band can provide network flexibility in terms of wavelength allocation of different signals in the network, the flexibility in the generation of the driving signals (in terms of baud rate and number of levels) can enable additional flexibility in the tradeoff between transmission reach and total throughput up to 384 Gb/s per single lane for high-speed connectivity between DCs. The optical subassembly of the transmitter consists of two PolyBoards and an InP chip with high-speed MZM array, featuring 3-dB bandwidth in excess of 42 GHz and  $V_{\pi}$  below 2Vpp. The three chips are combined using the butt-coupling technique. The first (back-end) PolyBoard comprises an external cavity laser with an InP gain chip as the active medium and a Bragg Grating (BG) on the PolyBoard as the semi-transparent mirror, which provides tunable light emission over 23 nm inside the C-band. The second (front-end) PolyBoard receives the modulated I and Q products at the outputs of the two InP MZMs and combines them into a single QAM signal after a 90° optical phase shifter in the lower part and a Y-junction. The InP MZMs are driven by two 3-bit-selector-power-digital-to-analog-converters (3b-SPDACs) based on the InP-double heterojunction bipolar transistor (InP-DHBT) technology, which can generate up to PAM-8 electrical signals after multiplexing, digital-to-analog conversion and amplification stages, and thus can result in the generation of QAM signals at the output of the IQ modulator up to 64-QAM. The SP coherent receiver on the other hand is based on the same mixture of photonic and electronic technologies and the same integration techniques, using a PolyBoard for the accommodation of the tunable local oscillator, the necessary optical attenuators and the 90° optical hybrid, an InP chip with a quad photodiode (PD) array with 3-dB bandwidth higher than 90 GHz, and an InP-DHBT electronic chip with two ultra-fast transimpedance amplifiers (TIAs) with potential for operation at rates up to 64 Gbaud.

In the remainder of the present manuscript, we present in detail the system design of the SP-transmitter and the coherent receiver, and the integration and packaging concept for both devices. We also present the experimental results from the

static characterization of the transmitter and from its system testing at 25 Gbaud. The latter includes transmission of QPSK and 16-QAM signals over 100 km in lab settings, and transmission of QPSK signals over 232 km over installed fiber in the network of Telecom Italia in Torino. Bit error rate (BER) below the Forward-Error Correction (FEC) limit with 7% overhead was achieved in all cases. Results from the experimental testing of the receiver are not presented, since relevant efforts are ongoing.

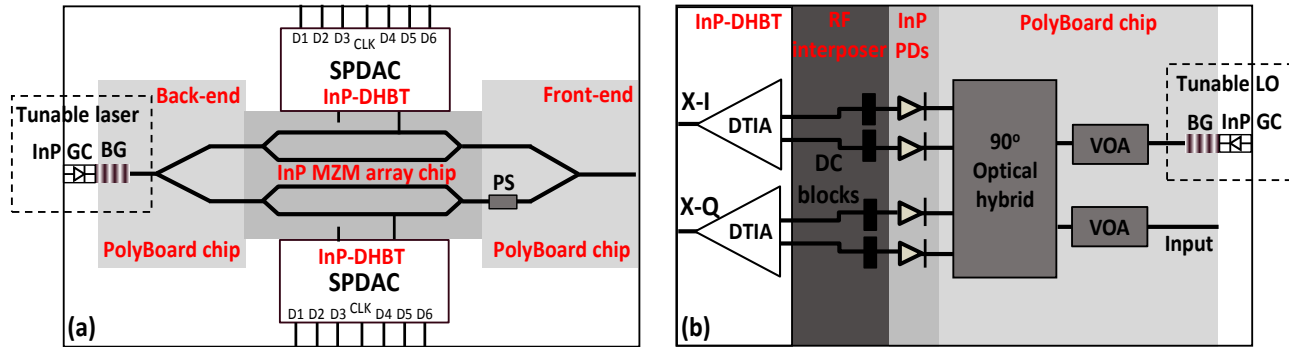


Figure 1. Layout of: (a) the 64 Gbaud SP-IQ tunable transmitter based on the hybrid integration of a PolyBoard-InP-PolyBoard chip and (b) the 64 Gbaud SP coherent receiver relying on the hybrid integration of PolyBoard with InP photodiodes and InP-DHBT electronics. The LO of the coherent receiver is based again on an external cavity laser that spans across the InP GC and the PolyBoard. Tunability is provided by the tunable BG on the PolyBoard.

## 2. DESIGN AND INTEGRATION CONCEPT OF MULTI-FORMAT SP-IQ TUNABLE TRANSMITTER

Figure 1(a) illustrates the schematic of our multi-format SP-IQ tunable transmitter with potential for modulation of  $m$ -QAM ( $m=4, 16, 64$ ) signals at rates up to 64 Gbaud. Its optical part is based for the first time on the combination of two PolyBoards with an InP chip between them, which comprises two Mach-Zehnder modulators (MZMs). PolyBoard is a single-mode photonic integration platform based on optical polymers. It has a proven potential for operation as a low-cost and multi-functional photonic integration platform, since it is characterized by low propagation loss (0.5 dB/cm at 1550 nm), large variety of monolithically integrated structures and possibility for hybrid integration of InP components like gain chips (GCs) and photodiodes (PDs) in a fast and easy way [42]. Although efforts for the development of fast modulators are ongoing based on the heterogeneous integration of graphene sheets inside the structure of its polymer waveguides [43], the possibility for high-speed modulation can be addressed via the hybrid integration of InP chips with either electro-absorption or Mach-Zehnder modulators (EAMs or MZMs, respectively).

### 2.1 Optical design and optical integration of multi-format SP-IQ tunable transmitter

As illustrated in Figure 1(a), the first PolyBoard (back-end PolyBoard) is responsible for the hybrid integration of the tunable laser and the driving of the generated light into the two MZMs of the IQ modulator on the InP chip. The tunable laser is an external cavity laser based on the hybrid integration of an InP gain chip to the PolyBoard via butt-end coupling, and the monolithic integration of a Bragg-Grating on the PolyBoard. The Bragg Grating can be thermally tuned over a range of 23 nm inside the C-band, and can act as the semi-transparent mirror of the cavity of the tunable laser [42]. Figure 2(a) presents indicative experimental data from the testing of the tunable laser, revealing that the tuning of the Bragg-grating results in the same range (23 nm) of emission wavelength tunability. Throughout this range, the operation of the tunable laser is very stable with side-mode suppression ratio (SMSR) higher than 40 dB and homogeneous in terms of output power. After its generation, the light is split into two parts by a Y-junction and is directed to the inputs of the two MZMs on the InP chip for the modulation of the I and Q components of the optical signal. The total power that enters the InP chip is 5.4 dBm. Each MZM is single-driven, has a  $V_{\pi}$  of 2 V and a bandwidth of 42 GHz, as illustrated in Figure 3(b). This bandwidth performance can facilitate high speed IQ modulation at 56 or even 64 Gbaud, provided that high-speed electronic circuits and packaging methods are also used. At the maximum transmission point of each MZM, the InP features an insertion loss of 1 dB. Finally, the front-end PolyBoard comprises a Y-junction with a 90° phase shifter on the lower arm, and is responsible for the combination and orthogonality between the I and Q modulation components. A picture of the optical subassembly of the transmitter with the main dimensions of the chips is illustrated on Figure 3.

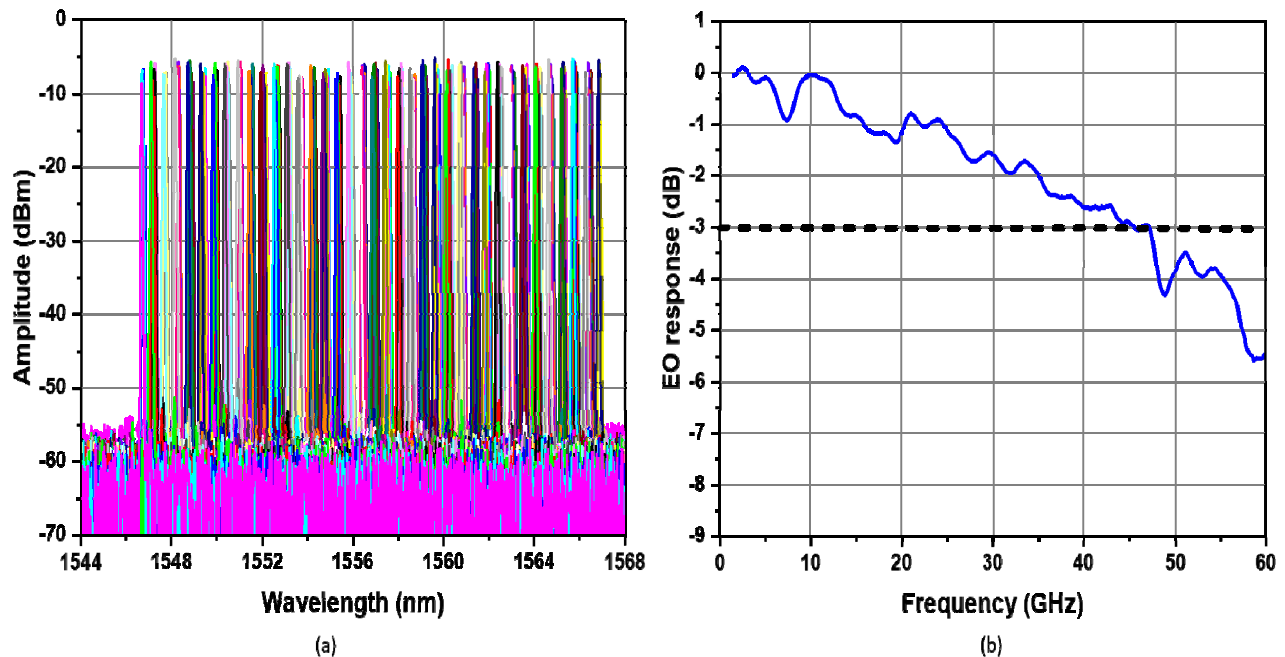


Figure 2. (a) 23 nm of laser tunability over 1541-1564 nm range revealing high-quality emission with SMSR higher than 40 dB and (b) 3-dB EO frequency of InP-MZM in excess of 42 GHz.

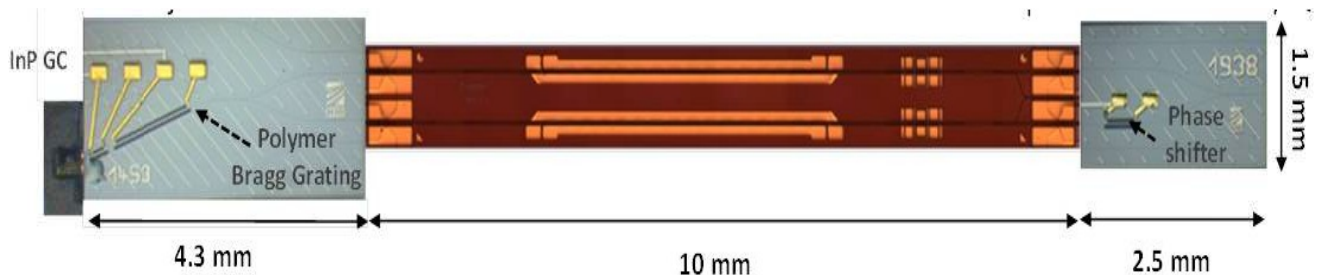


Figure 3. Picture of the optical subassembly of the tunable SP-IQ transmitter comprising the back-end PolyBoard with the tunable laser, the InP chip with the two parallel MZMs and the front-end PolyBoard with the 90° phase shifter.

The integration of the 3 photonic integration circuits and the preparation of the optical subassembly of the transmitter illustrated in Figure 3, was based on the butt-end-coupling technique. In order to optimize the coupling between the PolyBoard and the InP chip in either case and compensate for the imperfections and coupling losses that would be present due to the different mode-field profiles in the two platforms, a coupling optimization process was carried out relating to the waveguide facet width of the PolyBoards. Due to the mode mismatch between the InP chip and the PolyBoards, the facet of the polymer waveguides were laterally tapered in order to eliminate this mismatch. In Figure 4 (c), the simulated coupling losses between the InP MZM waveguide and the PolyBoard waveguide as a function of the final width of the PolyBoard waveguide are presented. As shown, a minimal coupling loss of 0.6 dB can be obtained for a polymer waveguide width of 3  $\mu\text{m}$ . Figure 2(d), depicts in turn, the alignment tolerance between the two chips by means of an alignment offset in either axis. As illustrated, the additional misalignment loss is kept lower than 1 dB if the misalignment is lower than  $\pm 0.8 \mu\text{m}$  in either axis. During the assembly process, experimental tests showed that the actual coupling loss between each PolyBoard and the InP chip was only 0.8 dB, in very good agreement with the simulation results.



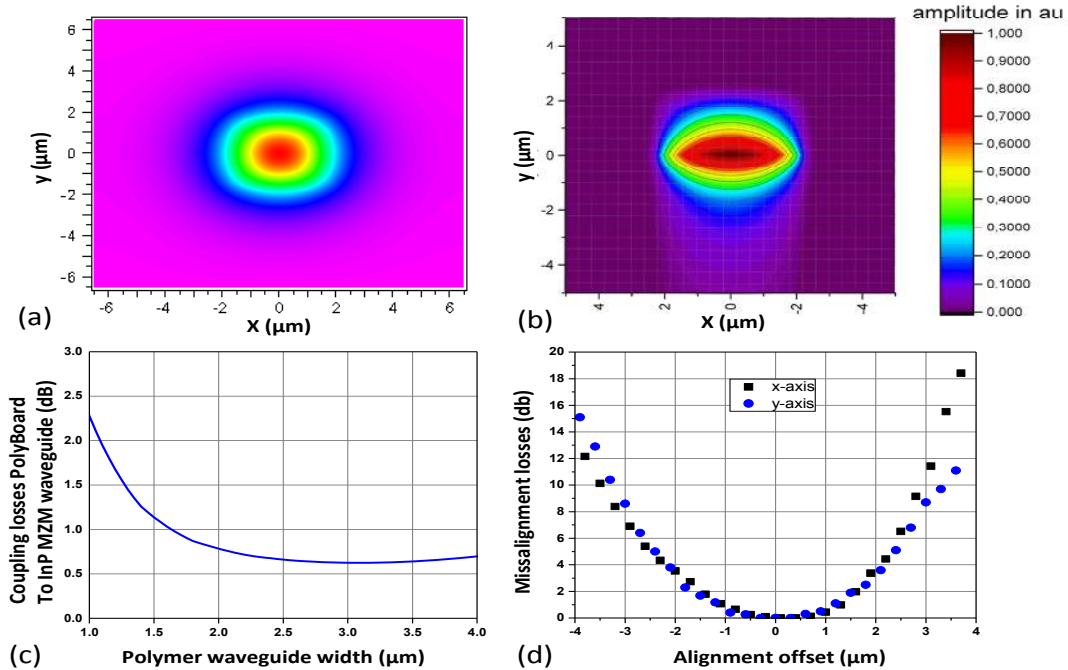


Figure 4. Simulated mode field distribution of: (a) PolyBoard waveguide, and (b) InP MZM waveguide for TE mode, (c) simulated mode-overlap coupling losses of PolyBoard to the InP waveguide for different PolyBoard waveguide widths ( $W_T$ ), and (d) optical losses for alignment offset between the two waveguides in the horizontal and vertical axis (with respect to the optimum  $W_T$  value).

## 2.2 Electrical design and packaging of multi-format SP-IQ tunable transmitter

The electrical part of the transmitter is based on the use of two electrical circuits built on the InP-double heterojunction bipolar transistor (InP-DHBT) technology [44]. Both circuits are 3-bit-selector-power-digital-to-analog-converters (3b-SPDACs) and integrate in a single chip the elements that are needed for the accommodation of the multiplexing, digital-to-analog conversion and amplification functionalities. Each SPDAC receives as input six electrical data signals (D1, D2, D3, D4, D5, D6) and a clock signal (Clk) at half the final rate, and provides after 2:1 time division multiplexing, digital-to-analog conversion and amplification, a driving electrical signal with up to 8 levels that drives each MZM on the InP chip. Since each SPDAC has two output ports providing complementary outputs, the operation of the modulators can be realized in single-ended or differential mode. In our case, the operation of the InP MZMs is single-ended, since the second port is unused and 50 Ohm terminated. Figure 5(a) illustrates a micro-photograph of the SPDAC with footprint  $1.8 \text{ mm} \times 3 \text{ mm}$ . On the left side of the photograph we have the six single-ended input ports for the input data

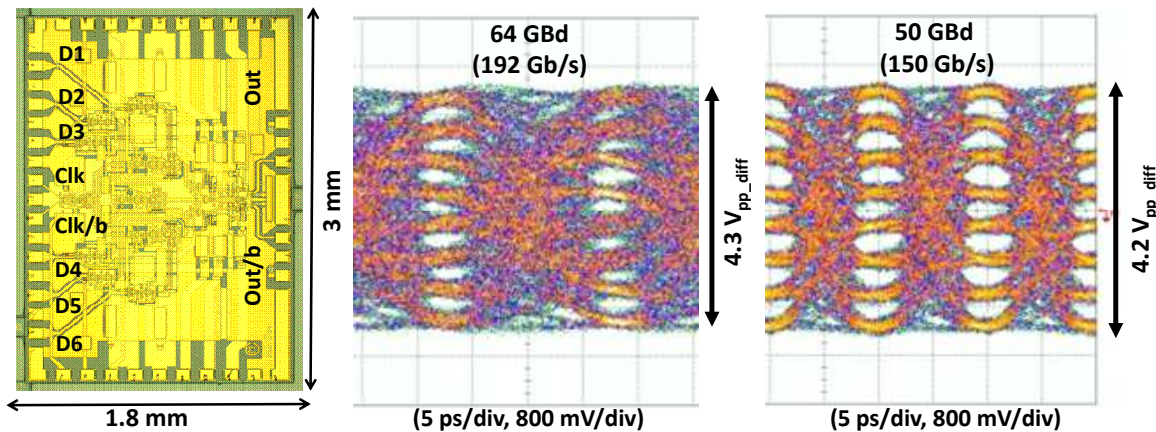


Figure 5. (a) Microphotograph of SPDAC chip with eight input data streams and two complementary output ports. (b) and (c) Electrical eye-diagrams of differential output signal with 8-levels (PAM-8) at 64 Gbaud and 50 Gbaud, respectively.

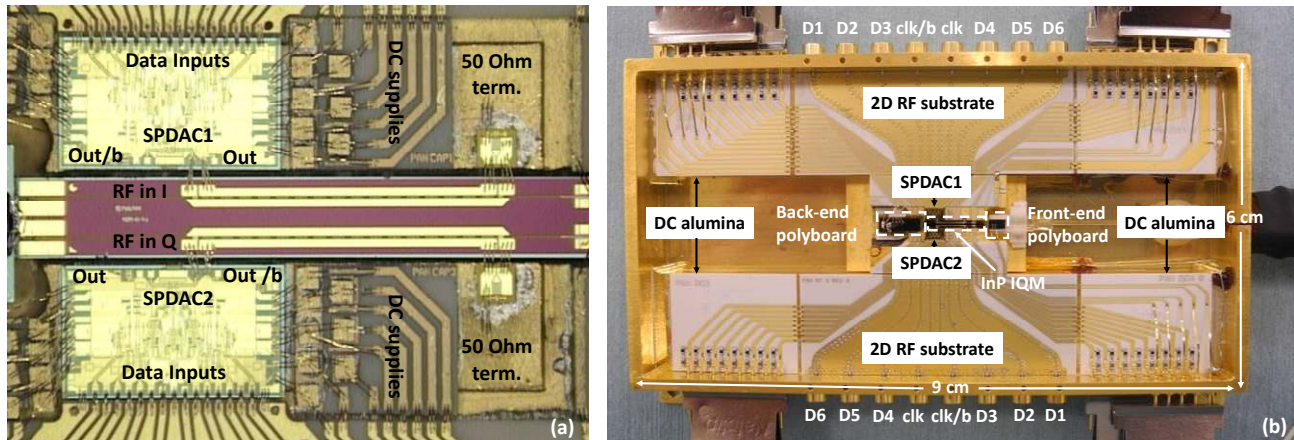


Figure 6. (a) Close-up of the electrical interconnects between the SPDACs and the two MZMs on the InP chip, and (b) final assembly of our multi-format SP-IQ transmitter tunable inside the package.

signals (D1, D2, D3, D4, D5 and D6) and two more for the complementary clock signals (clk and clk/b). All eight signals with amplitude up to 400 mVpp operate at rates up to 32 Gb/s and 32 GHz. Taking advantage of the 2:1 multiplexing stage, the output multi-level signals can have up to 8 levels and symbol-rate up to 64Gbaud. The multilevel electrical signal after the DAC stage on-chip is forwarded to the cascode architecture for the output buffer that is responsible for the linear amplification of the generated multilevel signal at both outputs (out and out/b). The power consumption of the circuit is 2.9 W. Measured eye-diagrams on-wafer at 50 and 64 Gbaud are presented in Figure 5(b) and Figure 5(c) with differential amplitude up to 4.3 Vpp. Both eye-diagrams are of high quality and reveal the high-speed potential of the InP-DHBT electronics technology.

Within our transmitter, the two SPDACs are used for the driving of each MZM and thus for the modulation of the I and Q components of the final QAM signal. Figure 6(a) gives a close view of the integration of the SPDACs with the InP chip. More specifically, on the top and the bottom of Figure 6(a) it is shown how the outputs of the two SPDACs are connected with ultra-short wire bonds (<150  $\mu\text{m}$ ) to the RF travelling wave electrodes of both the I and Q MZMs. At their end, the RF travelling wave electrode lines are directly connected to a 50 Ohm termination. Since the MZMs have been designed for single-drive operation, the unused output of each SPDAC is terminated using an on-chip 50 Ohm resistor. Figure 6(b), on the other hand, depicts the final assembly of our transmitter inside its FeNiCo package. The optical subassembly is based on the use of gold plated submounts of CuW that provide mechanical support for the optical and electrical components, DC and RF coupling substrates, active thermal control with a thermo-electric cooler (TEC), and a lensed fiber for the coupling of the modulated signal out of the box. Regarding the RF coupling substrates, an RF interposer is used for the connection of the input RF connectors (GPPO connectors) to the SPDACs on either side of the transmitter. In more detail, the RF interposer has been designed for 45 GHz 3-dB bandwidth, and has been implemented on alumina substrate, where 50 Ohm RF microstrip lines connect the eight GPPO connectors to the SPDACs through coplanar waveguide (CPW) RF lines on a second RF alumina. Due to the complexity of the device, its total power consumption is estimated to be around 15.7 W (or 41 mW/Gbps) taking into account the consumption of the tunable laser (0.215 W), the consumption of the two SPDACs (5.8 W), the phase-shifters for the biasing of the 2 MZMs (0.12 W), the phase shifter for the 90° relation between the I and Q component (0.02W), and the TEC (around 9.5 W). The total optical loss in the package is 7 dB including the propagation loss and the insertion loss of all elements in the 3 discrete photonic integrated circuits, the coupling losses between the 3 circuits and the fiber coupling loss. This total loss of 7 dBm results in -2 dBm output power, when the device is tested without modulation signal (continuous wave operation) at the transmission peak of each MZM.

### 3. DESIGN AND INTEGRATION CONCEPT OF SP COHERENT RECEIVER

The layout of our tunable SP coherent receiver is depicted in Figure 2 and it is capable of mQAM ( $m=4, 16, 64$ ) signal detection up to 64 Gbaud. Our device is based on the hybrid integration of a PolyBoard chip with a high-speed quad InP-pin PD array comprising the optical sub-assembly. Only one input fiber is coupled to the PolyBoard chip and is associated with the modulated signal, while this device employs an integrated tunable LO oscillator in order to add additional functionality to the receiver. An amplification stage based on high-speed InP-DHBT differential transimpedance amplifiers (DTIAs) follows the optical sub-assembly.



### 3.1 Optical design and optical integration of SP coherent tunable receiver

According to figure 7 (d), the PolyBoard chip of the receiver's side accommodates a LO, which is an external cavity relying on the hybrid integration of an InP GC with the monolithic BG on chip using butt-coupling technique, two variable optical attenuators (VOAs) for adjusting the relative optical power between LO and input signal and a 90° optical hybrid. The performance of the tunable LO was evaluated, and typical power-current (P-I) curves measured at the output waveguides O1-O4 for a lasing wavelength of 1550 nm are shown in Figure 7 (a). At a gain current of 100mA, the output power at the 4 outputs vary in a range between 0.95 and 1.1 mW, which result in maximum output power of 1.1 mW including 0.7 dB coupling losses with lensed fibers. In Figure 7 (b)-(c), the measured lasing wavelengths and corresponding SMSRs at different BG heater power are shown, revealing a tuning range of more than 20 nm and an SMSR better than 40 dB with maximum heater power lower than 40 mW.

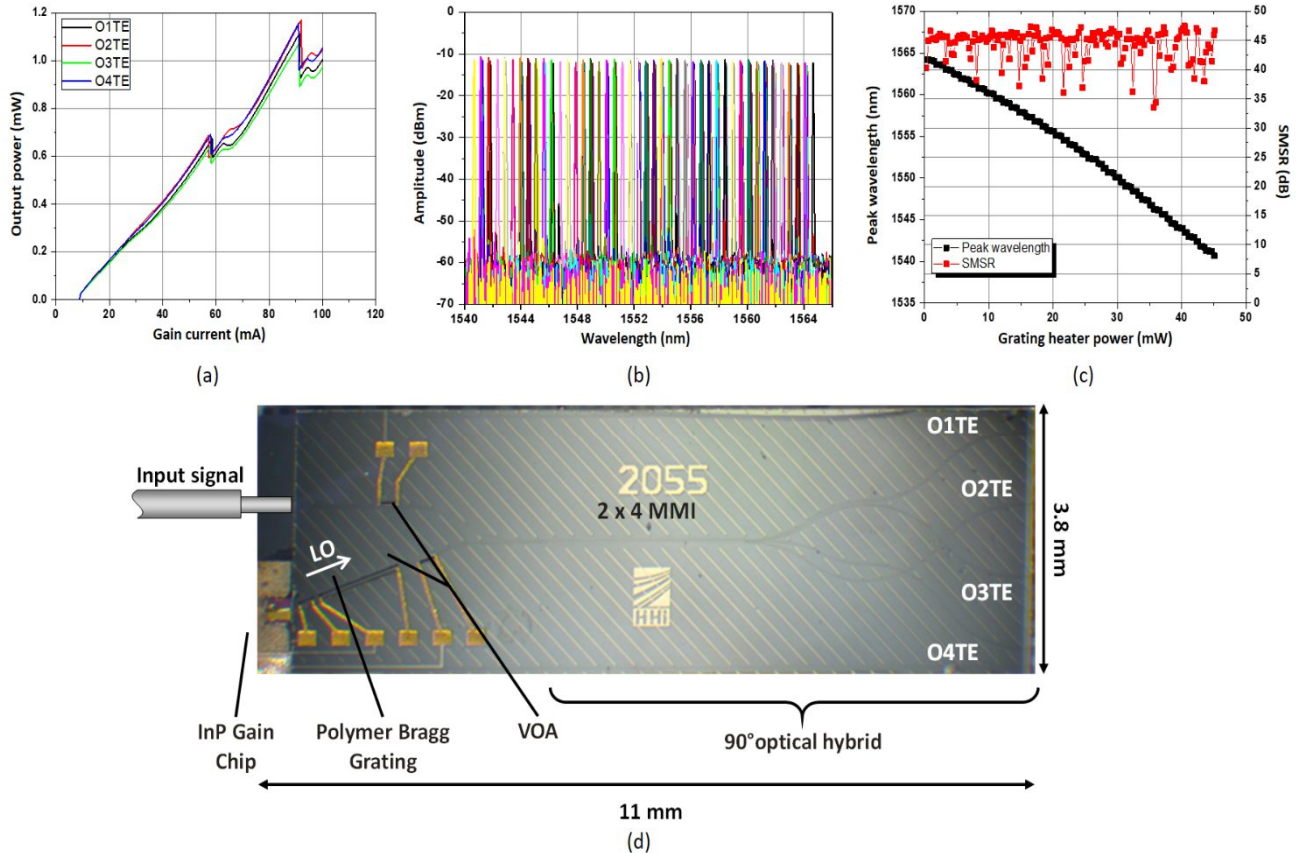


Figure 7. (a) Measured P-I curve, (b) optical spectra with 20 nm tunability of optical coherent receiver polyboard for an input signal with TE polarization, (c) P-I curve of the LO, and (c) tuning behavior of the integrated LO in SP-coh. receiver and (d) photograph of the PolyBoard with InP GC for the SP coh. receiver.

The performance of the receiver 90° optical hybrid, which is based on a polymer 2x4 multimode interferometer (MMI) design [42], is depicted in figure 8. Insertion losses from the signal input to the outputs O1-O4 of the PolyBoard were measured using SSMFs, and the results for transverse electric (TE) polarization input signal are shown in Figure 8 (a). The receiver's PolyBoard for TE polarization at the outputs O1-O4 show similar performance, with insertion loss lower than 11 dB in the C-band, of which approximately 1.6 dB are attributed to the fiber-to-chip and chip-to-fiber coupling losses, while the imbalance between the output ports results in lower than 0.6 dB.

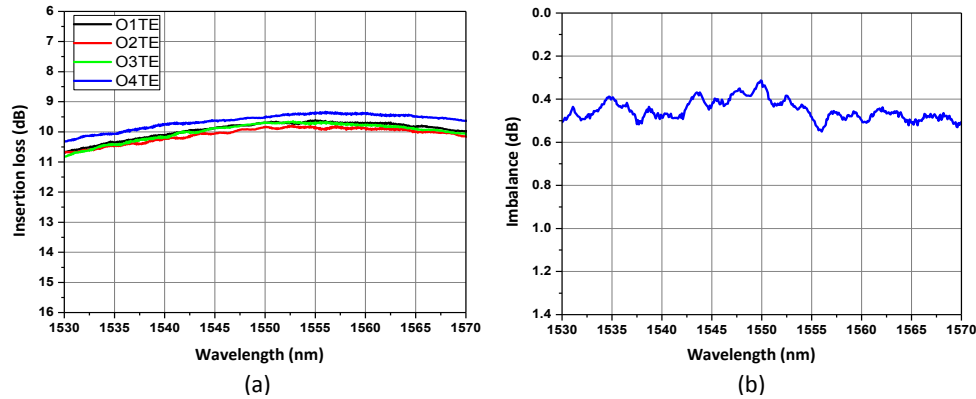


Figure 8. (a) Insertion loss, and (b) imbalance of receiver's PolyBoard for an input signal with TE polarization.

For the photonic detection part of the device, the pin-PDs are monolithically integrated with the rib waveguides of the InP platform, having a width of  $2\ \mu\text{m}$  and are coupled evanescently to an absorbing InGaAs layer with a thickness of  $350\ \text{nm}$  by means of an internal matching layer. This matching layer serves additionally as the n-contact of the pin PD. A sophisticated p-type heterostructure contact layer stack, which is optimized to ensure low polarization dependent loss (PDL), serves as low ohmic contact access to the pin PD as reported in [45]. The size of the PD mesa is  $5 \times 20\ \mu\text{m}^2$  and the specific mesa design is combined with a  $50\ \Omega$  termination resistor. The presence of this resistor results in  $0.65\ \text{A/W}$  responsivity and low conversion gain ( $16\ \text{V/W}$ ). Figure 9 (a) shows a close view of the quad InP-pin PD array with  $1\ \text{mm}$  pitch, while figure 9 (b) presents the on-wafer heterodyne bandwidth measurements for all PDs with average 3-dB bandwidth higher than  $90\ \text{GHz}$ . From bandwidth measurements, the potential of the specific PD design for operation at bit-rates up to  $64\ \text{Gb/s}$  and beyond is confirmed. The integration of the two photonic chips relied on the butt-end coupling technique comprising the optical sub-assembly of the SP coherent tunable receiver, while a taper structure deployed on the designed PolyBoard waveguides of the  $90^\circ$  optical hybrid in order to ensure the optimization of coupling efficiency between the two facets.

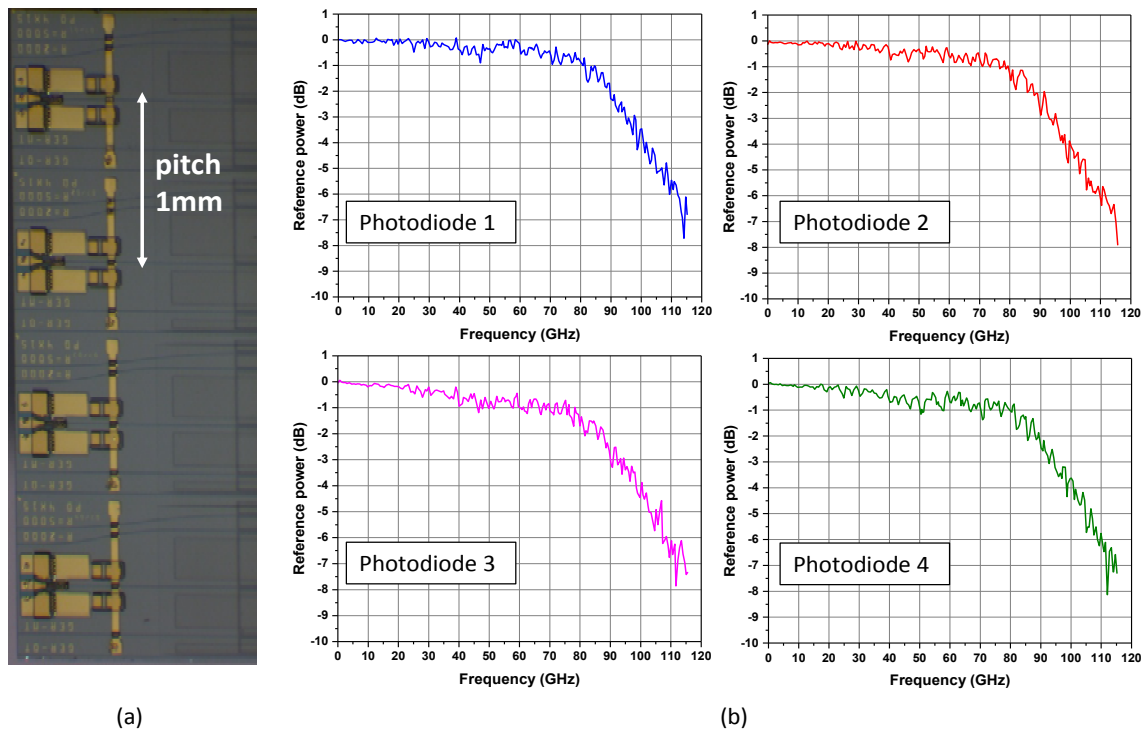


Figure 9. (a) Photograph of quad InP-pin PD array with  $1\ \text{mm}$  pitch, and (b) on-wafer frequency response measurements of a WG-PD quad-array with mesa size of  $5 \times 20$  with  $50\ \Omega$  termination.

### 3.2 Electrical design and packaging of SP coherent tunable receiver

The electrical part of our SP coherent tunable receiver is based on two mirrored InP-DHBT differential TIAs (DTIAs) at the back-end of the device. Each electrical circuit comprises two independent DTIA units on the same die (dual DTIA array) with manual gain control and 3-dB bandwidth higher than 50 GHz. Consequently, each TIA's differential output voltages after the reception of the generated electrical signals from the quad InP-pin PD array provide the wanted in-phase and quadrature two level baseband signals with amplification to fit in the dynamic range of the processing units coming after the TIA increasing by this way the overall sensitivity of the proposed SP coherent tunable receiver.

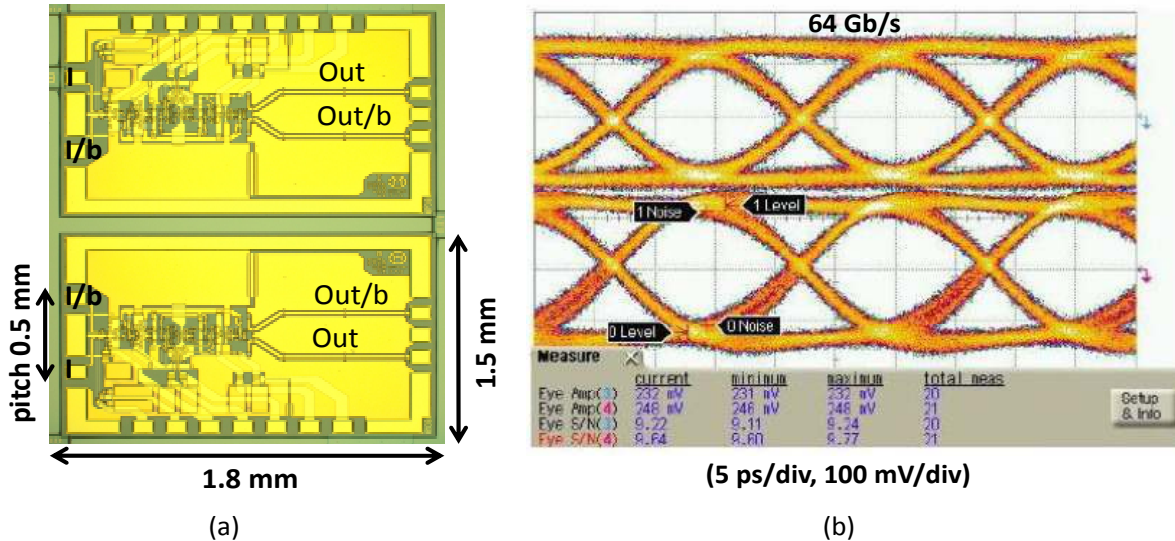


Figure 10. (a) Fabricated DTIA chips' microphotographs (size: (2x)1.8x1.5 mm<sup>2</sup>), and (b) electrical output eye diagrams measured on-wafer for OOK at 64 Gb/s.

Figure 10 (a) presents a micro-photograph of the fabricated dual DTIA circuit with footprint 1.8x1.5 mm<sup>2</sup> and input pitch 0.5 mm, while on the left side of the photograph are depicted the two input ports for the input data signals (I, and I/b for each circuit). Each unit receives two input data signals from the quad InP-PD array up to 64 Gb/s and perform a subtraction of the photocurrents [46] resulting in amplified complementary OOK signals at output ports (Out and Out/b). The power consumption of each units is below 0.6 W, while OOK eye diagrams of single DTIA measured at 64 Gb/s are shown in Figure 10 (b) revealing excellent eye opening and similar signal quality for both complementary outputs with Signal-to-Noise (S/N) ratio above 19dB.

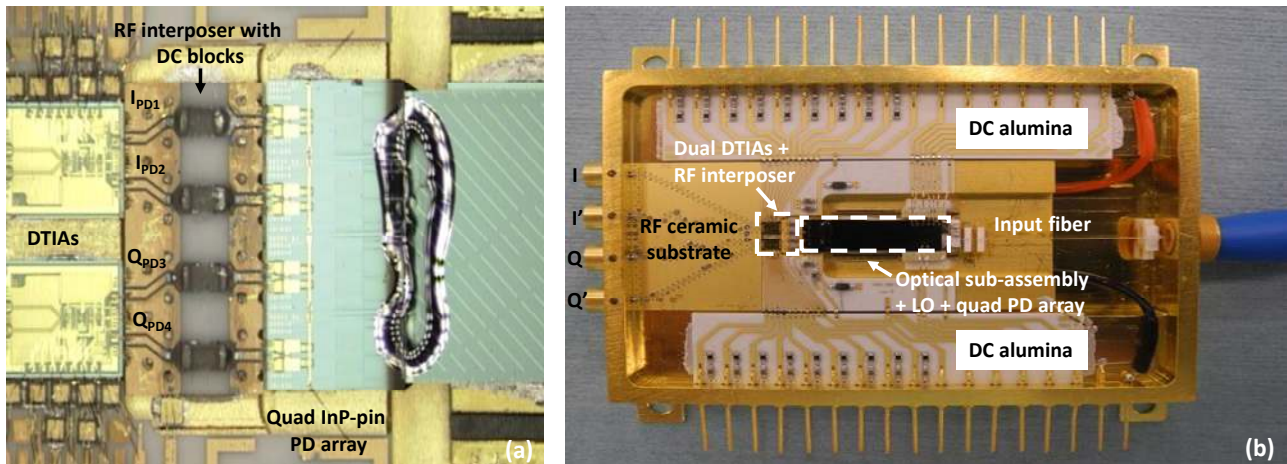


Figure 11. (a) Close view of RF interposer with DC blocks interconnecting DTIAs and quad PD array and (b) packaged device of 64 Gbaud SP coherent tunable receiver.



Since the pitch of the quad InP-pin PD array (1 mm) is different to the pitch of the DTIA (0.5 mm) and the two components have different impedances at the respective ports, an RF interposer needed to be used in between the two units. Figure 11 (a) provides a close view of the developed RF interposer on  $\text{Al}_2\text{O}_3$  material with DC blocks on signal electrodes to match the characteristics of the two components. Following this approach, the DTIA inputs managed to hybrid integrated with the quad InP-pin PD array through the use of the intermediate RF interposer. Moreover, high frequency gold wire-bonds with ultra-short lengths ( $<150\mu\text{m}$ ) are used to connect the RF paths while standard ribbon bonding is used for the DC interconnects. The polyboard, PD array and TIAs are placed on a CuW submount with a TEC beneath for the thermal management of the active devices and are placed inside a kovar case, that constitutes the 64 Gbaud SP coherent tunable receiver, as shown in figure 11 (b). One input with a lensed fiber is employed and concerns the coupling of the optical modulated signal in the device, while an RF ceramic substrate with 50 Ohm microstrip structure and 3-dB bandwidth higher than 45 GHz developed and placed in between the four GPPO connectors and the outputs of the two DTIAs through CPW RF lines to support high bit rates. Regarding the total power consumption, due to the complexity of the receiver, it results in 11.6W (or 30 mW/Gbps), taking into account the consumption at the VOAs (0.64W), LO (0.215W), PD array (0.02W), TEC (9.5W) and two DTIAs (1.2W) circuits.

#### 4. EXPERIMENTAL SETUP AND RESULTS

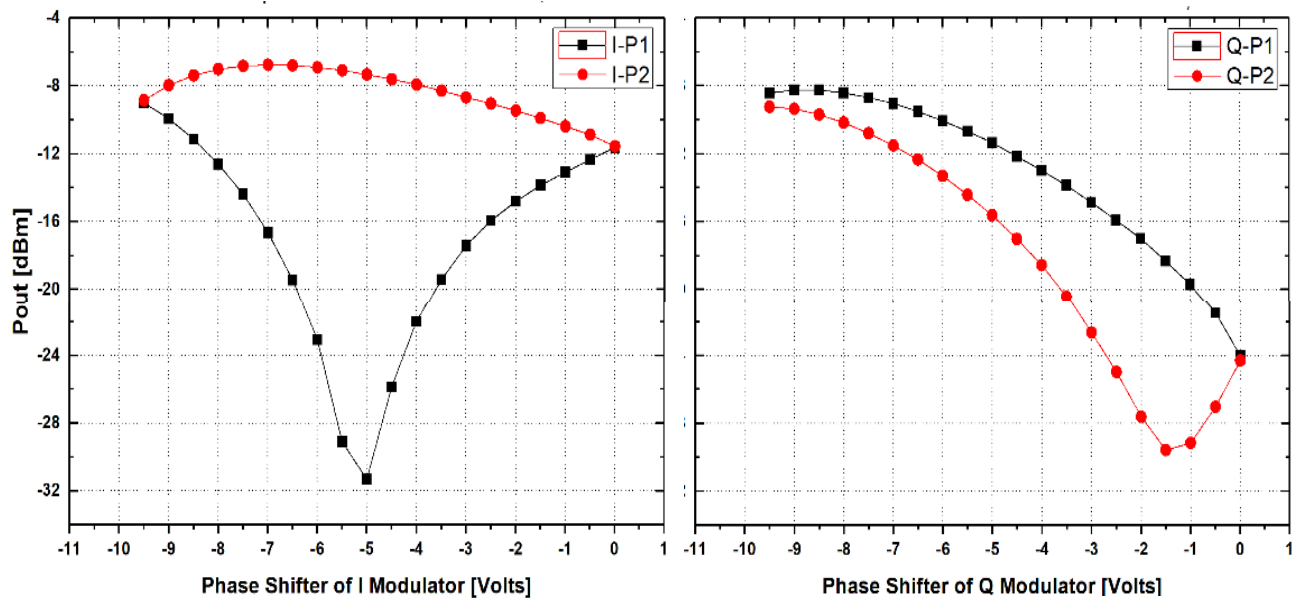


Figure 12. Static transfer functions of I (MZM1) and Q path (MZM2) at 1553.2 nm as a function of the bias voltage on their PS.

Figure 7 presents the basic results from the static characterization of the 64 Gbaud multi-format SP-IQ tunable transmitter. It depicts the power of the 1553.2 nm continuous wave (cw) at the transmitter output as a function of the bias voltage on the thermal phase shifters of the respective InP MZM. More specifically, each InP MZM has two bias phase shifters P1 and P2, which act in a complementary way, as the first bias phase shifter increases the optical power up to the maximum value at the output of the transmitter, while the second one is responsible for achieving the minimum optical power. The transfer functions were measured at a stable temperature of  $40^\circ\text{C}$ , as, at this condition and in the range of 1550 nm for the emitting wavelength, the InP MZMs achieve the best performance in terms of extinction ratio, switching voltage and insertion loss. The four curves exhibit extinction ratio, which ranges from 21.5 dB in the case of Q MZM to 24 dB in the case of I MZM. The maxima of these curves have only 1 dB difference ( $-8$  dBm for Q MZM1 and  $-7$  dBm for I MZM) and reveal the low imbalance of the Y-junction couplers from both back-end and front-end PolyBoards and comes in agreement with the measurements on the test structures presented in Figure4. By adjusting the bias points to the maximum values for each MZM, the total optical power at the output of the transmitter measured  $-2.04$  dBm, while when biases shifted to the minima the optical output power reached  $-25.84$  dBm.

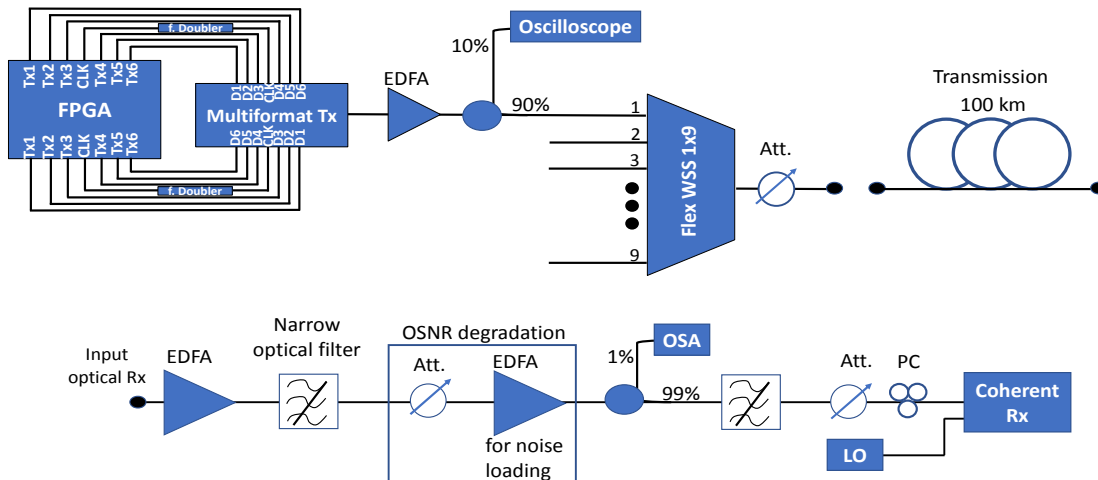


Figure 13. Experimental setup of module 1 in lab settings.

The evaluation of the 64 Gbaud SP-IQ tunable transmitter has been performed in a laboratory environment as well as in a field trial on a system testbed that was deployed in the Telecom Italia network. It is noted that the reconfiguration of the emitting wavelength of the integrated laser and the selection of the desired modulation format and symbol rate was controlled by a software defined optics (SDO) agent [23]. Specifically, the SDO controlled in real time the applied currents on the InP GC and on the BG of the back-end PolyBoard chip, while on the other hand it defined the number and the bit rate of the generated electrical binary sequences from an FPGA board that drove the multi-format SP-IQ tunable transmitter. In principle, a wide range of modulation formats can be implemented in the proposed SP-IQ transmitter module achieving modulation formats up to 64QAM. However, due to a malfunction on one out of the 3-bits of the upper SPDAC that drives the InP I MZM, the highest modulation format was limited to 16QAM.

The first experimental setup that was established in the laboratory environment is depicted in Figure 13. A Xilinx Virtex 7 series FPGA board generated  $2^{11}-1$  long pseudo-random binary sequences (PRBS) and two clock signals in order to drive the two SPDACs of the multi-format SP-IQ tunable transmitter. SP-QPSK and the SP-16QAM formats were utilized, while the symbol rate was set at 25 Gbaud defining the maximum number of the generated electrical binary sequences from the FPGA board to eight with a bit rate of 12.5 Gb/s each. The developed FPGA design satisfying these specifications confined the frequency of the generated clock signals to 6.125 GHz. The frequency up conversion of the clock signals to 12.5 GHz was performed using electrical amplifiers followed by passive frequency doublers. The decorrelation between the binary electrical sequences was achieved using different patterns that were loaded on the FPGA board, while electrical phase shifters were used to enable bit-level synchronization before entering the input ports of the SP-IQ transmitter.

The integrated laser emitting at 1553.2 nm generated the optical carrier, whose amplitude and phase was modulated by the InPMZM array. By adjusting the bias PS of both MZMs to the minima transmission points, the output optical power of the transmitter was measured at -25 dBm. Due to the low optical power, an EDFA was employed for the amplification of the generated SP-QPSK or SP-16QAM optical signal at 25 Gbaud before entering the 9x1 flexgrid wavelength selective switch (WSS) with 50 GHz wide flat passband. The WSS constitutes a part of an ingress node aggregating optical signals coming from a transmitter array, based on SP-IQ transmitters and/or multiflow transmitters [23] in order to perform optical signal distribution to the desired direction following the network scenarios. At the receiver side, the optical signal was amplified after the 100 km SSMF transmission to compensate the losses, while an optical band-pass filter, filtered out the out-band ASE noise.

The performance of the system was evaluated in back-to-back (B2B) and transmission measurements, by degrading the optical signal-to-noise ratio (OSNR) using an optical attenuator followed by an EDFA and an optical band-pass filter. Finally, an optical attenuator in front of the coherent receiver, kept the optical power of the signal stable for the different values of the OSNR, while a polarization controller ensured the proper polarization state of the received signal. A low linewidth laser source (100 kHz) is utilized as LO for the coherent receiver. The detected photocurrents were sampled and stored by a real-time oscilloscope with 33 GHz bandwidth, 80 GSa/s (Agilent DSAX93304Q) and decoded using an in-house developed DSP toolbox.



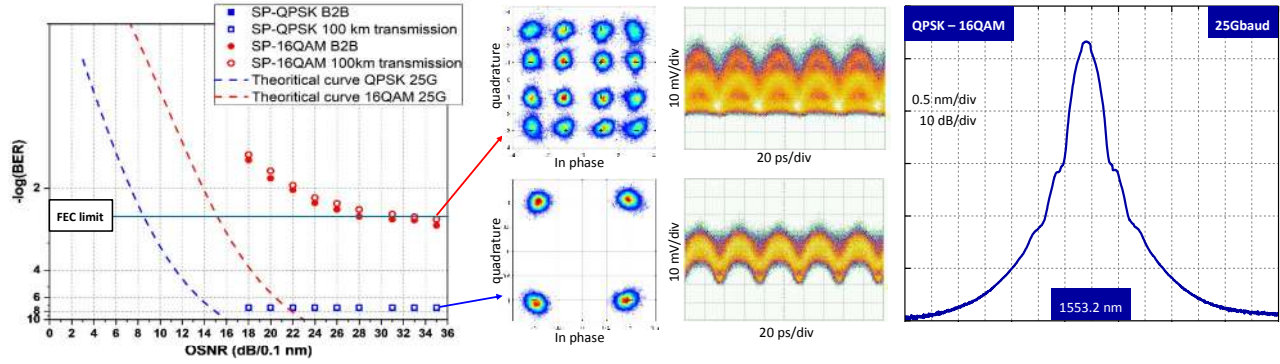


Figure 14. BER vs. OSNR measurements for B2B and transmitted SP-QPSK, SP-16QAM at 25 Gbaud signals (100 km) together with the theoretical limits, the correspondent IQ constellations at maximum OSNR and the received optical spectra.

Figure 14 depicts optical eye diagrams at the output of the SP-IQ transmitter and their respective constellation diagrams at maximum OSNR after offline DSP for SP-QPSK and SP-16QAM signals at 25 Gbaud. The received BER curves as a function of OSNR are depicted on the left side of Figure 14 for both modulation formats at 25 Gbaud for back-to-back (B2B) and after 100 km transmission over SSMF. Dot lines represent the theoretical BER curves for the respective format and rate, while symbols correspond to the measured BER values. It is noted that the minimum BER value was limited by the memory of the real-time oscilloscope and consequently by the maximum number of the stored samples. For the SP-QPSK signal, the minimum feasible OSNR value was 18 dB, resulting in an error free operation for both B2B and transmission with only 3 dB OSNR penalty relative to the theoretical results, while for the SP-16QAM signal error-free operation has been achieved for OSNR values above 28 dB considering hard-decision (HD) FEC limit with 7% overhead at a BER of  $3.8 \cdot 10^{-3}$ . However, there is larger than  $\sim 10$  dB penalty relative to theoretical results for 25 Gbaud SP-16QAM signal at the same BER level. We believe that the discrepancy between experimental and theoretical results is mainly due to the low RF swing generated by SPDACs for driving the InP IQ modulator. Due to the malfunction on the medium bit of the upper SPDAC, it was possible to use only the most significant bit (MSB) and least significant bit (LSB) at the inputs of the SPDACs, thus resulting in PAM4 signals with RF swing lower than 1.5 Vpp and closer amplitude levels. For this reason, an under-driven modulation scheme is applied on the InP IQ modulator. Better performance in terms of BER values can be achieved by using the combination of MSB and medium bits of the SPDACs for generating the 16QAM signal.

Regarding the second part of the experimental validation of the SP-IQ transmitter, a metro regional link between Turin and Chivasso in the north-west region of Italy was employed to emulate a realistic on field fiber condition, without any modification to the existing line system. Two different links were available with total fiber lengths of 156 km and 232 km respectively. For the purposes of the field trials, the modulation format was QPSK at 25 Gbaud/s symbol rate, defining the selection of the second link as the more appropriate for the evaluation of the SP-IQ transmitter.

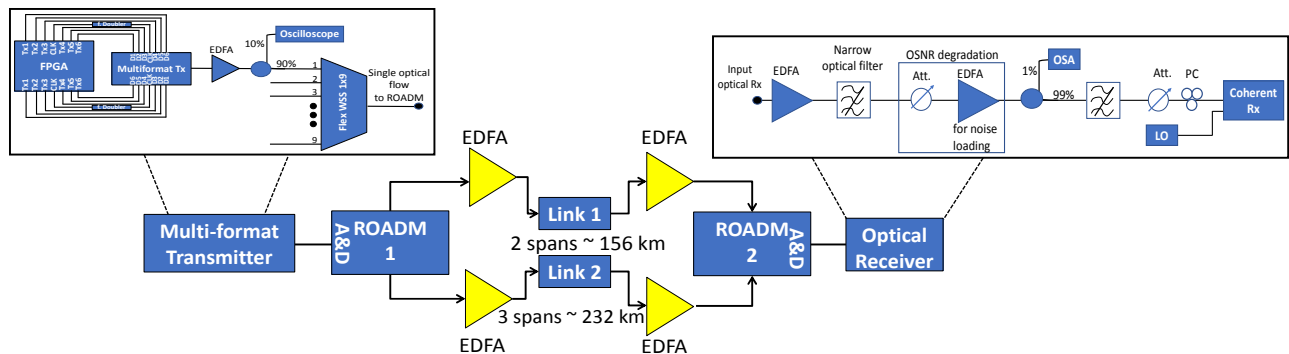


Figure 15. Experimental Setup of SP-IQ transmitter inside the field of Telecom Italia in Turin.

The experimental setup and the operating conditions remained the same for the transmitter and receiver side as they have been described for the laboratory experiment. The interface with the metro regional link was based on reconfigurable optical add-drop multiplexers (ROADMs) followed by EDFAs to compensate for the insertion losses. In addition,

EDFAs were also used for the compensation of the losses induced by the transmission on the link. The developed SDO agent was integrated with a software defined network (SDN) controller for real-time reconfiguration and control of the optical parameters of the ROADM nodes. Figure 16 presents the measured BER curves with respect to the OSNR of the received optical SP-QPSK signal at 25 Gbaud for B2B and transmission over 232 km. Figure 16 presents the measured BER curves with respect to the OSNR of the received optical SP-QPSK signal at 25 Gbaud for B2B and transmission over 232 km.

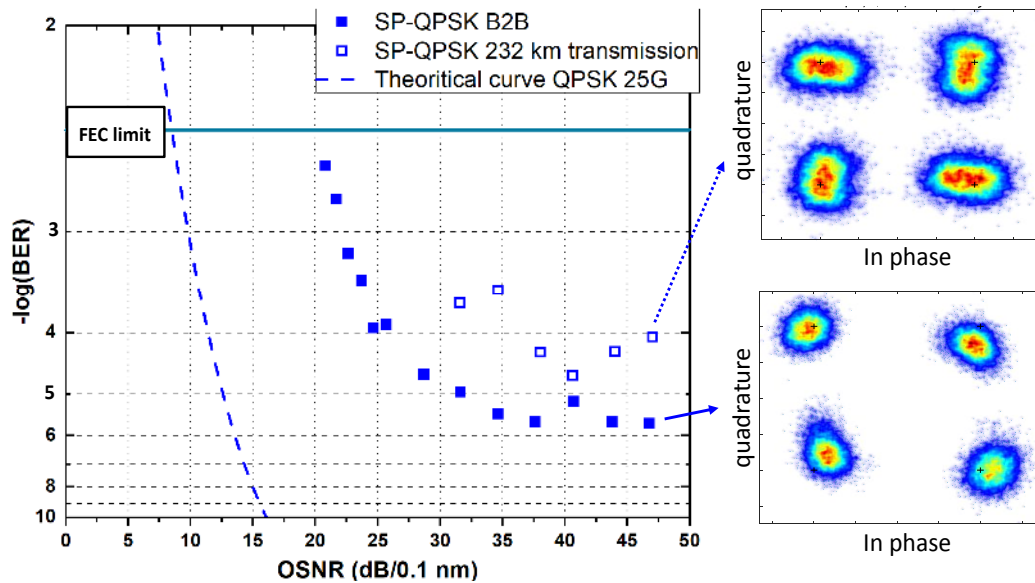


Figure 16. BER vs OSNR measurements for B2B and transmission over 232 km in the field link for SP-QPSK at 25 Gbaud and the respective constellation diagrams after offline DSP for maximum OSNR values.

Both sets of results were gathered and plotted in one graph to compare their performance and to evaluate the OSNR penalty with respect to the theoretical curve of SP-QPSK at 25 Gbaud. HD FEC threshold with 7% overhead is also depicted in the BER vs OSNR plot validating the proper performance of the device. Blue and blue-white symbols correspond to the B2B and transmission curves respectively, while the blue-dot curve is related to the theoretical values. In the case of 25 Gbaud SP-QPSK signal with 50 Gb/s total bitrate, error free performance has been achieved for all OSNR measurements for both B2B and transmission cases, as the BER values for OSNR above 20 dB are well below the HD-FEC limit ( $3.8 \cdot 10^{-3}$ ), considering FEC with 7% overhead.

A BER value of  $\sim 2.5 \cdot 10^{-3}$  has been achieved with an OSNR value of 21 dB. This corresponds to high relative penalty ( $\sim 12$  dB) respective to theoretical curve. This can be justified by the low performance of the phase shifter on the front-end PolyBoard of multi-format SP-IQ tunable transmitter that leads to phase misalignment between I and Q, which can also be confirmed by the constellations of figure 16. Even in the case of transmission, the performance of the device reveals error free operation as the measured BER values are far below HD-FEC limit. These variations between the measured OSNR values are mainly due to the instantaneous changes in the signal's polarization state, which are typical on a field environment.

## 5. CONCLUSIONS

We have presented the system and integration concept of a hybrid SP-IQ transmitter with wavelength tunability and a coherent receiver, which both are based on the hybrid integration of PolyBoards with InP photonic chips and InP-DHBT electronic chips and have the theoretical potential component-wise for operation at rates up to 64 Gbaud. The transmitter is capable of different mQAM ( $m=4, 16, 64$ ) modulation formats using two integrated 3-bit power DACs inside the box for driving an array of two InP MZMs, and using two PolyBoards for generating a laser line over a 23 nm range inside the C-band, and for combining the outputs of the two MZMs into a single IQ signal. The coherent receiver comprises a tunable local oscillator and a  $90^\circ$  optical hybrid on its front-end PolyBoard, a quad PD array on its InP chip and a pair of high speed InP-DHBT TIAs. Results from the extensive experimental tests of the transmitter at 25 Gbaud have been presented confirming error-free operation with QPSK and 16-QAM signals in lab and real-network settings. Further experimental efforts involve the investigation of the transmitter performance at higher symbol rates (up to 64 Gbaud), as well as the system testing of the SP receiver.

## ACKNOWLEDGMENTS

The present work was supported by the European Commission through the project ICT-PANTHER (Contract No. 619411) funded under the seventh Framework Programme (FP7).

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