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Optimal Design Methodology for High-Order Continuous-Time Wideband Delta-Sigma Converters

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Abstract— A systematic design methodology for high-order continuous-time wideband Delta-Sigma modulators is proposed. This method provides a direct way for determining the coefficients of the modulator. Trade-offs between the choice of the coefficients and the power consumption is analyzed. The method is illustrated for a 4th-order 4-bit modulator with OSR of 8, while 20 MHz signal bandwidth and 12 bit resolution is achieved. The required GBW of the first integrator is less than 1.5 times the sampling frequency, which reduces the overall power consumption.

I. INTRODUCTION

In recent years continuous-time Delta-Sigma modulators (CT DSMs) are preferred over their discrete-time (DT) counterparts for applications with larger signal bandwidth due to their faster speed and lower power consumption. However, CT DSMs are susceptible to non-idealities such as clock jitter in their feedback digital to analog converters (DACs), excess loop delay and inaccurate RC time constants.

Among the DSM topologies the single-loop modulators do not require very accurate coefficient matching and they demand opamps with lower dc gain. Also their other circuit requirements are more relaxed compared to their cascade counterparts at the expense of being more prone to instability and reduced signal-to-noise-ratio (SNR). Single-bit single-loop DSMs are the most popular type used for low-bandwidth standards in the past [1] [2] because of their relative simplicity and high linearity. However, future mobile communication systems demand larger bandwidth and higher speed. If a single-bit quantizer is used, a large oversampling ratio (OSR) and a gigahertz sampling frequency are needed for upcoming standards like WLAN802.11n (which has a baseband signal bandwidth up to 20MHz). This makes the design extremely difficult since opamps with very large GBW are needed and the quantizer has to be fast enough to not degrade the overall performance. In such cases, a multi-bit quantizer can be employed to reduce the sampling frequency and the clock jitter influence. In addition, the stability is also improved compared to the single-bit type. The drawback brought by the multi-bit quantizer is the presence of a less linear multi-bit DAC in the feedback path. Since Dynamic Element Matching [3] or digital calibration [4] can be applied to solve this problem, the linearity problem of the multi-bit DAC won't be elaborated further in this paper.

In this paper a design methodology for single-loop high-order multi-bit CT DSMs for wideband applications is presented. In section II the proposed design methodology of the high-order multi-bit CT DSMs is described and is illustrated for a 4th-order 4-bit modulator. In order to verify the proposed design methodology, MATLAB simulations are performed in section III. Finally, the paper is concluded in section IV.

II. DESIGN METHODOLOGY FOR SINGLE-LOOP MULTI-BIT CT DSMs

In this section the design methodology for single-loop high-order multi-bit CT DSMs is described. For this purpose a forth-order CT DSM with low oversampling ratio and with multi-bit quantizer is

designed for a wideband application as an illustrative example in this paper.

A. NTF Design

There are two main techniques for designing the NTF. One is based on the design of a DT DSM first, from which an equivalent CT DSM is computed afterwards. The other one is based on a full design in continuous time. The design techniques based on the continuous-time domain as proposed in [5] however have two disadvantages. First, the linear model used is only valid for single-bit CT DSMs [6]. Secondly, the model seems to be more adequate for CT DSMs with high OSR since it has not included the sampling process that occurs inside the loop. In addition, the design technique does not indicate how to systematically solve the influence of excess loop delay (ELD) and the sampling instant uncertainty, whereas good techniques exist for DT modulators. We therefore present a design methodology that designs in the DT domain first and that converts it to the CT domain afterwards.

The starting point of our methodology is to specify certain specifications according to the targeted application, namely dynamic range, SNR, required signal bandwidth (BW) and maximum clock frequency. In the first step, the proper values for the modulator order, the number of quantizer bits and the OSR has to be chosen to meet the specification requirements. To illustrate the methodology, we will use the example of designing a wideband CT DSM modulator with signal bandwidth around 20 MHz and with more than 11 bit resolution. Since the signal bandwidth is very high, we need to use a low OSR ratio, which in our case is 8, as to minimize the sampling frequency and to reduce the corresponding gain-bandwidth of the opamps used in the integrators. The proper number of quantizer bits and the modulator orders can be estimated by using the following formula [7], which gives the ideal performance of a DSM :

$$DR = \frac{3}{2} \cdot \frac{2n+1}{\pi^{2n}} \cdot (2^N - 1)^2 \cdot OSR^{2n+1} \quad (1)$$

With a 4th-order modulator and a 4-bit quantizer, the ideal SNR is around 76 dB when the OSR is 8. However, this SNR will be lower when stability is taken into account. To maintain a certain margin, the zeros of the noise transfer function can be spread over the signal bandwidth to reduce the in-band quantization noise.

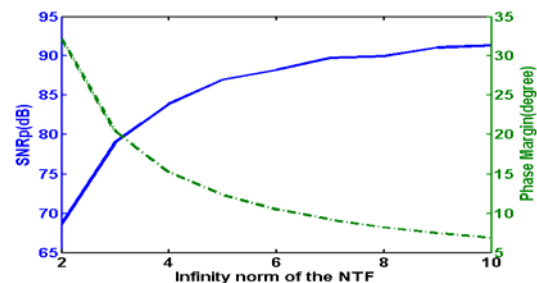


Fig. 1. Peak SNR and phase margin vs. the infinity norm of the NTF.

The second step in the methodology is to find an initial stable NTF. For the single-bit case, the $\|x\|_{\infty}$ (the infinity norm of the NTF) is normally chosen to be 1.5 as a rule of thumb to maintain stability. For the multi-bit case, the $\|x\|_{\infty}$ can be increased to improve the SNR. Fig. 1 shows the simulated peak SNR versus $\|x\|_{\infty}$. It is obvious that the peak SNR is continuously increasing as the $\|x\|_{\infty}$

value increases. However, the SNR does not increase a lot when $\|x\|_\infty$ is larger than 5 and the phase margin of the open-loop transfer function is decreased to less than 15 degrees. To balance between the SNR performance and enough stability margin, $\|x\|_\infty$ is chosen to be 4. Then using the Synthesize algorithm of Schreier's toolbox [8] results in the NTF of a DT filter where its closed-loop poles are placed as to increase the peak SNR of the modulator while guaranteeing the stability of the loop. For our example this gives :

$$NTF(z) = \frac{(z^2 - 1.982z + 1)(z^2 - 1.887z + 1)}{(z^2 - 0.7131z + 0.1458)(z^2 - 0.6831z + 0.3985)} \quad (2)$$

Then, considering the block diagram of Fig. 2a and the relation (3) between the NTF and the open-loop transfer function, the open-loop transfer function $H(z)$ is obtained as (4) :

$$H(z) = 1 / NTF - 1 \quad (3)$$

$$H(z) = \frac{2.472(z - 0.6234)(z^2 - 1.281z + 0.611)}{(z^2 - 1.982z + 1)(z^2 - 1.887z + 1)} \quad (4)$$

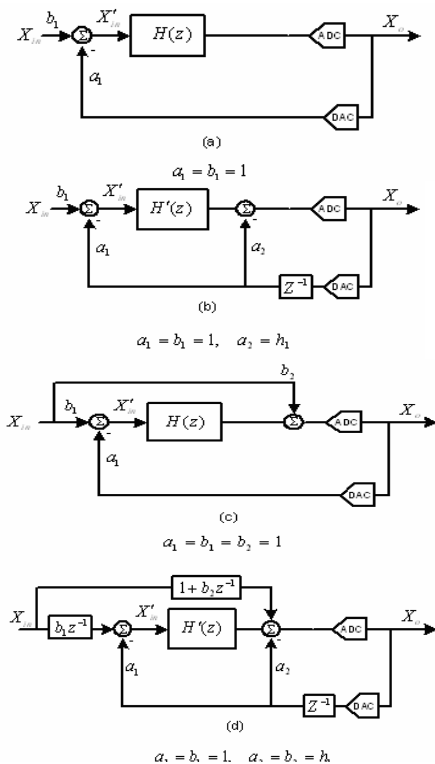


Fig. 2. (a) The block diagram of a DT DSM, depicting the loop gain. (b) The structure of a DT DSM with an intentional delay in the feedback path. (c) A simple solution to achieve a flat STF for Fig.2a. (d) A simple solution to achieve a flat STF for Fig.2b.

B. Excess Loop Delay

The third step in the design methodology is to compensate the Excess Loop Delay (ELD) without influencing the NTF. Although there are some traditional topologies for the realization of DT DSMs, they are not suitable for the realization of CT DSMs. The ELD of CT DSMs is a main problem for high-speed applications. Since the quantizer and the DAC are clocked by the same phase in Fig. 2a, any delay in the quantizer decision time and DAC output, called ELD, may degrade the performance and may even lead to instability, because this ELD pushes the feedback pulse out of one clock cycle into the next. This D/A pulse shift causes an additional zero in the NTF, located at $z=0$, which equivalently increases the modulator order and modifies its stability, while the in-band quantization noise power is unaffected.

A way to compensate the ELD of the modulator is to insert an intentional delay in the feedback path of the modulator [3,4] (see fig 2b). Compensating ELD has been considered in our proposed

methodology as follows. The open-loop transfer function is rewritten as follows :

$$H(z) = \frac{\sum_{i=1}^n a_i z^{-i}}{b_0 + \sum_{i=1}^n b_i z^{-i}} \quad (5)$$

$$H(z) = h_1 z^{-1} + z^{-1} H'(z) \quad (6)$$

In the example of this paper h_1 and $H'(z)$ are extracted from (6) as follows:

$$h_1 = 2.47 \quad (7)$$

$$H'(z) = \frac{4.858(z - 0.720)(z^2 - 1.483z + 0.706)}{(z^2 - 1.982z + 1)(z^2 - 1.887z + 1)} \quad (8)$$

Thus the structure of the DT DSM with an intentional delay in the feedback path will be as shown in Fig. 2b.

The method described above compensates exactly one period delay. In fact, the compensated delay can be chosen to be any value between one period delay and zero delay. However, for design convenience, only one period delay and half period delay is more suitable for a real implementation. The method used for the full-period delay compensation can also be used here for the half-period delay compensation. The only difference is that the initial z-domain transfer function given in the second step needs to be resampled using double the sampling frequency used in the full-delay design. Then the same method used in the third step can be applied to get the new loop filter function. For our example this gives :

$$H''(z) = \frac{1.48z^3 - 3.795z^2 + 3.327z - 0.9928}{z^4 - 3.967z^3 + 5.934z^2 - 3.967z + 1} \quad (9)$$

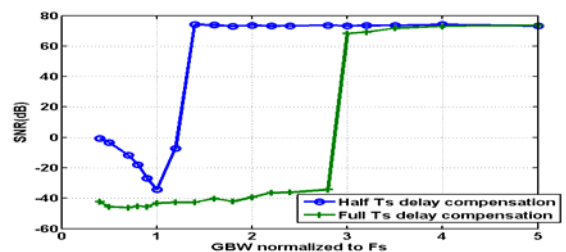


Fig. 3. SNR versus GBW for half-period and full-period delay.

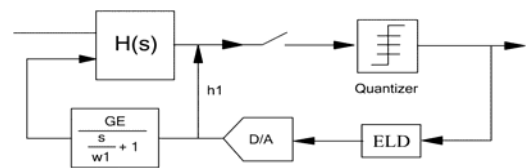


Fig. 4. ELD and delay caused by finite GBW.

When the same initial z-domain open-loop transfer function is used, the value of the compensated delay will have an influence on the minimal GBW needed to maintain the stability of the loop filter and this in turn influences the power consumption. It is found from behavioral simulations that a lower GBW can be used when a lower ELD needs to be compensated. As shown in Fig. 3, the minimum GBW of the first integrator using half-period-delay compensation can be reduced almost by half compared to the one using full-period-delay compensation (only the first integrator is set to finite GBW in the simulations). An intuitive explanation of this can be seen from Fig. 4 where the influence of the finite GBW of the first integrator is modeled as a gain error and a time delay [9]. Since the gain error can be solved by calibration, only the time delay is considered here. If a larger ELD exists in the feedback path, the tolerable delay caused by the GBW also needs to be

smaller, which means that a larger GBW is needed to reduce the delay. In order to achieve a better power efficiency while at the same time compensate a reasonable ELD, the half sampling period delay is chosen here for ELD compensation.

C. Signal Transfer Function (STF)

The forth step in the design methodology is to design a DT DSM with a unity-gain signal transfer function. A designer can employ some feedforward paths from the input signal of the modulator and select their coefficients to achieve a flat STF [10]. As a simple solution, by using the topology of Fig. 2c, a flat STF is obtained for an arbitrary loop transfer function $H(z)$ [11]. Similarly, the required equations are calculated and the structure of Fig. 2b is evolved into Fig. 2d. The benefit of the structures shown in Fig. 2c and Fig. 2d is that the input signal of the loop filter $X'_{in}(z)$ does not contain any product of the input signal of the modulator $X_{in}(z)$.

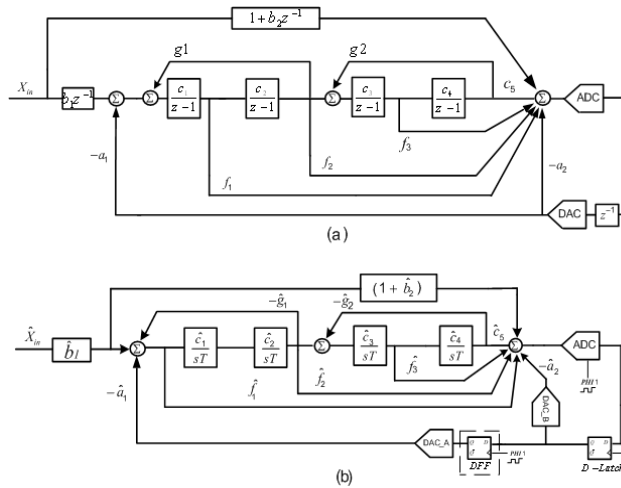


Fig. 5. (a) The CIFF architecture for the realization of the DT loop transfer function $H'(z)$. (b) The CIFF architecture for the realization of the CT loop transfer function $H'(s)$.

Therefore, it is concluded that the input signal of the loop filter $X'_{in}(z)$ involves the quantization noise only. So the harmonic distortion due to the nonlinearity of the loop filter, resulting from the analog circuit imperfections, is reduced. Also, this causes only the quantization noise to enter the loop rather than a part of the signal and as a consequence the required swing for the integrators will be reduced too and their linear behavior will be improved. Thus, in the design of the modulator it is important to choose the coefficients a_1 and b_1 identical.

In the forth step in the design methodology, the DAC feedback pulse shape is chosen first considering clock jitter sensitivity, required BW and slew rate of the opamps [9,12]. The use of a decaying waveform maximally minimizes the jitter influence [12], while the opamp power is increased due to increased slew rate. For our 20 MHz bandwidth case, an amplifier with very high GBW is needed when a decaying waveform is used. Therefore, the NRZ DAC shape can be used for low power consideration and reasonable jitter tolerance. Then the Impulse Invariant Transform (IIT) can be executed following the steps below to convert the DT solution to the CT domain.

First, the open-loop transfer function has to be calculated as a partial fraction expansion. Then, each fraction has to be converted from the z -domain to the s -domain. Finally, the results are recombined to get the CT loop transfer function $H'(s)$. The rectangular CT-DT transformation [13], which assumes a non-return-to-zero (NRZ) multi-bit DAC lasting from $\alpha=0$ to $\beta=T$, can be used to calculate the corresponding CT loop transfer function,

$H'(s)$. For our example this yields:

$$H'(s) = \frac{2.437s^3 + 1.948s^2 + 1.192s + 0.309}{s^4 + 1.344s^2 + 0.00203} \quad (10)$$

However, unlike for the loop gain of the CT DSM, it is not necessary to make a precise equivalence between the signal transfer function, STF, of the CT and DT DSMs [12]. Therefore, in our design methodology the following approximations are used:

$$z^{-1} \cong 1 \quad (11)$$

Thus, when a_1 and b_1 are chosen to be 1, the coefficient for the direct path from the signal input to the input of the quantizer is simply $1+h_1$ after the discrete- to continuous-domain transformation. The $STF(s)$ does not equal 1 exactly now due to the transformation approximation.

The fifth step in the design methodology is dedicated to architecture selection. There are several architectures such as CRFF (Cascade of Resonators Feedforward), CRFB (Cascade of Resonators FeedBack), CIFF (Cascade of Integrators FeedForward) and CIFB (Cascade of Integrators FeedBack) for the realization of the modulator [11]. Mostly used in recent designs because of some advantages [3] [4], Fig. 5 depicts the CRFF architecture which is mostly used in recent designs [3,4] and which is also chosen for the realization of $H'(z)$ and $H'(s)$ with the applied feedforward path to guarantee high linearity. Note that there are two resonator loops to create local zeros in the transfer function.

In this single-stage dual-loop modulator architecture, shown in Fig. 5, the clock driving the D-latch array has opposite phase to the clock driving the quantizer and the DFF array synchronizing DAC-A. The D-latch array effectively adds a half clock cycle in front of DAC-A and DAC-B, thus there is now one digital delay between the quantizer output and the DAC-A input, giving the quantizer a full clock period to settle without adding any extra loop delay. The DFF array should be omitted when half-period delay compensation is used (shown in Fig.5b.). During this fifth step, gains and coefficients are computed by equating the general parametric equation of the system with the one which is calculated during the first four steps, $H'(s)$. Since there are 10 variables and 6 equations in the design example of our 4th-order modulator, the designer should assign some initial values to four of them, e.g. $\hat{c}_1, \hat{c}_2, \hat{c}_3, \hat{c}_4$, and then solve for the others. In our example these coefficients are set to be one initially. Of course the designer has the freedom to choose other coefficients in the design tool or modify them afterwards.

D. Transient simulation and coefficient scaling

Finally, the last step in the design methodology, which is very important, is devoted to transient and system-level simulations in order to test essential issues such as the required gain-bandwidth of the integrators which directly influences the power consumption, the output swing of the integrators which should be scaled according to the used technology and the required linearity, the amplitude of the quantizer input signal to prevent its saturation, the coefficient spread, the robust performance and robust stability against probable mismatch between the ideal gains and their values during actual implementation. Because of the above considerations, some iterations may be needed between this step and the former to find the final best coefficients.

In our example, the initial coefficients were calculated by setting all the coefficients of the integrators $\hat{c}_1, \hat{c}_2, \hat{c}_3, \hat{c}_4$ to one. This method doesn't take into account the output signal level of each integrator, so it is quite likely that one of the integrators will be saturated in a real implementation if the output voltage level becomes too large. On the other hand, the distortion contribution

TABLE I
INITIAL AND FINAL COEFFICIENTS

	\hat{c}_1	\hat{c}_2	\hat{c}_3	\hat{c}_4	\hat{f}_1	\hat{f}_2	\hat{f}_3	\hat{f}_4	\hat{g}_1	\hat{g}_2	\hat{a}_2	$1+\hat{b}_2$
before scaling	1	1	1	1	2.43	1.94	1.15	0.27	0.114	0.0178	0.99	1.99
after scaling	1.45	1.06	1.05	0.432	1.67	1.25	0.71	0.38	0.0741	0.0391	0.99	1.99

from the output stage becomes a major factor as the output swing of the integrator is very large. To solve both issues, a scaling method [14] is used here to guarantee a reasonable signal swing at each integrator output. The idea of this method can be divided into two steps. First, the gain of each integrator can be divided by a factor d_i given by :

$$d_i = \frac{V_{out_i,max}}{V_{out_i,desired}} \quad (12)$$

to scale the output swing to the desired value (which is 1/4 of the reference voltage in our example). Secondly, the d_i are distributed in such a way that the open-loop filter function is preserved, which means that there is no d_i in the final open-loop transfer function. Since the scaling process does not change the continuous-time loop transfer function, the feedback coefficient of the internal loop (which compensates the ELD) stays the same after scaling. Likewise, since both the NTF and the internal loop gain do not change, there is no need to change the gain of the direct path (from the signal input to the quantizer) during scaling. Table II shows the initial and final coefficients before and after the above scaling for our example. Fig. 6 also shows the output swing of the integrators before and after the scaling. It can be seen from Fig. 6 that initially the output swing of the fourth integrator is beyond the desired value, while the output swings of the other integrators fulfill the requirement. After scaling, the output swings of the first three integrators increase a bit while the fourth one decreases to around 1/4 of the reference voltage. This guarantees the overall linearity and reduces the power consumption of the first 3 integrators.

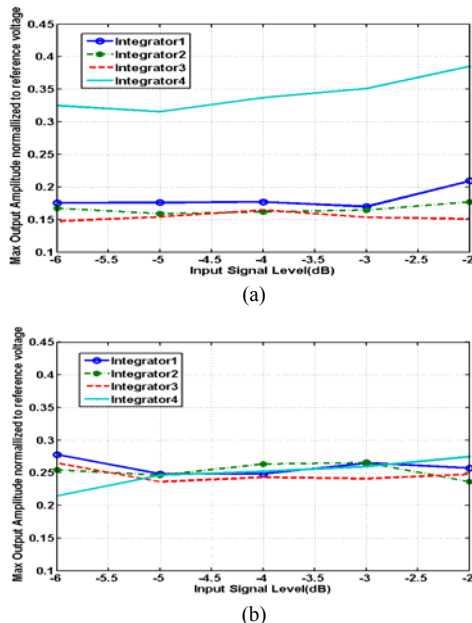


Fig. 6. Integrator output swing before scaling (a) and after scaling (b).

III. SIMULATION RESULTS

In order to verify the validity of the proposed design methodology of high-order multi-bit CT DSMs, MATLAB simulations have been performed for the illustrative example design. All of the simulations are verified on the described CT DSM of section II and the results are summarized in this section. In all of the simulations, a 16384-point FFT is used to calculate the SNR. The OSR of the modulator is 8 while the sampling frequency is set at 320 MHz. Also, the Hanning window is utilized for the SNR calculations. From Fig. 7 it can be seen that the required GBW for the first integrator, the most power-critical one, is less than 1.5 times the sampling frequency which is much lower compared to [4] (only the corresponding integrator is set to finite GBW), while for the other integrators half of the sampling frequency is enough. Hence, power can be further

saved for the other stages. This minimizes the overall power consumption of the designed CT modulator.

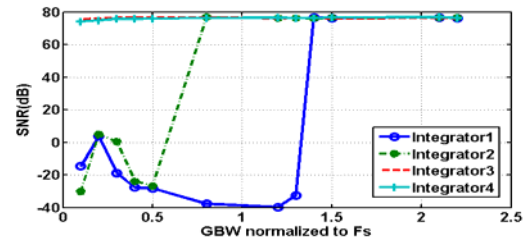


Fig. 7. SNR vs. GBW of the different integrators.

IV. CONCLUSIONS

In this paper a systematic design methodology for high-order multi-bit continuous-time Delta-Sigma modulators has been proposed. The strategy is to design the modulator in the z-domain and then to convert the modulator to the s-domain. The validity of the proposed design methodology has been shown through the design example of a 4th-order 4-bit CT DSM for an application with a 20 MHz signal bandwidth and 12 bit resolution. Simulations confirm the validity of the design approach. This design methodology results in a much lower power consumption compared to other published solutions.

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