has done research in graph theory and network analysis and synthesis.

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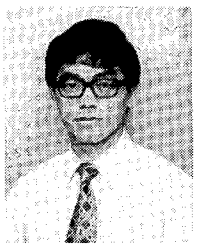

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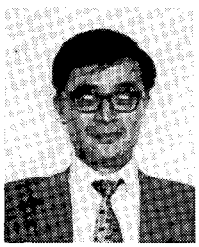

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Optimal Design of Nonlinear DC Transistor Circuits Without Solving Network Equations

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Abstract—**A method is described for the optimization of nonlinear dc circuits. A performance index is defined to measure the difference between the desired and the actual specifications. The novel approach taken here is to treat the network equations as equality constraints on the design parameters. The constrained optimization problem is then converted to an unconstrained one by a penalty function technique. A straightforward method is given for computing all the gradients needed during the optimization, given only the topology of the network and the branch relationships. This makes the algorithm easily amenable to a package program.**

I. Introduction

RECENTLY, methods have been given for the computer-aided design of several types of nonlinear dc circuits [1]–[4]. A great deal of the computation time for such a design is spent on the nonlinear circuit analyses [6], making any design algorithm efficiency dependent on the efficiency of the analysis algorithm.

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In this paper a method is proposed for nonlinear dc optimization without solving network equations. This is achieved by treating the network equations as equality constraints on the parameters. A penalty function is defined to transform the constrained problem into a sequential unconstrained problem [7], [8], which is then solved by an algorithm due to Morrison [7], with an improvement proposed by Kowalik *et al.* [8]. This particular algorithm is found to be the most suitable one for the present problem.

II. Problem Formulation

Performance Index

Given a design specification in terms of the various voltages and currents appearing in the circuit, an error term is associated with each of them. Such a term measures the difference between the actual and the desired values. The overall performance index may be written as

$$f = \sum_{i=1}^{N_V} [W_{V_i}(V_i - \hat{V}_i)]^2 + \sum_{j=1}^{N_I} [W_{I_j}(I_j - \hat{I}_j)]^2 \quad (1)$$

where V_i, I_j are the actual voltages and currents, and $\hat{V}_i$, $\hat{I}_j$ are the corresponding specified values; N_V, N_I are the

number of voltage and current specifications, respectively, while W_{V_i}, W_{I_j} are the positive scaling parameters. If $\hat{V}_j \neq 0$, the parameter W_{V_i} is chosen as $W_{V_i} = \hat{W}_{V_i}/|\hat{V}_i|$ where $\hat{W}_{V_i}$ is another scaling parameter. This has the effect of normalizing the corresponding error term in (1). Similar considerations apply to W_{I_j}. Let the network equations be defined by $\boldsymbol{g} = \mathbf{0}$. Then the optimization problem can be stated as: minimize f subject to the constraint $\boldsymbol{g} = 0$.

A set of transistor parameters and source excitation values may be called an "environmental condition." The performance function of (1) yields a design under a nominal environmental condition; however, it can easily be extended to include several such conditions simultaneously such that the bias point fluctuation is minimized (worst case design). A performance function like (1) is then defined for each environmental condition, and the overall performance function is the algebraic sum of all such functions. To minimize power dissipation, terms of the type $W_p I_p V_p$ are added to f in (1) for each power supply, where W_p is a weighting factor used to have a tradeoff between the accuracy of specified voltage and current, and the power consumption.

DC Transistor Model

For the formulation of nodal equations the Ebers–Moll transistor model [6] replaces the transistors. Such a model for an n-p-n transistor is shown in Fig. 1.

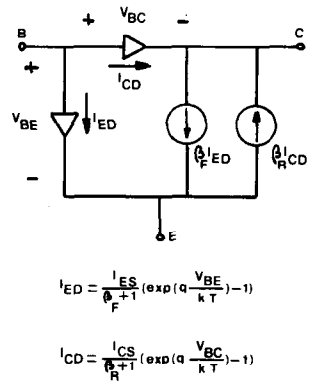

Fig. 1. Ebers–Moll model for n-p-n transistor.

III. Modified Morrison's Algorithm

The original problem is converted to an unconstrained problem by replacing the constraints by a penalty function, as follows. Define

$$F_i(\boldsymbol{x}) = [f(\boldsymbol{x}) - M_i]^2 + \sum_j k_j[g_j(\boldsymbol{x})]^2, \qquad \text{where } k_j \geq 0. \tag{2}$$

The algorithm below is given in [8].

a) Start with an estimate M_1 with $f(\bar{\boldsymbol{x}})$, the optimum value of f, $\geq M_1$, i.e., start with an optimistic guess for M_1. Let $i = 1$.

b) Minimize $F_i(\boldsymbol{x})$, and let $\boldsymbol{x}_i$ be the resulting solution. Define

$$F_{i0} = [f(\boldsymbol{x}_i) - M_i]^2 + \sum_j k_j[g_j(\boldsymbol{x}_i)]^2.$$

c) Let

$$M_{i+1} = M_i + F_{i0}{}^{1/2}. \tag{3}$$

d) If $M_{i+1} = M_i$, stop. Otherwise go back to b), with $i \leftarrow i + 1$. The basis for the algorithm is that if M_1 is an optimistic guess, then M_i is an optimistic guess for all i, and M_i's converge monotonically to $f(\bar{\boldsymbol{x}})$ under some mild conditions on f and $\boldsymbol{g}$.

Calling M as the Morrison parameter, Kowalik *et al.* [9] have given an improved scheme for updating the parameter. It is given by

$$N_{i+1} = N_i + F_i \Big/ \left(F_i - \sum_j k_j g_j{}^2\right)^{1/2} \tag{4}$$

where N is the new Morrison parameter. Comparing (4) with (3) it may be seen that $N_i \geq M_i$ for all i, so that the N_i's converge faster than M_i's. Since f as defined in (1) is always nonnegative, any negative number may be chosen as the initial guess for N.

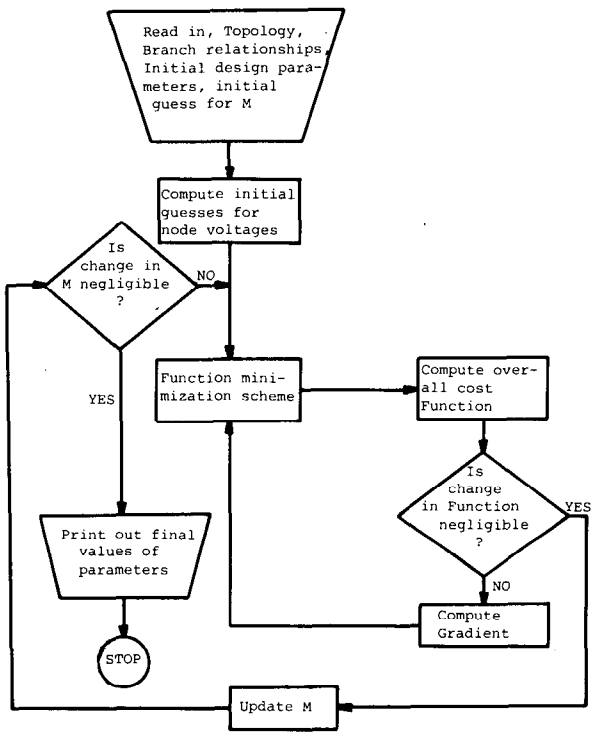

Fig. 2. Flowchart of design algorithm.

In case of dc design of transistor circuits, $\boldsymbol{g}(\boldsymbol{x})$ is taken to be the set of network equations while f is the performance index. The penalty augmented function is thus given by

$$F = (f - N)^2 + k \sum_i g_i{}^2 \tag{5}$$

where k is a scaling factor.

Flow Chart of the Algorithm

A flow chart based on Morrison's algorithm applicable to our design problem is given in Fig. 2.

IV. Computation of Gradients

Let $\boldsymbol{x}$ be a vector of the design parameters. Differentiating the penalty augmented function F in (4) with respect to $\boldsymbol{x}$,

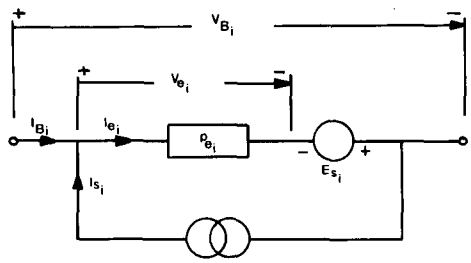

Fig. 3. Generalized ith branch.

we have

$$\frac{\partial F}{\partial \boldsymbol{x}} \triangleq \nabla F$$

$$= 2(f - M)\frac{\partial f}{\partial \boldsymbol{x}} + 2k\left(\frac{\partial \boldsymbol{g}}{\partial \boldsymbol{x}}\right)^T \boldsymbol{g} \tag{6}$$

where, from (1)

$$\frac{\partial f}{\partial \boldsymbol{x}} = 2\sum_{i=1}^{N_V} W_{V_i}(V_i - \hat{V}_i)\frac{\partial V}{\partial \boldsymbol{x}} + 2\sum_{j=1}^{N_I} W_{I_j}(I_j - \hat{I}_j)\frac{\partial I_j}{\partial \boldsymbol{x}}. \tag{7}$$

Computation of $\partial f/\partial \boldsymbol{x}$ in (7) involves the computation of $\partial V_i/\partial \boldsymbol{x}$ and $\partial I_j/\partial \boldsymbol{x}$ which is straightforward and is therefore not described here. To derive $\partial \boldsymbol{g}/\partial \boldsymbol{x}$ in (6) we proceed as follows.

Without any loss of generality all the controlled sources in a linear lumped network can be assumed to be voltage controlled current sources. Assuming a generalized ith branch to be as shown in Fig. 3, the different branch parameters for the whole network may be expressed in vector form as follows:

$\boldsymbol{p}_e \rightarrow$ branch element "parameter" vector
$\boldsymbol{V}_e \rightarrow$ element voltage vector
$\boldsymbol{I}_e \rightarrow$ element current vector
$\boldsymbol{E}_s \rightarrow$ voltage source vector
$\boldsymbol{I}_s \rightarrow$ current source vector
$\boldsymbol{I}_B \rightarrow$ branch current vector
$\boldsymbol{V}_B \rightarrow$ branch voltage vector.

$\boldsymbol{I}_e$, $\boldsymbol{E}_s$, and $\boldsymbol{I}_s$ may now be expressed as functions of $\boldsymbol{V}_e$ and $\boldsymbol{p}_e$ as $\boldsymbol{I}_e = f_1(\boldsymbol{V}_e,\boldsymbol{p}_e)$, $\boldsymbol{E}_s = f_2(\boldsymbol{V}_e,\boldsymbol{p}_e)$, and $\boldsymbol{I}_s = f_3(\boldsymbol{V}_e,\boldsymbol{p}_e)$. From Fig. 3, $\boldsymbol{I}_B = \boldsymbol{I}_e - \boldsymbol{I}_s = f_4(\boldsymbol{V}_e,\boldsymbol{p}_e)$, and Kirchhoff's current law (KCL) yields $\boldsymbol{A}\boldsymbol{I}_B \triangleq \boldsymbol{g} = \boldsymbol{0}$.

Gradient with Respect to the Node Voltages

The penalty term is given by

$$\sum_j g_j^2 = \boldsymbol{g}^T\boldsymbol{g}$$

$$\triangleq P.$$

Denoting the node voltage vector by $\boldsymbol{V}_n$, Kirchhoff's voltage law (KVL) yields, $\boldsymbol{V}_B = \boldsymbol{A}^T\boldsymbol{V}_n$. However, $\boldsymbol{V}_e = \boldsymbol{V}_B + \boldsymbol{E}_s = \boldsymbol{A}^T\boldsymbol{V}_n + \boldsymbol{E}_s$, and hence $\boldsymbol{g} = \boldsymbol{A}f_4(\boldsymbol{A}^T\boldsymbol{V}_n + \boldsymbol{E}_s,\boldsymbol{p}_e)$. Differentiating P with respect to $\boldsymbol{V}_n$, we have

$$\frac{\partial P}{\partial \boldsymbol{V}_n} = 2\boldsymbol{A}\left[\frac{\partial f_4(\boldsymbol{V}_e,\boldsymbol{p}_e)}{\partial \boldsymbol{V}_e}\right]^T_{\boldsymbol{V}_e = \boldsymbol{A}^T\boldsymbol{V}_n + \boldsymbol{E}}\left(\boldsymbol{A}^T + \frac{\partial \boldsymbol{E}_s}{\partial \boldsymbol{V}_n}\boldsymbol{g}\right). \tag{8}$$

In case of each branch current source and each branch voltage source being controlled by a single parameter or a single voltage source, (8) can be considerably simplified. Specifically, suppose the sources in the ith branch depend only on V_{e_j} and p_{e_j}. Then I_{e_i}, E_i, and I_i can be expressed as, $I_{e_i} = f_1(V_{e_j},p_{e_j})$, $I_i = f_2(V_{e_j},p_{e_j})$, and $I_i = f_3(V_{e_j},p_{e_j})$. Note that this situation prevails in the dc transistor model in Fig. 1. Furthermore, $\partial \boldsymbol{E}_s/\partial \boldsymbol{V}_n = \boldsymbol{0}$, and (8) becomes

$$\frac{\partial P}{\partial \boldsymbol{V}_n} = 2\boldsymbol{A}\boldsymbol{J}^T\boldsymbol{A}^T\boldsymbol{g} \tag{9}$$

where the Jacobian $\boldsymbol{J}$ is given by

$$\boldsymbol{J} = \left.\frac{\partial f_4(\boldsymbol{V}_e,\boldsymbol{p}_e)}{\partial \boldsymbol{V}_e}\right|_{\boldsymbol{V}_e = \boldsymbol{A}^T\boldsymbol{V}_n + \boldsymbol{E}_s}. \tag{10}$$

Thus the Jacobian is the same as the branch admittance matrix of a transistor ac equivalent circuit, where the diodes are replaced by equivalent conductances given by

$$G_j = \frac{I_s q}{kT}\exp\left(\frac{q}{kT}V_{e_j}\right).$$

Denoting the branch conductance matrix by $\boldsymbol{Y}_B$, $\partial P/\partial \boldsymbol{V}_n = 2\boldsymbol{A}\boldsymbol{Y}_B{}^T\boldsymbol{A}^T\boldsymbol{g} = 2Y^T\boldsymbol{g}$, where $\boldsymbol{Y}$ is the nodal admittance matrix of the new network. Note that $\boldsymbol{Y}_a = \boldsymbol{Y}^T$, where $\boldsymbol{Y}_a$ is the nodal admittance matrix of the linearized adjoint network [5].

Gradients with Respect to the Design Parameters

Differentiating (1) with respect to $\boldsymbol{p}_e$, we have

$$\frac{\partial \boldsymbol{g}}{\partial \boldsymbol{p}_e} = \boldsymbol{A}\left.\frac{\partial f_4(\boldsymbol{V}_e,\boldsymbol{p}_e)}{\partial \boldsymbol{p}_e}\right|_{\boldsymbol{V}_e = \boldsymbol{A}^T\boldsymbol{V}_n + \boldsymbol{E}_s}. \tag{11}$$

However, when the design parameters are lumped conductances, f_4 becomes $f_4(\boldsymbol{V}_e,\boldsymbol{Y}_e)$ and (11) may be simplified as follows.

Let the incidence matrix $\boldsymbol{A}$ be partitioned as $\boldsymbol{A} = [\boldsymbol{A}_1 \mid \boldsymbol{A}_2]$, where the columns of $\boldsymbol{A}_1$ correspond to the conductances to be optimized, and those of $\boldsymbol{A}_2$ to the remaining branches. Accordingly, the linearized branch admittance matrix $\boldsymbol{Y}_b$ is partitioned as

$$\boldsymbol{Y}_b = \begin{bmatrix} \boldsymbol{Y}_{b_{11}} & \boldsymbol{Y}_{b_{12}} \\ \boldsymbol{Y}_{b_{21}} & \boldsymbol{Y}_{b_{22}} \end{bmatrix}$$

where $\boldsymbol{Y}_{b_{11}}$ is diagonal. Therefore,

$$\frac{\partial P}{\partial \boldsymbol{p}_e} = 2\frac{\partial}{\partial \boldsymbol{Y}_e}\{\boldsymbol{A}_1\boldsymbol{Y}_{b_{11}}(\boldsymbol{A}_1{}^T\boldsymbol{V}_n + \boldsymbol{E}_s)\}^T\boldsymbol{g}. \tag{12}$$

Gradient with Respect to an Independent Voltage Source

Let

$$\frac{\partial P}{\partial \boldsymbol{E}_s} = 2\boldsymbol{A}\left.\frac{\partial f_4(\boldsymbol{V}_e,\boldsymbol{Y}_e)}{\partial \boldsymbol{E}_s}\right|_{\boldsymbol{V}_e = \boldsymbol{A}^T\boldsymbol{V}_n + \boldsymbol{E}_s}\cdot \boldsymbol{g}$$

$$= 2\boldsymbol{A}\boldsymbol{J}_1\boldsymbol{g} \tag{13}$$

where the Jacobian $\boldsymbol{J}_1$ is the branch admittance matrix of the branches involving the independent voltage sources as parameters, with the other admittances set to zero.

TABLE I

Parameters	Initial values				Final Values
	[illegible]	Run 2	Run 3	Run 4	
G_1	[illegible]$\times10^{-3}$	0.1×10^{-3}	0.1×10^{-3}	0.1×10^{-3}	0.218×10^{-3}
G_2	[illegible]$\times10^{-3}$	0.1×10^{-3}	0.1×10^{-3}	0.1×10^{-3}	0.218×10^{-3}
G_3	[illegible]$\times10^{-3}$	0.1×10^{-3}	0.1×10^{-3}	0.1×10^{-3}	0.666×10^{-3}
G_4	[illegible]$\times10^{-3}$	0.1×10^{-3}	0.1×10^{-3}	0.1×10^{-3}	0.625×10^{-3}
G_5	[illegible]	0.1	0.1	0.1	0.578×10^{-1}
V_1	[illegible]	15.5	15.5	15.5	15.659
V_2	[illegible]	-0.5	-0.5	-0.5	-0.640
V_3	[illegible]	-17.5	-17.5	-17.5	-17.323
V_4	[illegible]	-17.6	-17.6	-17.8	-17.982
V_5	[illegible]	15.0	15.0	15.0	15.0
V_6	[illegible]	15.5	15.5	15.5	15.659
V_7	[illegible]	16.5	16.5	16.5	16.5
CPU Time	[illegible]	4.2 s	4.7 s	3.5 s	
No. of Fletcher-Powell iterations	[illegible]	39	44	33	

TABLE II

Parameters	Initial values			Final Values
	Run 1	Run 2	Run 3	
G_1	$.1\times10^{-3}$	$.1\times10^{-4}$	$.1\times10^{-4}$	$.949\times10^{-5}$
G_2	$.1\times10^{-3}$	$.1\times10^{-4}$	$.1\times10^{-3}$	$.706\times10^{-4}$
G_3	$.1\times10^{-3}$	$.1\times10^{-3}$	$.1\times10^{-3}$	$.184\times10^{-3}$
$v_1^{(1)}$	1.1	1.5	1.0	1.08
$v_2^{(1)}$	5.6	6.0	5.5	5.43
$v_3^{(1)}$	0.6	1.0	1.0	0.42
$v_1^{(2)}$	1.1	1.0	1.0	0.76
$v_2^{(2)}$	5.6	6.0	5.5	5.43
$v_3^{(2)}$	0.6	1.0	1.0	0.44
CPU Time	2.4 s	2.8 s	2.6 s	
No. of Fletcher-Powell iterations	44	50	47	

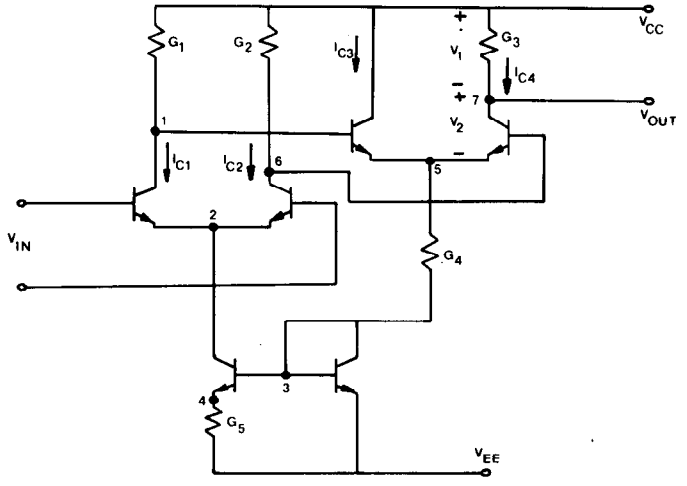

Fig. 4. Two-stage operational amplifier example.

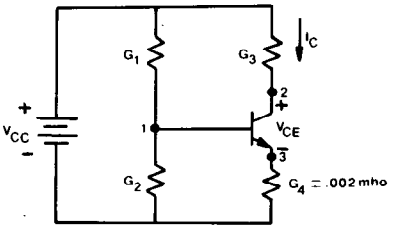

Fig. 5. One transistor biasing circuit example.

V. Examples

Due to shortage of space only two examples are presented to illustrate the effectiveness of the approach, which are taken from [1]. It is found that the convergence to the desired optimum occurs readily if the initial node voltage values are chosen in the neighborhood of the feasible region. To do this the transistors are replaced by a model without the collector-to-base diode and the corresponding current source in Fig. 1. Whenever a voltage between two nodes is given as a design specification, a voltage source equal to the specified value is connected between the nodes. For each collector current specification, the base-to-emitter diode is replaced by a voltage source equivalent to the voltage drop in the diode. The other diodes in the circuit are replaced by voltage sources of magnitudes in the feasible range (say, $0V \leq V_{be} \leq 0.6$ V), taking care that the KVL is also satisfied. The resultant modified network which may be termed the "modified network," is then analysed and the node voltages thus obtained are taken as the initial node voltage values for the algorithm. The examples are run on a CDC 6400 computer available, using the optimization algorithm due to Fletcher and Powell [9] as in [1]. The termination criterion is $N_{i+1} - N_i \leq 10^{-15}$.

Example 1—Gain Stages for Operational Amplifier

The circuit is shown in Fig. 4. The adjustable parameters are the five conductances G_1 to G_5. The bias point specifications are as follows: $I_{c_1} = 0.5$ mA, $I_{c_2} = 0.5$ mA, $I_{c_3} = 1.0$ mA, $I_{c_4} = 1.0$ mA, $E_1 = 1.5$ V, and $E_2 = 1.5$ V. The final results are shown in Table I. In Run 1 the initial guesses for the node voltages are found by analyzing the modified network; while in Runs 2 to 4 the initial values are varied slightly from that in Run 1. In all the runs the network equations are satisfied to the order of 10^{-18}.

Example 2—Single Transistor Stage: Two Environmental Conditions

The circuit to be designed is shown in Fig. 5. It is desired to have minimum deviation in the bias point at two environmental conditions, while minimizing power dissipation. The desired operating point is: $I_c = 1$ mA, and $V_{c_E} = 5$ V; with the designable conductances being G_1 to G_3. The transistor

parameters at the two environmental conditions are as follows. Condition 1: $\beta_F = 25$; condition 2: $\beta_F = 100$; while $\beta_R = 5$, $I_{C_S} = 10^{-14}$ A, and $I_{E_S} = 10^{-14}$ A for both conditions. The results are shown in Table II where the superscripts denote the environmental conditions. The network equations are satisfied to the order of 10^{-18}. The specified voltages and currents are realized as follows:

$$V_{c_E}^{(1)} - 5 = 0.95 \times 10^{-2}$$
$$V_{c_E}^{(2)} - 5 = -0.25 \times 10^{-2}$$
$$I_c^{(1)} - 1 = 0.62 \times 10^{-6}$$
$$I_c^{(2)} - 1 = 0.61 \times 10^{-6}.$$

The power dissipations are 0.926 mW and 0.928 mW at the two operating points. The final values of the modified Morrison's parameter N is of the order of 10^{-5}.

VI. Discussion

It has been found by the authors that if the initial guess for the node voltage values are in the neighborhood of the ones obtained by analyzing the modified network as mentioned in Section 5, convergence is fast. Justification for the final design is based on the fact that the design specifications are realized as the vector $g(x)$ of the KCL equations becomes zero. However, in reality it is a vector of very small numbers. Since the various currents in the circuits are of the order of milliamperes, to make the second term in (5) of the same order as the first term $(f - M)^2$, one should normalize the KCL equations with respect to the Euclidean norm of the current vector.

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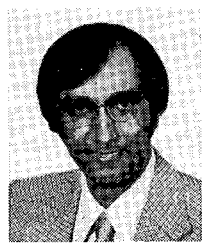

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