Optimal Design of the Active Droop Control Method for the Transient Response

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***Abstract*— Use of the Active droop control method is a popular way to achieve adaptive voltage position (AVP) for the voltage regulator (VR). This paper discusses the small-signal model of the active droop control method, which is shown to be a two-loop feedback control system. The compensator design impacts both the current and voltage loops, making the design complicated. An optimal design method is proposed in order to achieve equal crossover frequencies for the two loops so that constant output impedance is realized in the VR. Simulation and experimental results prove the good VR transient response and high efficiency.**

Keywords-active droop control; transient response; VR; VRM

I. INTRODUCTION

Due to the fast development of the microprocessor, it has become necessary to use a special voltage regulator (VR) for power management. Intel's road map shows that the VR for the microprocessor is a very fast-moving target. It must support less than 1 V of output voltage with tight regulation, and more than 100 A of current with a high dynamic slew rate [1]. These requirements pose a stringent challenge to the VR voltage regulation, especially in the transient response. The use of many output capacitors to reduce the voltage spike during the transient is an approach that has been taken. However, for future microprocessors, increasing the capacitors' numbers to meet the even higher transient requirement will no longer be acceptable because of size and cost issues.

One way to alleviate this problem is based on the adaptive voltage position (AVP) control [2-5]. The basic idea is to control the output voltage level so that it is slightly higher than the minimum value at full load and slightly lower than the maximum value at light load. As a result, the entire voltage tolerance window can be used for the voltage jump or drop during the transient. Compared with the conventional constant-output voltage feedback control, AVP control can halve the number of output capacitors needed to meet the same transient requirement. A side benefit of the AVP control is that the VR output power at full load is reduced, which greatly facilitates the thermal design. Furthermore, with the AVP design it is very easy for the VR output to meet the load-line specification [4,5].

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Current mode controls with finite DC gain for the compensator have been reported to achieve AVP [6-9]. The finite DC gain introduces a steady-state output voltage error, which is small in light loads and large in heavy loads. As a result, the AVP design depends on the accuracy of the DC gain. A DC gain that is too small will introduce a greater output voltage error, but a DC gain that is too large cannot take advantage of the entire voltage tolerance window for the transient. Fig. 1 shows these limitations clearly.

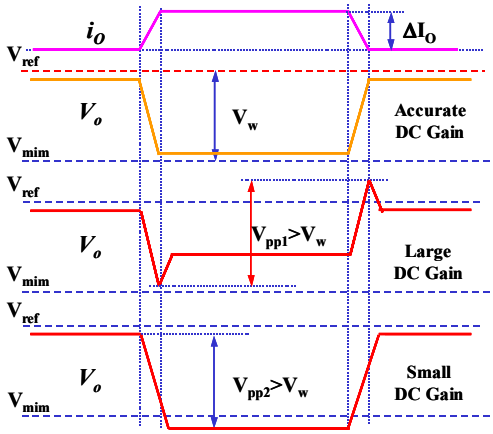

Figure 1. The limitations of the finite DC gain to achieve AVP.

As a result, the active droop control method is proposed to solve these problems by using an infinite DC gain design for the feedback compensator [10-11]. From the standpoint of the output characteristics of the VR, the AVP control is comparable to introducing a droop function. Droop control has been widely discussed in applications involving current sharing between multi-power supplies [12-13]. However, there are few reports about its transient performance. Although Intersil, Fairchild and some other IC manufacturers have already developed control ICs for VRs based on the droop control idea, there is no design guideline for the feedback compensator and good transient response cannot be achieved. This paper clarifies all these issues. Section II explains the idea of the active droop control method. The small-signal model in Section III shows the design considerations. Section IV proposes an optimal design method to achieve perfect AVP. Finally, the simulation and experimental results in Section V prove all the theoretical analyses.

II. ACTIVE DROOP CONTROL

Fig. 2 shows the basic idea of the active droop control method. The inductor current information is sensed and fed back to adjust the output voltage reference according to the droop requirement. Larger current means smaller voltage reference. Then, the feedback control forces the output voltage to follow the voltage reference. The infinite DC gain of the feedback compensator ensures that the values of the output voltage and the voltage reference are equal. Since the output voltage droop is related to the output load current, it can be controlled perfectly. Fig. 3 shows the key operation waveforms of the active droop control method.

However, the output voltage waveforms during the t_1 and t_2 transient periods in Fig. 3 are not clear. The inductor current feedback loop determines the dynamic performance of the voltage reference. The voltage feedback loop determines the dynamic performance of the output voltage. Potentially, these two loops may conflict with each other, causing either transient voltage spikes or an unstable system.

As a result, finding the best way to design the current and voltage loops is a big issue for the active droop control method. Without a good design, voltage spikes and ringing can still occur in the VR transient response [10]. In the next section, a small-signal model is proposed for more detailed analysis.

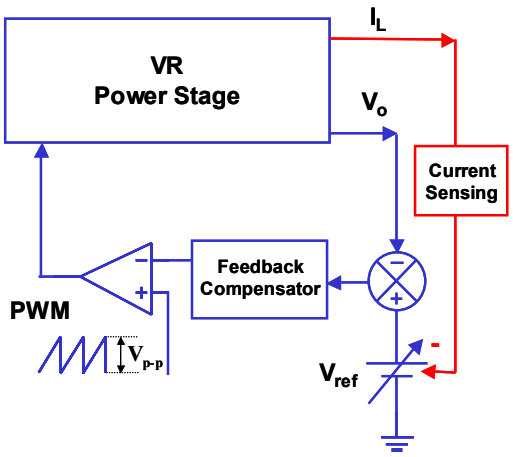

Figure 2. The active droop control method.

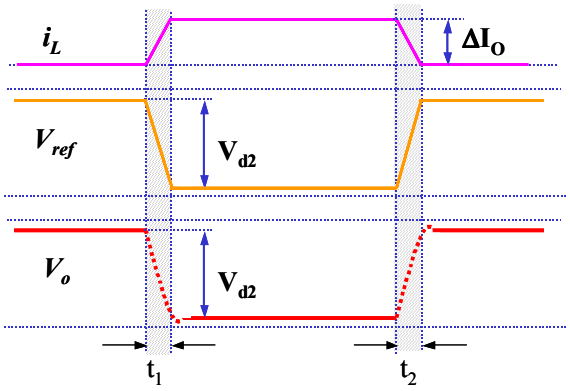

Figure 3. The key operation waveforms of active droop control.

III. SMALL-SIGNAL MODEL ANALYSIS

The multiphase buck converter is widely used for the VR design. Some small-signal modeling work [14] shows that the multiphase interleaving makes no difference in the small-signal model because of the average effect. As a result, a simple single-phase buck converter can be used for the small-signal analysis. Fig. 4 shows all the parameters in a single-phase buck converter with the active droop control. L_o is the equivalent output inductance of the multiphase inductors in parallel. R_L includes the DC resistance of the inductor L_o, the conduction resistance $R_{ds\text{-}on}$ of the MOSFETs, and the parasitic resistance of the traces. R_{i1} is the inductor current sensing gain. R_o represents the microprocessor load. R_C is the equivalent series resistance (ESR) of the output capacitor C_o. The equivalent series inductor (ESL) of the output capacitor is ignored here since the high-frequency ceramic capacitors in parallel greatly reduce its effect.

Fig. 5 shows the small-signal block of a buck converter with the active droop control method based on the multi-loop analysis method [15]. Z_o is the power stage open-loop output impedance. G_{vd} is the transfer function of output voltage V_o to duty cycle d. G_{ii} is the transfer function of inductor current i_L to load current i_o. G_{id} is the transfer function of inductor current to duty cycle. A_v is the feedback compensator transfer function. And F_m represents the pulse width modulation (PWM) comparator effect.

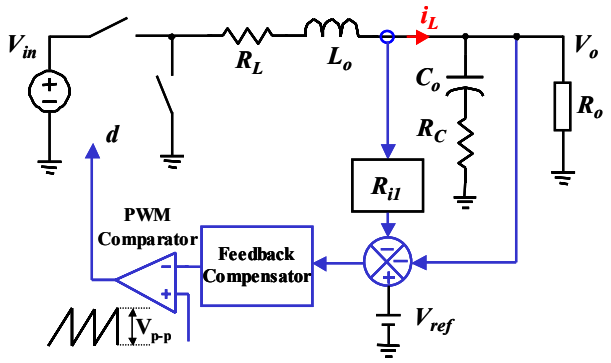

Figure 4. The single-phase buck converter with the active droop control.

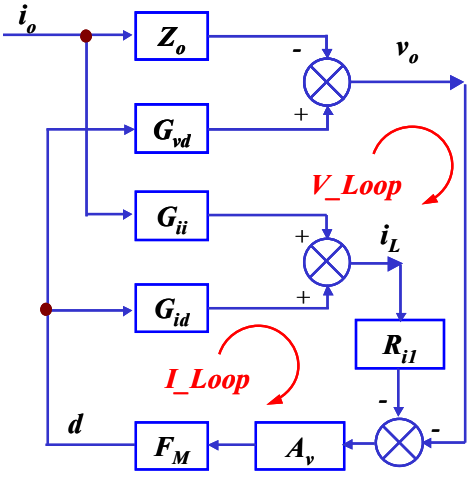

Figure 5. The small-signal block of the active droop control.

$$Z_o(s) = R_L \cdot \frac{(1+s/\omega_C)\cdot(1+s/\omega_L)}{1+s/(Q\cdot\omega_o)+s^2/\omega_o^2} \quad (1)$$

$$G_{vd}(s) = V_{in} \cdot \frac{1+s/\omega_C}{1+s/(Q\cdot\omega_o)+s^2/\omega_o^2} \quad (2)$$

$$G_{ii}(s) = \frac{1+s/\omega_C}{1+s/(Q\cdot\omega_o)+s^2/\omega_o^2} \quad (3)$$

$$G_{id}(s) = \frac{V_{in}}{R_o} \cdot \frac{1+s/\omega_R}{1+s/(Q\cdot\omega_o)+s^2/\omega_o^2} \quad (4)$$

$$F_M = \frac{1}{V_{p-p}} \quad (5)$$

$$\omega_o \approx \frac{1}{\sqrt{C_o \cdot L_o}} \quad (6)$$

$$Q \approx \frac{\sqrt{L_o/C_o}}{R_L + ESR_C} \quad (7)$$

$$\omega_C = \frac{1}{R_C \cdot C_o} \quad (8)$$

$$\omega_L = \frac{L_o}{R_L} \quad (9)$$

$$\omega_R = \frac{1}{R_o \cdot C_o} \quad (10)$$

From Fig. 5, it is very clear that the active droop control is a two-loop feedback system. The current loop T_i and voltage loop T_v are defined as:

$$T_i = A_v \cdot F_M \cdot G_{id} \cdot R_{i1}, \text{ and} \quad (11)$$

$$T_v = A_v \cdot F_M \cdot G_{vd}. \quad (12)$$

Figs. 6 and 7 show a current mode controlled buck converter and its small-signal block. R_{i2} is the inductor current sensing gain. G_{ci} is the current loop compensator transfer function, and G_{cv} is the voltage loop compensator transfer function.

The comparison between Figs. 5 and 7 shows that the active droop control is very similar to current mode control. When

$$G_{cv} = \frac{R_{i2}}{R_{i1}} \text{ and} \quad (13)$$

$$A_v = \frac{R_{i2}}{R_{i1}} \cdot G_{ci}, \quad (14)$$

these two small-signal blocks are equivalent. The active droop control is just a special example of the current mode control with a constant voltage compensator gain as shown in (13). As a result, the design for the active droop control must have something similar to that of the current mode control. However, there is a significant difference between these two control methods. In the current mode control, the current loop is inside of the voltage loop. The voltage loop compensator needs a finite DC gain to achieve AVP control, and the designs of G_{ci} and G_{cv} can be separated. But in the active droop control, the information about both current and voltage is fed back and then the two values are added together. As a result, it is also referred to as summing mode control [16]. The compensator design of A_v influences both the current and voltage loops and requires an infinite DC gain. As a result, the design for the active droop control is relatively more complex. The next section will discuss the design in detail.

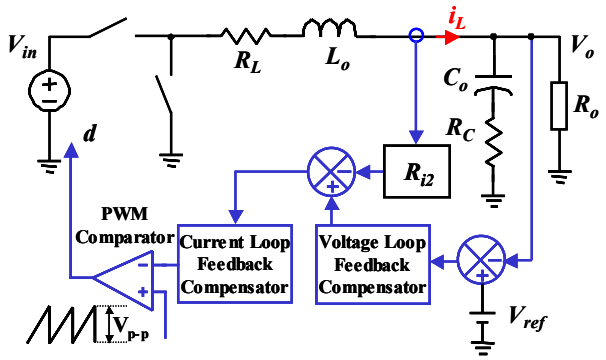

Figure 6. The single-phase buck converter with the current mode control.

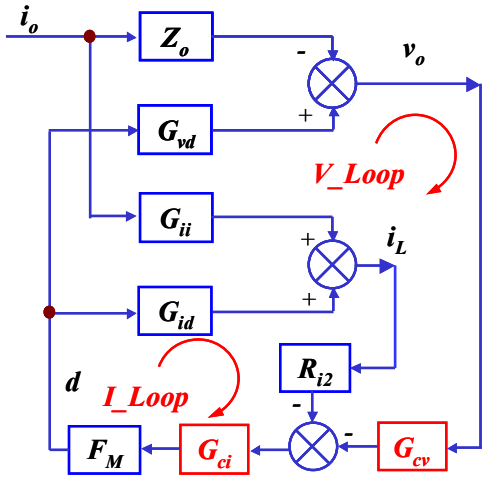

Figure 7. The small-signal block of the current mode control.

IV. Design for Active Droop Control

In Fig. 5, the current loop determines the dynamic performance of the voltage reference, and the voltage loop forces the output voltage to follow the voltage reference. As a result, the voltage loop must be fast enough to follow the change of the voltage reference. A voltage loop that is too slow will cause transient voltage spikes and ringing. However, a voltage loop that is too fast may cause system stability problems. As a trade off, if the current and voltage loops have the same dynamic characteristics, these two loops will not fight each other and perfect AVP can be achieved.

Since the loop-crossover frequency determines the dynamic performance, the two loops need to be designed to have the same crossover frequency. Because the compensator design for A_v impacts both the current and voltage loops, it does not

contribute to the difference between the two loops. Equations (11) and (12) show this point clearly. Thus, only the current sensing gain R_{i1} determines if the two loops can have the same crossover frequency. The ratio T_v/T_i represents the difference between these two loops:

$$\frac{T_v}{T_i}=\frac{G_{vd}}{R_{i1}\cdot G_{id}}=\frac{R_o\cdot(1+s/\omega_C)}{R_{i1}\cdot(1+s/\omega_R)}. \tag{15}$$

Normally, the output capacitor ESR zero ω_C is much larger than ω_R.

When $\omega>\omega_C$ and $R_{i1}=R_c$, (15) equals 1, which means that the current and voltage loops have the same crossover frequency if the current sensing gain is the same value as the ESR of the output capacitor, and the bandwidth is designed to be higher than the ESR zero of the output capacitor.

Then, the only challenge left is how to design compensator A_v. Regardless of which kind of transfer function is chosen for A_v, it will not change the relationship of the two loops. As a result, the poles and zeros can be designed following the same rules for the current loop in the current mode control, such that:

$$A_v=\omega_i\cdot\frac{1+s/\omega_z}{s\cdot(1+s/\omega_p)}. \tag{16}$$

A zero ω_z is placed to compensate for the power stage double pole, so that the current loop will be stable with a phase margin of about 90 degrees. A pole ω_p is placed in the high-frequency range to filter the switching-related noise. It is especially important to design ω_i large enough so that the current loop has a crossover frequency that is higher than the ESR zero of the output capacitor.

With the proposed design for R_{i1} and A_v, we can achieve equal crossover frequency for the current and voltage loops and a stable system. Fig. 8 shows the loop gains and phases for a buck converter with active droop control based on the small-signal model. T_2 is the outer loop, which determines the system stability.

$$T_2=\frac{T_v}{1+T_i} \tag{17}$$

Fig. 8 shows the stable current loop and outer loop. All three loops (current loop T_i, voltage loop T_v and outer loop T_2) have nearly the same crossover frequency. At high frequencies, the current loop undergoes a significant phase change due to the current sample and hold effect [15].

The closed-loop output impedance is:

$$Z_{o\_c}=\frac{Z_o\cdot(1+T_i)+T_i\cdot\dfrac{G_{vd}\cdot G_{ii}}{G_{id}}}{1+T_i+T_v}. \tag{18}$$

Fig. 9 shows the closed-loop output impedance of the proposed design using active droop control. The open-loop output impedance is a typical secondary-order system with a power-stage double pole. With the proposed closed-loop design, the impedance gain is almost constant, the value of which is just the ESR of the output capacitor. The impedance phase is also almost constant with a value of zero. The phase change is within ±10 degree in the entire frequency range. All of these indicate a constant output impedance design. The transient voltage spike is about $R_c\cdot\Delta I_o$, and the steady-state voltage droop is controlled exactly with this value. As a result, the optimal design for the transient can be achieved.

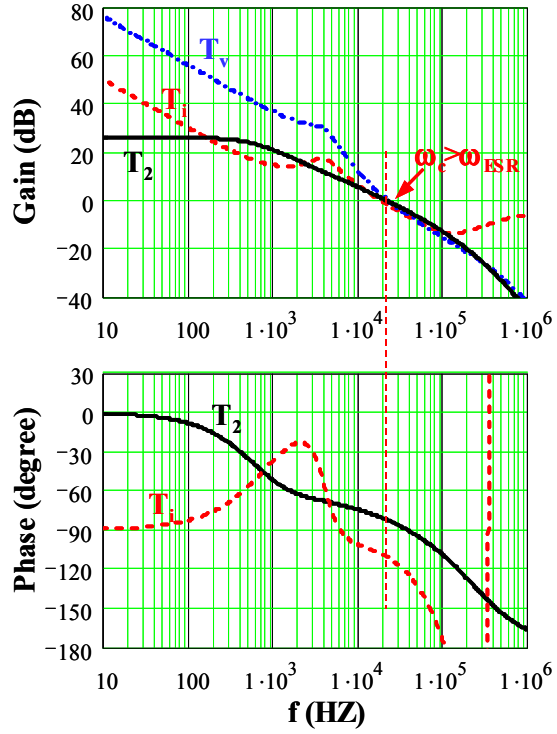

Figure 8. The loop gain and phase of the active droop control.

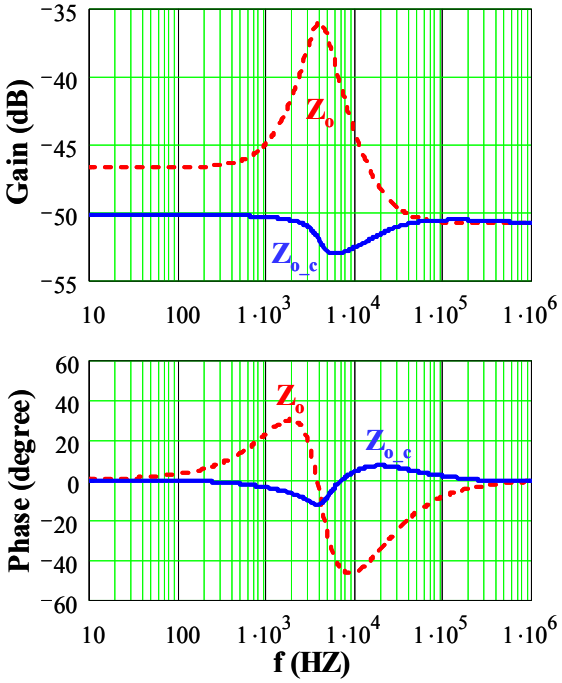

Figure 9. The output impedance.

V. Simulation and Experimental Results

A two-phase interleaved buck converter is designed for a 12V-to-1.5V/25A VR to verify the theoretical analysis. Fig. 10 shows the circuit. Four Oscon capacitors (820μF/4V) are used in parallel as the bulk output filter capacitor C_o. Each capacitor has an ESR of about 12 mΩ. According to (8), the ESR zero of the output capacitor is about 16 KHz. As a result, the bandwidth is designed to be 20 KHz, which is very easy to achieve with a 250KHz switching frequency. The output filter inductor in each phase is set as 1 μH, following the design guideline of the critical inductance [17]. The current ripple is relatively small, so high efficiency is expected.

Fig. 11 shows the PSPISE simulation results for the transient response. The compensator design follows the discussion in Section IV. Perfect AVP is achieved.

For the real prototype, Hitachi's 30V trench MOSFETs with SO-8 lead-free packaging are used for their good performance. HAT2116H is used for the top switches Q1 and Q3 because of its fast switching speed. HAT2099H is used for the bottom switches Q2 and Q4 due to its low conduction resistance. The gate driver is National Semiconductor's LM2726, which has fast driving capability and can drive both the top and bottom switches with self-adaptive dead time control. Intersil's multiphase controller HIP6301 is used, since it adopts the active droop control method and has the current sharing function. A TDK EIR-18 core with 2-turns winding structure is used to implement the 1 μH output inductor in each phase.

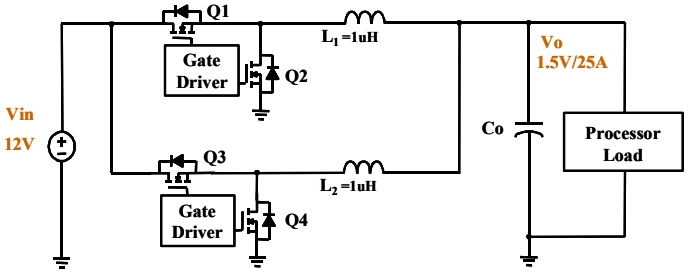

Figure 10. The designed two-phase interleaved buck converter.

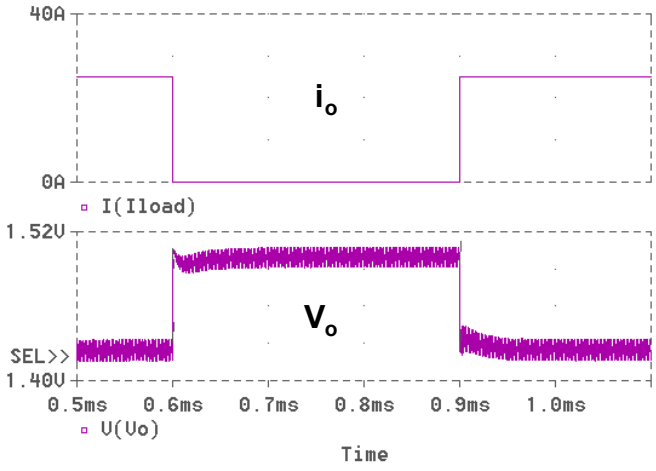

Figure 11. The simulation results for the transient.

Fig. 12 shows the test waveforms of the transient response. Almost-ideal AVP is achieved by following the feedback control design given in Section IV.

Fig. 13 shows the test efficiency of the whole VR. The full-load efficiency is more than 89%, and the peak efficiency is more than 92%.

Fig. 14 shows the developed prototype. The inductors can be replaced with some commercial ones.

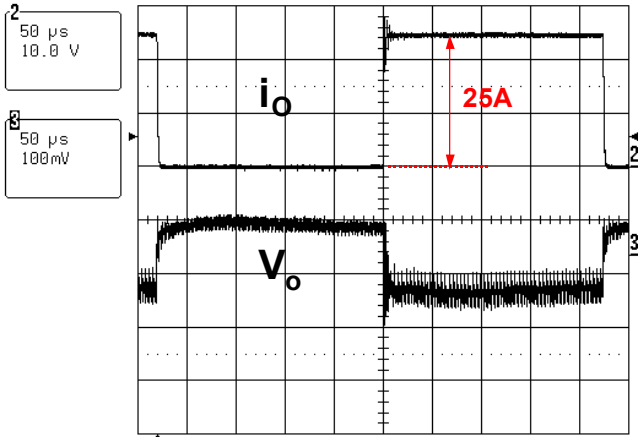

Figure 12. The experimental results for the transient.

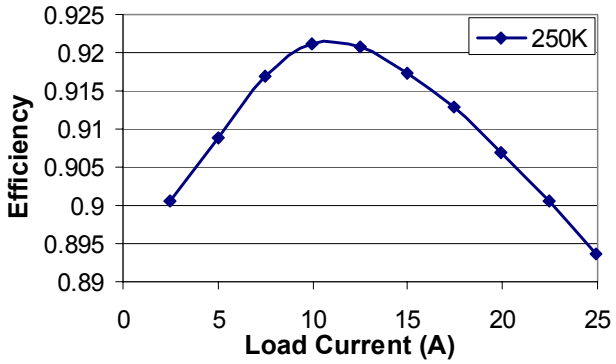

Figure 13. The VR efficiency.

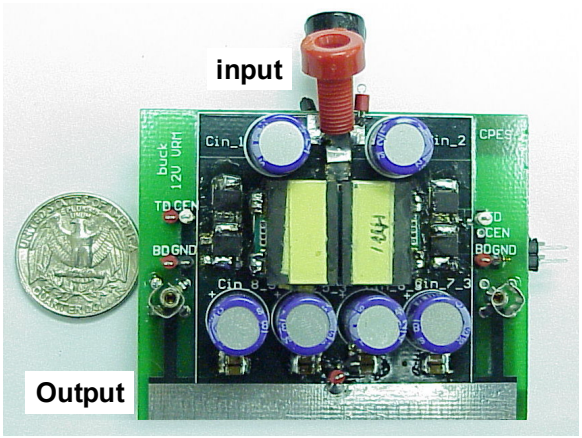

Figure 14. The developed prototype.

VI. CONCLUSION

This paper uses a small-signal model to discuss in detail the active droop control method. Based on the analysis of the dynamic relationship between the current and voltage loops, the same crossover frequency design for the two loops is proposed. A design guideline is developed for the feedback compensator design in order to achieve perfect AVP control. Simulation and experimental results prove that the optimal design is achieved for the active droop control, and that good transient response and high efficiency are obtained.

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