Optimal Dynamic Range Integrators

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Abstract—**The design of optimal dynamic range integrators that are meant as building blocks for optimal dynamic range analog continuous-time filters is discussed. A fundamental limit for the dynamic range of an integrator is given. This limit is a function of the supply voltage and the available amount of capacitance. It is shown how integrators are to be designed if this limit is to be reached. Different conventional integrator realizations are evaluated and optimized, so that they can be compared to the fundamental limit. A design example of a filter with integrators that approach this limit closely is given.**

I. Introduction

In many applications, the key problem of integrable continuous-time analog filters is their dynamic range, which is defined as the ratio of the largest and the smallest signal level which the circuit can handle. The largest signal level is determined by clipping or distortion, the smallest one by noise. Applications in which the dynamic range of analog filters is critical are radio and audio circuits. In video circuits the dynamic range that is wanted is usually less, and therefore less critical.

In critical applications one should optimize the dynamic range of the filter. Optimization can take place at different levels: the filter network and the building blocks that constitute the filter can be taken into consideration. As a direct consequence of its definition, an nth-order filter consists of a network of n integrators if differentiators are excluded. If one wants to design high dynamic range filters one should therefore be able to design high dynamic range integrators as filter components. This is the subject of this paper.

As high side of the dynamic range we adopt the signal level where clipping occurs. In some applications (for instance intermediate-frequency filtering) this is not appropriate, because below this signal level distortion may already be too much. In these situations, the level where distortion products just rise above the noise level is taken as maximal signal level. One then talks about *distortion-free* dynamic range. We will not handle this measure in this article, but because the type of dynamic range that we discuss here is an upper limit for the distortion-free dynamic range, it is still important for situations where distortion-free dynamic range is of primary importance.

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In the past, many types of integrators have been proposed. These have different dynamic-range properties. When all these propositions are considered, it is not evident which one can have the largest dynamic range. In fact, one wants to know what the maximal dynamic range is that can be attained using integrated integrators, and how this maximum can be attained.

For this end, we want to compare the possible integrators in a systematic way. Therefore, first a division of integrators in four categories is made. After that we show how the dynamic range of an integrator is defined and can be evaluated. For this evaluation, the noise characteristics and the maximal signal levels belonging to the integrator must be known. Therefore, these are discussed first. If the definitions and the evaluation methods for the dynamic range are discussed, we formulate a fundamental maximum for the dynamic range. Using the different categories of integrators we met, the dynamic range of different types of integrators is evaluated and optimized. The results are compared to the fundamental maximum. In this way, a figure of merit for the different types of integrators is obtained, which makes it possible to determine what kind of integrator can best be used for optimal filters in different situations. It is shown that there are two ways to construct an integrator that reaches the fundamental maximum. These are favored if dynamic range is the only design constraint. In other situations, where for instance very high working frequencies or a large tuning range are needed, other stages may be preferred.

II. Realizations of Integrators

An integrator is an electronic circuit that realizes the transfer function a_0/s, where a_0 is a real number, and s is the Laplace operator.

When an integrator is to be realized on a chip the part of the integrator that performs the integration is a capacitor. The input signal of this capacitor is a current, whereas the output signal is a voltage. Therefore, the capacitor implicitly realizes an impedance function. In a filter, inputs of integrators must be connected to outputs of other integrators so that voltage-to-current converters are necessary. More specific, if the input signal of one integrator is the output signal of another integrator, a voltage-to-current converter should be present between the capacitor of the first integrator and the capacitor of the second integrator; that is, *the impedance function of the capacitor must be matched by an admittance function.* The converter can be seen as a part of the first integrator or as a part of

the second integrator. In the first case the converter is placed at the output of the integrator, in the second case at the input of the integrator. This choice is only a matter of point of view, but has no consequences for the filter itself. We will therefore follow the usual convention, in which the converter is situated at the input of the integrator. This implies that the input quantity, as well as the output quantity of the integrator is a voltage.

In this way an integrator consists of an admittance part, realizing the admittance function, and an impedance part, realizing an impedance function. The impedance part contains the integrating capacitor C and the impedance function has a value $1/sC$, whereas the admittance function has the real value G; G is the transadmittance factor of the stage that realizes the admittance part, defined as the ratio of the small-signal output current and the small-signal input voltage. This is a convention that we will use throughout this paper. The realizations of these functions can differ from this assumption due to parasitic high and low frequency effects, but that is not included in the scope of this paper.

The impedance function can be realized as an impedance or as a transimpedance and the admittance function can be realized as an admittance or as a transadmittance. This gives rise to four types of integrators, which are shown in Fig. 1. The admittance-impedance integrator of Fig. 1(a) is in many cases not practical because it has its pole not in the origin of the s-plane. The transimpedances in Fig. 1 are realized with opamps.

Usually one should be able to electronically tune the integrators. There are two ways to realize this, namely by a tunable capacitance (a tunable impedance function) or by a tunable admittance function. A tunable capacitance is usually realized as a junction capacitance with adjustable bias voltage. If this option is used, it is likely that it is the capacitance that imposes an upper limit to the signal level at the output of the integrator. Larger signal levels can be handled if a fixed linear capacitance is used. We assume therefore that the capacitor is linear, so that the maximal signal level is not determined by the capacitance. Tuning is then realized in the admittance part.

When it is important to keep the distinction between different types of admittances clear, we denote transadmittances by active admittances, and the other type by passive admittances. The word admittance is then used for both types together. A similar convention is used for impedances.

III. Noise

Dynamic range is determined at the low side by noise. It is the admittance part of the integrator that is responsible for the production of noise.

When it comes to noise behavior, an integrator is modeled here as a noise-free integrator that has a noise voltage source with (double-sided) voltage spectrum

$$S_{ni}(\omega) = \frac{2kT\xi}{|G|} \tag{1}$$

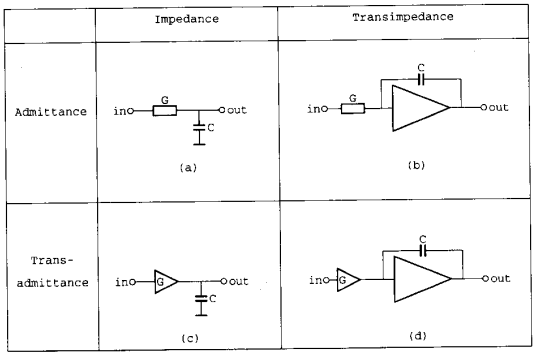

Fig. 1. Integrators can be classified into four types, dependent on the nature of the impedance part and of the admittance part.

in series with its input. In this equation, T is the absolute temperature, ξ is the noise factor of the integrator, that usually has a minimal value of 1; k is the Boltzmann constant, and G is the value of the transadmittance function.

We consider the noise spectrum to be white, so $1/f$-noise is discarded. The main reason for discarding this kind of noise is the fact that we are interested in optimal dynamic range integrators. Therefore, we only consider fundamental dynamic-range limitations. $1/f$-noise normally is no fundamental limitation as an integrator can usually be designed such that this type of noise is not dominant. How this can be done will be shown later on.

From the input-referred noise voltage spectrum, the input-referred total noise level $\overline{V_{ni}^2}$, that can be interpreted as the mean squared input-referred noise voltage, is determined by integrating $S_{ni}(\omega)$ over the noise bandwidth:

$$\overline{V_{ni}^2} = \frac{1}{2\pi}\int_{-B}^{B} S_{ni}(\omega)\,d\omega. \tag{2}$$

It makes sense to equal the noise bandwidth B to the crossover frequency $|G|/C$ of the integrator, because if the integrator is used in a low-pass filter, this frequency is in general approximately equal to the bandwidth of this filter. If this is done, the following expression is obtained for the equivalent total input noise level of the integrator.

$$\overline{V_{ni}^2} = \frac{2kT\xi}{\pi C}. \tag{3}$$

Here we see that the noise production of an integrator is in the first place dependent on the capacitance value that is used, and not on G as could be concluded from (1).

IV. Maximal Signal Levels

The high side of the dynamic range of an integrtaor is the maximal signal level it can handle. This is the maximal signal level that can appear at the input or at the output of the integrator. Due to the conventions we took in Section II, the input and output signals of the integrator are voltages.

To separate the signal voltage from the bias voltage at a certain point, we call the excursion from the bias level—due to an applied signal—of the voltage at this point the *value* of this signal. The *level* of a signal is the mean of its squared value in a certain time interval. The amplitude of a signal is its maximal absolute value in a time interval. The *swing* of a signal is the difference between its maximal (most positive) and minimal (most negative) value in a time interval. In the case of a periodical signal one period is taken for the time interval.

In a practical filter environment, the output signals of the integrators are the input signals of other integrators. Therefore, the integrators must be able to handle the same signal level at their inputs as at their outputs. So the actual maximal signal level an integrator can handle is the smallest of the maximal input signal level and the maximal output signal level. We denote the maximal signal amplitude corresponding to this level by V_{max}. If it is assumed that the signal is sinusoidal, as we do, its maximal level is then given by $V_{max}^2/2$.

If the integrator is of the transadmittance impedance type, in which the transadmittance part contains a single stage, the input voltage range is dependent on the output voltage. An example of such an integrator is shown in Fig. 2. For this integrator the voltage at the negative input may not rise more than about 0.4 V above the voltage at the positive output. This means that the maximal input signal amplitude is not only dependent on the output signal amplitude, but also on the phase relation between the input signal and the output signal.

If the integrator is to be used in a practical filter, no assumptions about the phase relations between the input and the output signal can be made, because it can have more than one input. The phase relations between the diverse input signals are not known in advance, and therefore the phase of the output signal is also not known. A worst case approach, in which the output signal maximally limits the input signal, must be used. For the transadmittance stages we will meet in this article, this means that we have to assume that the input and output signals are in antiphase. Because we saw that the amplitudes at the input and the output of the stage are equal, this means that we assume that

$$V_{out} = -V_{in} \tag{4}$$

if V_{out} and V_{in} are the output and input signal voltages, respectively.

The dependence of the maximal input signal level on the output signal can be eliminated by furnishing the transadmittance with a separate output stage. This may increase its maximal input signal level, as well as its maximal output signal level. This possibility is discussed later.

V. Dynamic Range

The dynamic range of a circuit is defined as the ratio of the maximal and minimal signal level the circuit can handle at the same time. The maximal signal level is

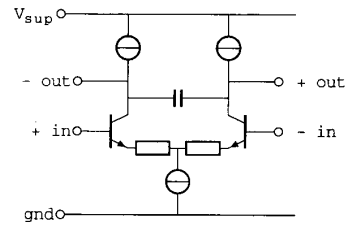

Fig. 2. A transadmittance impedance type integrator.

$V_{max}^2/2$, as explained in Section IV. As minimal signal level at the input we will use the input-referred noise level $\overline{V_{ni}^2}$. The dynamic range is then

$$DR = \frac{V_{max}^2}{2\overline{V_{ni}^2}}. \tag{5}$$

With (3) the dynamic range is expressed as

$$DR = \frac{\pi V_{max}^2 C}{4kT\xi}. \tag{6}$$

We see that the dynamic-range limiting factors of an integrator are its capacitance, its noise factor and the maximal signal level it can handle.

The appearance of the capacitance in the expression for the dynamic range is fundamental. To illustrate this, we determine the intrinisic dynamic range of a capacitor. This will give us a clue to determine the largest dynamic range that can be obtained with integrators that consist of admittances and capacitances, either active or passive, if the available amount of capacitance is a limiting factor.

5.1. Dynamic Range of a Capacitor

Fig. 3 shows a very simple low-pass filter, consisting of a capacitor with value C and a conductor with value G. The conductor produces noise that can be modeled as in (1) as a voltage source with spectrum $S_G(\omega) = 2kT/G$. This results in an output noise voltage with spectrum

$$S_o(\omega) = \frac{2kT/G}{1 + (\omega C/G)^2}. \tag{7}$$

If this spectrum is integrated the mean squared total output noise voltage results:

$$\overline{V_{no}^2} = \frac{1}{2\pi}\int_{-\infty}^{\infty} S_o(\omega)d\omega = \frac{kT}{C}. \tag{8}$$

This noise level is independent of the conductor, and can thus be seen as an intrinsic property of the capacitor.

If the maximal signal amplitude over the capacitor, due to the limits of the surrounding circuitry, is V_{max}, and the signal is assumed to be sinusoidal, the dynamic range of the capacitor, when defined as the ratio of the maximal mean squared output signal voltage and the mean squared output noise voltage is

$$DR_{cap} = \frac{V_{max}^2 C}{2kT}. \tag{9}$$

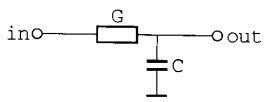

Fig. 3. A G-C type low-pass filter.

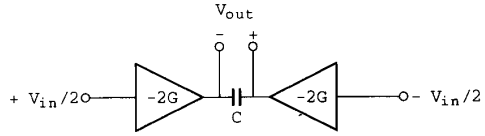

Fig. 4. If the capacitance is used floating between the outputs of two transadmittances, the maximal possible signal voltage across it can be maintained.

This equation is different from (6) because another definition of the noise bandwidth is used. In this situation, the noise bandwidth is known because the filter network is known. If an integrator is regarded apart from its filter context, the noise bandwidth is not known, and an assumption must be made. This has been done in the derivation of (6). The exact assumption that is made may influence the value of the dynamic range that is obtained, but it has no consequence for the optimization processes.

If the conductor in this circuit is replaced by a network of transadmittances with a noise factor that equals 1, the dynamic range that is obtained is equal to or less than the amount indicated by (9). In this way the capacitance imposes a lower limit to the noise production of any integrator that consists of an impedance part that contains the capacitance and a real valued admittance part. Together with the maximal signal level constraint that is imposed by the surrounding circuitry, an upper limit to the dynamic range is given by (9).

5.2. A Fundamental Maximum

From (9) we see that to maximize the dynamic range of the capacitor in an integrator, the maximal signal voltage over the capacitance must be maximized. We assume that the maximal signal level in the integrator is limited by the supply voltage. That is, if the supply voltage is V_{sup}, the maximal signal amplitude at any node in the circuit is $V_{sup}/2$. The maximal signal amplitude between two nodes is then V_{sup}, a value that is reached when the signals at the two nodes under consideration are in antiphase. Therefore, the maximal signal amplitude over the capacitor is V_{sup}.

A configuration in which the signal voltage over the capacitance can be made near to this maximal value is shown in Fig. 4. The capacitor there is shown to be connected between the outputs of two transadmittance stages. To make the differential transfer function of this integrator equal to $\pm G/(sC)$, the transadmittance factor of each of the two transadmittance stages must be $\pm 2G$. This means that the differential input-referred noise voltage of this integrator corresponds to that of a single-ended integrator with a transadmittance stage that has a transadmittance factor G.

In this context, V_{max} is the maximal differential signal amplitude at the input or at the output of the integrator. To avoid mixing up different conceptions, the single-ended maximal signal amplitude is denoted by $V_{max,s}$, so

$$V_{max} = 2V_{max,s}. \tag{10}$$

In order to reach the maximal signal amplitude V_{sup} over the capacitor when using this configuration, the transadmittance stages must be constructed in such a way that their maximal and minimal output voltages are equal to the maximal and minimal supply voltages. We will discuss further on to what extent this is possible.

A practical argument against using the capacitance differentially like this might be that it must be floating, while floating on chip capacitances usually have a parasitic capacitance from one of its connections to signal ground. This, however, does not need to be a problem because extra parasitic capacitances at the outputs of a passive impedance integrator do not influence its performance. Only the time constant is affected, which can be compensated for by an adjustment of the transconductance. As the extra parasitic capacitance appears at one side of the integrator, its symmetry will be affected. To overcome this problem the capacitor should be realized as an anti-parallel connection of two identical capacitors.

Now if it is assumed that the noise factor ξ has a minimal value of 1, an upper limit to the dynamic range that can be obtained if the supply voltage is V_{sup} and the available capacitance is C is, according to (6):

$$DR_{MAX}(V_{sup}, C) = \frac{\pi V_{sup}^2 C}{4kT}. \tag{11}$$

For a supply voltage of 5 V and a capacitance of 10 pF this upper limit is 107 dB. To reach this dynamic range, two requirements must be fulfilled:

- the noise factor of the integrator must be 1, and
- the voltages at the two connections of the capacitor must be able to assume the full range between the supply voltages, and these signals must be in antiphase with respect to the arithmetic mean of the highest and the lowest supply voltage.

There is a reason why these two requirements can not be fully met. The transadmittances in Fig. 4 control the current in the capacitor. To achieve this, the capacitor current is measured and, after conversion to a voltage, fed back to the input of a nullor that forms the heart of the transadmittance stage. If the capacitor current is to be measured, a component must be placed in series with the capacitor. This component is situated inside the transadmittance stage. In a situation where only conductive or capacitive components, or active components representing one or a combination of these groups, are available, this component must be a capacitance or a conductance (or a combination).

The voltage drop over this component limits the maximal voltage drop over the capacitor. Because the maximal output amplitude has to be as large as possible, the voltage drop over this component must be as small as possible. If this component is a capacitor, it must therefore be large when compared to the integrating capacitor. This is not what we want, because the available capacitance is limited, and can in order to attain a large dynamic range better be used as integrating capacitance, according to (6). Therefore, we choose a conductive element for the current measurement. Its conductance must be large if the voltage drop over it must be small. But this increases its noise current, which directly appears at the output. So the conductance must be neither very low nor very large for an optimal dynamic range, which means that an optimal value must be found.

A representative situation is depicted in Fig. 5. Here, a transadmittance stage that is to be used in the configuration of Fig. 4 is shown to be realized around a nullor N. The output current of the nullor is measured via a conductance $2aG$, where a is a dimensionless constant, still to be specified, and the resulting voltage is fed back to the input of the nullor via a voltage amplifier A, that has an amplification factor a. The transadmittance factor of this stage is $-2G$, so a is the ratio of the measuring conductance and the absolute value of the transadmittance. Because we want to find a fundamental maximum for the dynamic range, we assume that the nullor and the voltage amplifier are noise-free; it should be possible to design these such that their noise contribution is negligible. For the same reason we assume that the maximal and minimal terminal voltages of the nullor and the voltage amplifier equal the maximal and minimal supply voltages. This demand can be closely met [1]–[3].

The noise in this circuit originates from the conductor. It results in an equivalent input-referred noise voltage source with spectrum $4kTa/(2G)$, so the noise factor of this circuit is

$$\xi = a. \tag{12}$$

Let us assume that the supply voltages are $+V_{sup}/2$ and $-V_{sup}/2$. Due to symmetry, the quiescent level at the input and the output of the stage then is zero. The maximal voltage at the output of the nullor is then $V_{sup}/2$. The maximal output voltage of the stage is therefore $V_{sup}/2 - I_o/(2aG)$. I_o is the output current, which equals $-2GV_{in}$, if V_{in} is the input voltage. So

$$V_{out} \leq \frac{V_{sup}}{2} + \frac{V_{in}}{a}. \tag{13}$$

If this is combined with (4), $V_{max,s}$ can be determined:

$$V_{max,s} = \frac{V_{sup}a}{2(a+1)}. \tag{14}$$

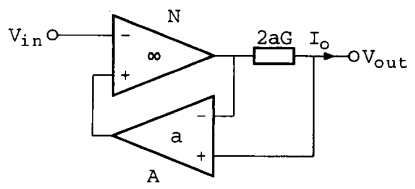

Fig. 5. A model for a transadmittance stage with transadmittance factor G. It consists of a nullor N, a voltage amplifier with amplification factor a, and a measuring conductance aG.

Due to (10) and (6), the dynamic range of the stage, if it is used differentially, is

$$DR = \frac{a}{(a+1)^2}\frac{\pi V_{sup}^2 C}{4kT}. \tag{15}$$

By solving $dDR/da = 0$, a maximum for $a = 1$ is found. At this maximum, the maximal signal amplitude over the capacitor is $V_{sup}/2$, and the noise factor is 1. The optimal dynamic range is then

$$DR_{opt} = \frac{\pi V_{sup}^2 C}{16kT}. \tag{16}$$

Note that by (12) it is possible to construct in this way a transadmittance stage with a noise factor that is smaller than 1, but from our calculations it follows that this results in a suboptimal dynamic range.

The extra limitation on the output voltage due to the measuring conductance does not apply to active-impedance integrators, such as the one that is shown in Fig. 1(b). The maximal output voltage of this integrator is limited by the op-amp only. If we assume, as we did above, that the maximal and minimal output voltage of the op-amp is limited only by the supply voltages, the maximal output signal amplitude is $V_{sup}/2$. In this configuration it is not possible to use the capacitor differentially with both connections driven in antiphase; one of the connections must be connected to virtual ground. Therefore, the maximal signal amplitude over the capacitor is $V_{sup}/2$. As the noise factor of this stage can not be made smaller than 1 in an optimal configuration, an upper limit for the dynamic range of this type of integrator is also given by (16).

We may conclude that there is no way to design an integrator with a dynamic range that is larger than indicated by (16). This value is therefore a fundamental maximum that we designate by DR_{max} and lies below the maximum indicated by (11):

$$DR_{max} = \frac{\pi V_{sup}^2 C}{16kT}. \tag{17}$$

If the supply voltage is 5 V, and the capacitance is 10 pF, this maximum is 101 dB.

Now to every integrator we can assign a figure of merit that reflects its "optimality" with respect to dynamic range. We denote this figure by the letter ζ that, by convention, has a value between 0 and 1, and is defined as the ratio of

the dynamic range of a practical integrator having a supply voltage V_{sup} and a total capacitance C, and the maximum by (17), or

$$DR(V_{sup}, C) = \zeta DR_{max}(V_{sup}, C) \qquad (18)$$

where DR is the dynamic range of the integrator under consideration. One way to realize an integrator that has a ζ of 1 is indicated by Figs. 4 and 5, another such integrator can be the admittance-transimpedance integrator of Fig. 1(b). We will discuss these and other stages in following sections.

VI. Differential

In many cases, one wants to realize the integrator differentially, mainly to reduce even-order nonlinearity, but also to reduce the effects of common-mode interference. Here we discuss what the effects of realizing the integrator differentially are on the dynamic range. Fig. 6 shows a single-ended and a differential version of an active-impedance integrator. These are realized with a single-ended and a differential op-amp, respectively [4]. As the total capacitance is a dynamic range determining factor, the total capacitance has the same value for both versions. Due to (3) the input-referred noise level $\overline{V_{ni}^2}$ for each input of the differential integrator is twice as much as the input-referred noise level of the single-ended version. The differential input-referred noise level is therefore four times as much. The maximal differential input signal level (which is proportional to the square of the maximal input signal amplitude) is also four times as much as for the single-ended version, and therefore the dynamic range of both types is the same.

For passive-impedance integrators the situation can be different. Fig. 7 shows one single-ended and two differential transadmittance-impedance integrators. The transadmittance factor of the differential transadmittance stages is, in accordance with the usual convention, defined as the ratio of the single-ended output current and the differential input voltage.

For the integrator of Fig. 7(b) the same reasoning applies as for the integrator of Fig. 6(b). This means that the integrators of Fig. 7(a) and (b) have the same dynamic range. For the integrator of Fig. 7(c) the situation is different. Its transconductance factor is the same as the transconductance factor of the unbalanced integrator. Therefore, its differential input-referred noise level is the same as the single-ended input-referred noise level of the single-ended stage. Its maximal differential input signal amplitude is twice the maximal signal amplitude of the single-ended version. Therefore, its dynamic range is a factor 4, or 6 dB, larger than the dynamic range of the single-ended integrator, when the same total amount of capacitance is used.

Ultimately, the reason for this increase in dynamic range is the fact that the capacitor is used differentially, so that the signal amplitude across the capacitor has increased by a factor two, as explained in Section 5.2.

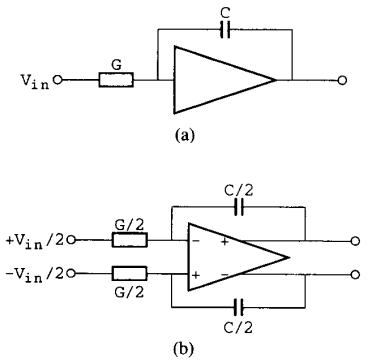

Fig. 6. A single-ended and a differential version of an active-impedance integrator, realized around a single-ended and a differential op-amp.

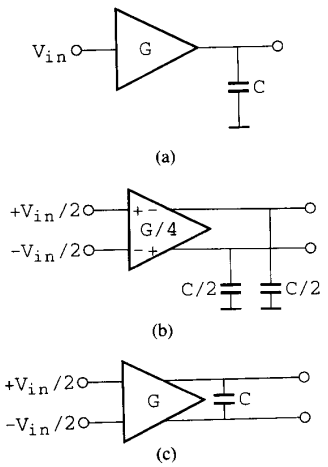

Fig. 7. Single ended and differential versions of a passive-impedance integrator.

VII. Biasing

Biasing transadmittance stages requires special attention, because the dynamic range of the stages depends on how the biasing has been arranged. In general, the bias sources produce noise, and they limit the maximal signal level. It will be shown in this chapter that if the noise production of the bias sources is reduced, the maximal signal level decreases. That is, in the design of the bias circuitry, the noise factor can be traded for the maximal signal level, and an optimum can be found. In some cases it is possible to design a bias circuit that effectively does not deteriorate the noise factor of the stage. We will go through a number of possible biasing schemes and figure out what type of biasing gives rise to the largest dynamic range.

7.1. Non-Floating

For the determination of the dynamic range it is assumed that all the transadmittance stages that are discussed here are to be used differentially in the configuration of Fig. 4. Therefore, all the transadmittance stages

that are discussed here have a transadmittance factor $-2G$.

Figure 8 shows how a transadmittance stage can be biased. The active part of the stage consists of a nullor with series feedback at the input and the output [5]. The feedback element is a conductance $2G$. For tunability, this conductance should be realized as a MOSFET conductance. We denote this part of the stage by the intrinsic transadmittance. It is biased with a current source, as shown in Fig. 8(a). In Fig. 8(b), the current source is implemented as a nullor with feedback via a conductance G_1. Fig. 8(c) shows a practical realization, in which the nullors have been realized as single bipolar transistors. To keep the discussion of the stage concrete, it will be held in conjunction with the implementation of Fig. 8(c).

The nullors should be designed in such a way that their noise contribution is negligible, as is the case in the realization of Fig. 8(c). The noisy elements in this circuit are the conductors. The noise contribution of the conductance $2G$ is unavoidable, because the value of this conductance determines the transconductance that is to be realized. The input-referred noise spectrum of this stage is

$$S_{ni}(\omega) = 2kT\frac{2G + G_1}{(2G)^2} \tag{19}$$

so the noise factor is

$$\xi = 1 + \frac{G_1}{2G}. \tag{20}$$

The noise production of the conductor in the bias current source is made as small as possible by making the conductance of this element as small as possible. If G_1 is made small, the voltage drop over this component will be large. This limits the dynamic range because it limits the maximal output signal level. Therefore, for the dynamic range to be maximal, G_1 must be neither very small nor very large. An optimum can be found.

As explained in Section IV we assume that the input amplitude is equal to the output amplitude, and that the input signal and the output signal are in antiphase. Because the output of the integrator in a filter is connected to inputs of other integrators, the input and output of this stage should be biased at the same level, which means that a level shifter should be connected to the input.

The current I_b that is delivered by the bias current source must be enough to supply the maximal output current of the stage. Supposing that the maximal (single-ended) input amplitude, as well as the maximal output amplitude is equal to $V_{\max,s}$, the bias current must minimally be $2GV_{\max,s}$. If the knee voltage of the transistors is negligible, the maximal output voltage of the stage is equal to the supply voltage minus the voltage drop over the conductor G_1, or

$$V_{\text{out,max}} = V_{\text{sup}} - \frac{I_b}{G_1} = V_{\text{sup}} - \frac{2GV_{\max,s}}{G_1}. \tag{21}$$

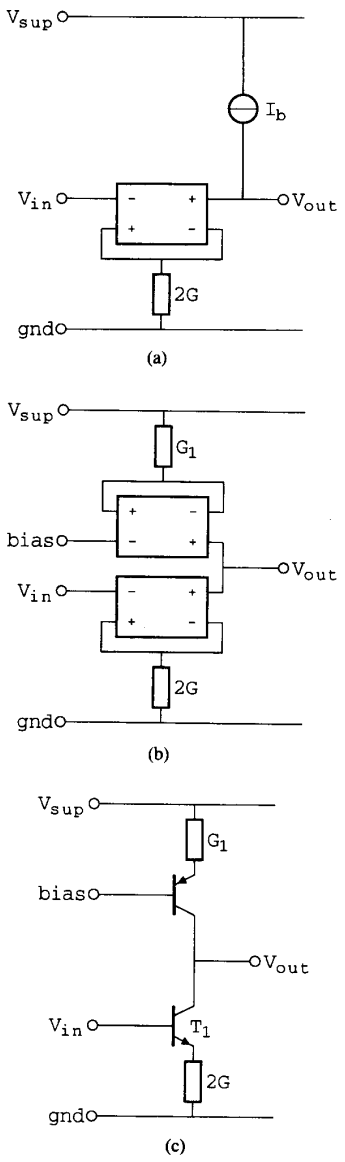

Fig. 8. The biasing of a transadmittance stage. The transadmittance factor of these stages is $2G$.

Because of the assumption that the output signal and the input signal are in antiphase, the maximal output voltage is reached if the input voltage is minimal, so that T_1 is not conducting. This happens if the input voltage V_{in} of this stage is equal to the base-to-emitter bias voltage V_{be} of the transistor. V_{be} is assumed to be constant. As the maximal input signal amplitude must be minimally equal to $V_{\max,s}$, the input must be biased at $V_{\max,s} + V_{\text{be}}$ or more.

The minimal output voltage is reached if the collector-emitter voltage of T_1 is equal to the knee voltage of that transistor, which is assumed to be zero. Because of the antiphase assumption, the minimal output voltage is

reached if the input signal voltage has its maximal value of $V_{max,s}$. Because, as we saw, the input bias voltage should minimally be $V_{max,s} + V_{be}$, and the maximal input signal amplitude is $V_{max,s}$, the maximal input voltage is minimally $2V_{max,s} + V_{be}$, so the minimal output voltage is

$$V_{out,min} = 2V_{max,s}. \tag{22}$$

The observation that

$$V_{max,s} = \frac{V_{out,max} - V_{out,min}}{2} \tag{23}$$

together with (21) and (22) can be solved for $V_{max,s}$. This results in

$$V_{max,s} = \frac{V_{sup}}{4 + \frac{2G}{G_1}}. \tag{24}$$

With (20) this is rewritten as

$$V_{max,s} = V_{sup}\frac{\xi - 1}{4\xi - 3}. \tag{25}$$

This is substituted with (10) into (6) to yield the dynamic range expressed in ξ:

$$DR = \frac{16(\xi - 1)^2}{(4\xi - 3)^2\xi} \cdot \frac{\pi V_{sup}^2 C}{16kT} \tag{26}$$

so that, by (17) and (18),

$$\zeta = \frac{16(\xi - 1)^2}{(4\xi - 3)^2\xi}. \tag{27}$$

By differentiating an optimum can be found. The optimal value for ξ is $(9 + \sqrt{33})/8$ or 1.84, giving rise to an optimal value of ζ:

$$\zeta_{opt} = \frac{69 - 11\sqrt{33}}{18} \equiv -4.9\ \text{dB}. \tag{28}$$

The optimum implies a noise factor of 1.84, so the stage is not noise optimal. By (20) a noise factor close to 1 is realizable, by choosing $G_1 \ll G$. But as explained above, this gives rise to a low dynamic range. The optimization of the dynamic range as shown above can be seen as dividing the supply voltage optimally over the intrinsic transadmittance part of the circuit and the bias current source. Making the noise factor close to 1 then means reserving a large portion of the supply voltage for the bias current source, leaving a small amount for the intrinsic transadmittance. This limits the maximal signal levels, and thus the dynamic range.

There is a better way to reduce the noise factor to 1. The reason why the noise factor is larger than 1 is that the bias source produces noise without doing anything to the signal in return. This problem is alleviated by making the bias source an active part of the transadmittance. If this is done, the noise production of the stage corresponds to its transadmittance, so that the noise factor is reduced to 1.

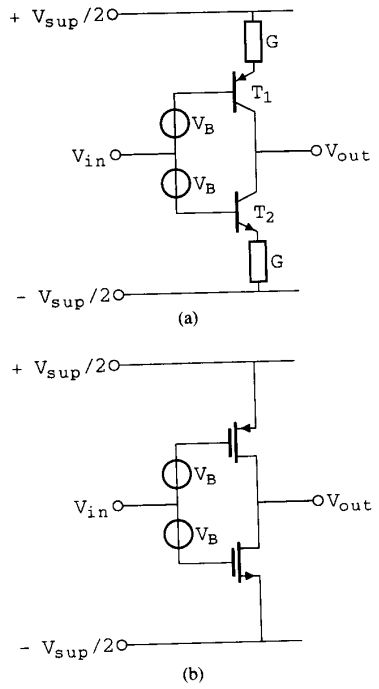

Fig. 9. Noise-free biasing of transadmittances.

Fig. 9 shows the principle. The circuit of Fig. 9(b) has been used by Nauta and Seevinck [6], [7] for frequencies well above the transit frequency of the MOSFET's.

As the noise factor of these stages is close to 1, optimization of the dynamic range is done by optimizing the maximal signal levels the stages can handle, which in turn is done by optimizing the bias voltage V_B, shown in the figure.

Utilizing the symmetry of the circuits, the supply voltage V_{sup} is divided in two equal parts $\pm V_{sup}/2$ over the supply rails. Due to the symmetry an optimal maximal input and output signal swing implies that the bias voltages at the input and output are zero.

We use the conventions

$$V_B' = V_B + V_{be} \tag{29}$$

for the bipolar version and

$$V_B' = V_B + V_t \tag{30}$$

for the MOSFET version. V_t is the threshold voltage of the MOSFET's. If the threshold voltages of the two FET's are not equal, this can be compensated by choosing the bias voltages V_B, which are chosen equal in Fig. 9, unequal.

Then optimizing the dynamic range yields

$$V_B' = \frac{1}{3}V_{sup} \tag{31}$$

$$V_{max,s} = \frac{1}{6}V_{sup}. \tag{32}$$

So according to (6) and (10), the maximal dynamic range of these stages is

$$DR = \frac{4}{9}\frac{\pi V_{sup}^2 C}{16kT}. \quad (33)$$

According to (17) and (18) these stages have a ζ of 4/9, or -3.5 dB.

It is instructive to compare the stage of Fig. 9(a) to the stage of Fig. 5. In fact, these two stages have the same construction, and yet have a different dynamic range. The reason is, that in the stage discussed here there is a bias voltage over the conductances G, which imposes an extra limit to the maximal output signal amplitude.

The dynamic range of the stage of Fig. 9(a) can therefore be further improved by biasing it in class B. Then there is no bias current through the transistors or the conductances, and thus also not a bias voltage over the conductances. The bias voltages V_B' must then be made equal to $V_{sup}/2$, and the conductances with value G must be replaced by conductances with value $2G$. With zero input voltage, both transistors are not conducting. When the input voltage is positive T_2 conducts, and T_1 conducts when the input voltage is negative. If the input and output signal are in antiphase, the maximal input amplitude or output amplitude is $V_{sup}/4$, which makes ζ equal to 1. This can not be done to the stage of Fig. 9(b), because in that case operation in class A is essential for second order distortion cancellation. Although this possibility has theoretical value, the practical value is not clear because it is difficult to avoid cross-over distortion in a practical implementation.

Another circuit is shown in Fig. 10. The MOSFET's are both biased in the nonsaturated or triode region. In this region, the relation between the drain current I_d and the gate-source voltage V_{gs} is approximately given by [8]

$$I_d = \frac{W}{L}\mu C_{ox}'\left[(V_{gs} - V_t)V_{ds} - \frac{1}{2}(1+\delta)V_{ds}^2\right] \quad (34)$$

where W and L are the width and length of the transistor, μ is the effective electron mobility, C_{ox}' is the gate-to-channel capacitance per unit area, V_{ds} is the drain-to-source voltage, and δ is a bias-dependent parameter with a value about 0.12. By this equation, if V_{ds} is constant, the dependence of the drain current on the gate-to-source voltage is linear, even if one transistor is used in a single-ended configuration. This principle to realize a linear transadmittance has in different configurations been utilized by Pennock [9] and Wong [10]. In the configuration of Fig. 10, a bipolar transistor is used to keep the drain voltage of the MOSFET to a fixed value. A MOSFET is less suited for this end, because it intrinsically has a much higher output impedance than a bipolar transistor, and will thus be less able to fix the drain voltage of T_1 and T_4 in Fig. 10.

The noise production of a transistor in the triode region corresponds to an equivalent channel resistance, and not directly to the transconductance. Therefore, its noise factor is larger than 1. As was the case with the stage of Fig. 8(c), it is possible to optimize this stage by trading the noise factor for the maximal signal level. Results of optimization are shown in Table I. Only two values for δ are used here; $\delta = 0$ because that is a much used value in simple MOSFET models and because this value gives the largest dynamic range, which can be used as an upper limit, and $\delta = 0.12$ because this value gives the largest dynamic range, which can be used as an upper limit, and $\delta = 0.12$ because that is a more realistic value. It appears that there is only a very small difference in biasing and performance between the situations corresponding to these two values.

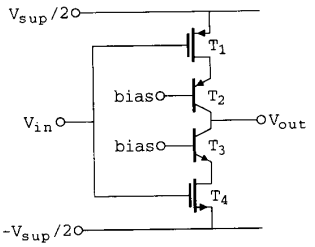

Fig. 10. A transadmittance stage using MOSFET's in the triode region.

TABLE I
THE OPTIMAL VALUES FOR V_{ds}, ξ, THE MAXIMAL DIFFERENTIAL SIGNAL AMPLITUDE AND ζ FOR THE STAGE OF FIG. 10, FOR TWO DIFFERENT VALUES OF δ

δ	V_{ds}/V_{sup}	ξ	V_{max}/V_{sup}	ζ
0	0.186	2.22	0.628	0.709 −1.5 dB
0.12	0.182	2.35	0.636	0.688 −1.6 dB

A great advantage of this stage over other stages is its wide tuning range. By varing V_{ds}, the stage can be tuned from zero to about 2.5 times its nominal transconductance. However, if the stage is tuned over a large distance from its optimal bias condition, its dynamic range decreases. If tuning is only used for compensating component tolerances, a tuning range of $\pm 25\%$ usually is enough. In that case, the dynamic range can diminish by 0.45 dB. Fig. 11 shows what happens to the dynamic range if the stage is tuned over its whole range when the stage is nominally optimal for $\delta = 0.12$.

7.2. Floating

The transadmittance stages of the previous section can be made floating by adding one or more extra bias current sources. This is one way to achieve a large common-mode rejection ratio, that in some differential filters is needed to ensure common-mode stability. Fig. 12 shows how the circuits of Figs. 8(c) and 9(a) can be made floating. These floating stages have almost the same differential-mode properties as their nonfloating counterparts discussed above. The only difference is that, due to the extra current sources, effectively less supply voltage is available for the stages. This means that the dynamic range of the

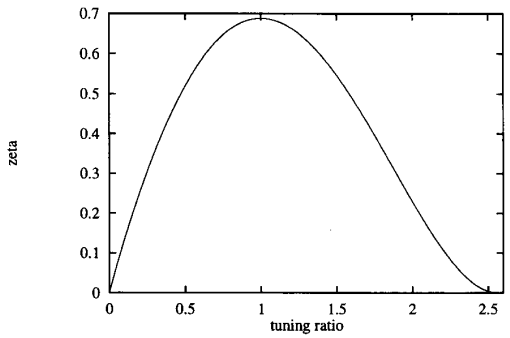

Fig. 11. The dependence of ζ on the tuning condition, which is the ratio of the actual transconductance and the nominal transconductance, of the stage of Fig. 10 that is optimized for $\delta = 0.12$.

floating stages is less than the dynamic range of the nonfloating stages.

The damage can be kept limited. The extra current sources produce noise, but the injected noise current is a common-mode current. If the circuits are designed in such a way that they are not or almost not susceptible to common-mode noise (as they usually are), the performance of the circuit is not degraded by this noise. These bias sources can thus be allowed to be quite noisy, so that only a small portion of the supply voltage is to be reserved for these sources. The deterioration of the dynamic range can therefore in principle be small, but there is a complication.

If the voltage drop over the extra bias current sources is small, the common-mode input range is also small. The common-mode signals should therefore be kept small, which can be accomplished by common-mode feedback [9], [11],–[14]. The loop gain of the common-mode feedback loop must be large enough so that common-mode stability is ensured even outside the nominal common-mode range. This can mean that the loop gain must be so high that common-mode stability can even be guaranteed for a nonfloating stage with this common-mode feedback circuit. This makes the usefulness of floating stages for high dynamic range filters doubtful.

VIII. Passive Admittances

Integrators that are realized with a passive-admittance part are shown in Fig. 1(a) and (b). It was explained in Section II that the use of a passive admittance in combination with a passive impedance is not practical. To realize an integrator with a pole (approximately) in the origin of the s-plane with a passive admittance, one should terminate the admittance by a low impedance. This can be done by realizing the impedance part actively, as shown in Fig. 1(b). Another way to realize a passive-admittance integrator is discussed in Section IX.

If the passive admittance is realized as a plain linear conductance, the input signal swing of the integrator can be arbitrary large, the input can even be driven beyond the supply voltages. In this case, the maximal signal level the integrator can handle is limited only at the output of the integrator. The noise factor of this conductance is 1. So concerning noise as well as maximal signal levels an active admittance will never behave better than a passive admittance, and therefore a passive admittance is favored.

In practical situations, the conductance is realized by an MOS transistor [4], as shown in Fig. 13, in order to realize tunability. If this is the case, the input range is limited by the gate voltage V_g of this transistor. If the transistor is to stay in the nonsaturated region, and assuming that we are dealing with an n-channel MOSFET, the input voltage should stay at least a threshold voltage below the gate voltage. Because the gate voltage is in practical cases less than the largest supply voltage, the threshold voltage must be negative to obtain a rail-to-rail input voltage range. So this transistor should be of the depletion type if an optimal dynamic range is to be obtained. We will assume that this is the case, or that rail-to-rail operation has been ensured in another way, if we are dealing with passive admittances.

Another advantage of using passive admittances is the possibility to eliminate $1/f$-noise. If MOSFET's are used as admittances, they usually produce a large amount of $1/f$-noise. The amount of this type of noise is dependent on the bias current of these devices [8]. If the bias current is zero, which can be realized with this type of integrator, the produced amount of $1/f$-noise is also zero. If the active impedance part of the integrator is also designed such that it produces little $1/f$-noise, an integrator with a low $1/f$-noise level can be constructed [12].

IX. Current Buffer

A drawback of many transadmittances is that the maximal input amplitude is dependent on the output signal. We saw this in Sections IV and VII. This problem can be overcome by adding a current buffer at the output of the stage. In a current buffer the output current must be measured and fed back to the input. Here, the same problem arises as with transadmittance stages. To measure the output current, a conductance must be placed in series with the output. If this conductance is large, it produces noise, and if it is small it limits the maximal output signal amplitude. The situation is even worse as with transadmittance stages, because the voltage over the measuring conductance must be converted to a current to be fed back to the input. For this purpose, a transadmittance stage that produces extra noise is needed. The conductance-transconductance combination produces noise and still are not enough to realize a transadmittance stage. The transadmittance stage that is to be connected to its input still has the unavoidable noise production of its own. Therefore, one can expect that with this kind of stage no net improvement of the dynamic range can be obtained. It can be proved that, even if the transadmittance stage at the input of the buffer is ideal with $\xi = 1$ and an infinite maximal input signal level, the maximal dynamic range that can be obtained in this way corresponds to a ζ of -4.4 dB.

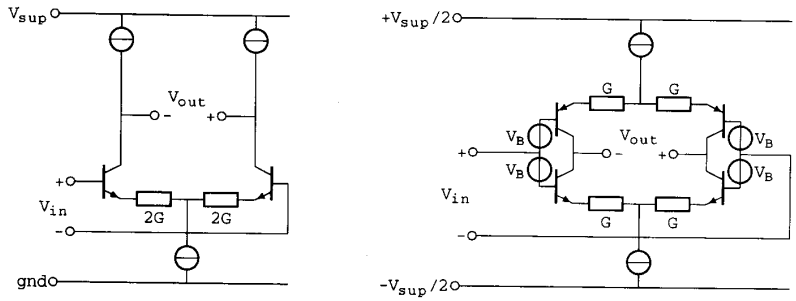

Fig. 12. Transadmittance stages of Figs. 8 and 9 made to float.

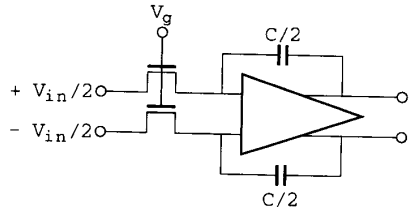

Fig. 13. In practical situations, a passive-admittance integrator is realized with a MOSFET as admittance part.

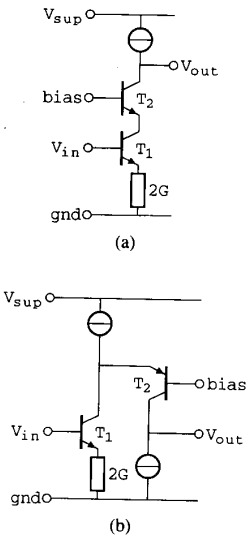

Fig. 14. Transadmittance stages with (a) a cascoded output and (b) a folded cascode output.

One might try to circumvent the problem of extra noise sources by applying *unity-gain non-energic feedback* [5]. This means that there are no *energic* elements, that is, elements that can dissipate or store energy, such as conductances, resistors, or capacitors, in the feedback circuit. This has an effect that the feedback circuit adds no extra noise to the signal. A daily-life example of a current buffer with non-energic feedback is a common-base or common-gate stage. Applying such a stage as an output stage for a transadmittance stage means that the transadmittance stage is cascoded. This is shown in Fig. 14(a). In this stage the noise production of the current buffer (T_2) is negligible, but it also imposes an extra limit to the maximal output signal amplitude, and thus it decreases the dynamic range.

This problem can be solved by applying a folded cascode stage, as shown in Fig. 14(b). In this way, adding the current buffer can increase the maximal output signal level, but extra bias current sources have to be added, so that the noise factor is increased. One of the extra current sources can be eliminated by making it active, as explained in Section VII. The stage is then realized as is shown in Fig. 15. In Fig. 15(a), the input stage is schematically depicted as a combination of two transadmittance stages. These can be realized passively, because the input impedance of the current buffer is low. It was shown in Section VIII that this gives rise to an optimal dynamic range. For the same reason, the bias current sources can be realized as plain conductances G_b, so that their noise production is minimized. This results in the circuit of Fig. 15(b).

The stage is optimized by finding an optimal value for G_b, implying an optimal value for the voltage drop V_b over this component. The larger this voltage drop, the less noise is produced, but the smaller the maximal output amplitude. An optimal value for G_b of $(1 + \sqrt{3})G$ is found, implying a noise factor of $2 + \sqrt{3}$ and a ζ of -4.5 dB.

As a conclusion we may say that applying a current buffer limits the attainable dynamic range below the optimum, and therefore this should not be done if a high dynamic range is wanted.

X. An Example Filter

In this section, the impact of the theories under consideration is demonstrated with the design of a fifth-order Butterworth low-pass filter. This will result in a filter with a dynamic range that is close to the fundamental maximum.

As a starting point we use an excellent filter design by Jaap van der Plas [12]. A schematic diagram of this filter is shown in Fig. 16. This filter consists of a first-order prefilter, followed by a fourth-order complementary ladder filter. It contains five balanced opamps, the schematic

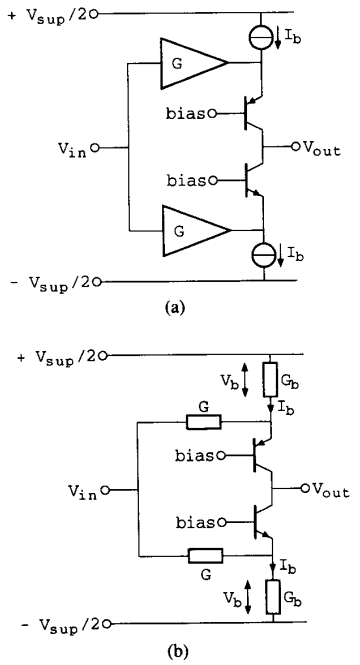

Fig. 15. Models for a folded cascode stage.

of which is given in Fig. 17. This op-amp is a two-stage op-amp with common-mode feedback. The filter and the op-amp have been designed such as to minimize the $1/f$-noise corner frequency of the filter to a value of 250 Hz [12]. The -3-dB cutoff frequency of the filter is 3-kHz nominally, and can be adjusted via the control voltage V_c in Fig. 16, which has a nominal value of 6.5 V. The values of C_1 to C_5 are 99 pF, 110 pF, 176 pF, 110 pF, and 44 pF, respectively. The MOSFET's in this figure all have an aspect ratio of 2.5/90. The filter can be viewed as a network of five integrators of the passive-admittance active-impedance type shown in Fig. 13. In Section 5.2, we found that this type of integrator can approach the fundamental dynamic-range maximum if they have a rail-to-rail input and output, and if their noise factor approaches unity. Therefore, this filter is a good starting point for redesigning it into a close-to-optimal filter.

If the total broad-band noise output voltage (excluding $1/f$-noise) of the configuration of Fig. 16 is determined, a value of 28 μV is found, if the noise production of the opamps is excluded. Measurements [12], as well as SPICE simulations of this circuit show a total output noise voltage of 31 μV. This shows that the integrators have a low noise factor of only 1.23, or 0.9 dB. This is quite acceptable.

Fig. 18 shows the dc transfer curve of this filter. This plot shows a linear behavior up to a differential output voltage of 4.2 V. This corresponds to a maximal root-mean-square output voltage of 3.0 V for sinusoidal signals at very low frequencies. At higher frequencies in the passband, the signal-handling capability decreases somewhat. This is shown by transient simulations. Measurements [12] show a maximal rms output signal level of 2.5 V for 0.3% distortion. Together with the noise level of 31 μV, this results in a dynamic range of 98 dB.

The signal-handling capabilities of this filter can be improved by increasing the gate overdrive voltages $V_{gs} - V_t$ of the transistors in Fig. 16. One way of doing this is decreasing the threshold voltage of these transistors, that is, according to Section VIII, one should use depletion transistors. If these are not available, rail-to-rail signal-handling properties can be obtained by lifting the gate voltages of these transistors above the supply voltages. For this purpose, an on-chip voltage multiplier [15] must be available. We assume that this is the case, and that the gate voltage of the transistors in Fig. 16 is 12 V. The aspect ratio of these transistors was changed into 2.5/400 to retain the same cutoff frequency. The output signal handling capacity of the opamp also needed to be enlarged. This was done by increasing the aspect ratio W/L of the transistors P_7 to P_{11} by a factor four. By simulations, the ac transfer function was unaltered after these modifications. Fig. 19 shows the dc transfer curve that was obtained in this way. The maximal output votlage now is 7.4 V. This comes very close to rail-to-rail operation, and corresponds to a maximal root-mean-square output voltage of 5.2 V, which has been confirmed by a transient analysis at 1 kHz. The noise output voltage of the filter had not changed. In this way, the dynamic range of the filter has been improved to 104.5 dB. This is the largest dynamic range of an integrated filter that has ever been reported. For continuous-time integrated filters, reported values range from 55 dB [16] for an application in which a high dynamic range is not required to 100 dB [17]. The latter filter is comparable to the filter that has been discussed here; it is a fifth-order low-pass filter with similar integrators. It also has comparable limits regarding supply voltage and capacitance. This also shows that the passive-admittance active-impedance integrator can be used to yield an optimal dynamic range.

10.1. Further Improvements

The integrator has a noise factor of 1.23, and a maximal output signal amplitude of 7.4 V. An optimal integrator would have unity noise factor, and a maximal output amplitude equal to the supply voltage, which is 8 V. Therefore, this integrator has a ζ of $(7.4/8)^2/1.23$, or -1.6 dB. The dynamic range of the filter can be improved by this amount by lowering the noise factor of the op-amp, or by enhancing its signal-handling capacity. The former is possible by enlarging transistors P_1 to P_6 of the op-amp, and the latter by furnishing the op-amp with a push-pull output stage.

Further improvements are possible by optimizing the filter network. For this particular filter, a first-order prefilter, followed by a fourth-order ladder network has been chosen. It can be proved that, if a properly scaled fifth-order ladder filter is used, with an optimal division of the total available capacitance over the five integrators, a

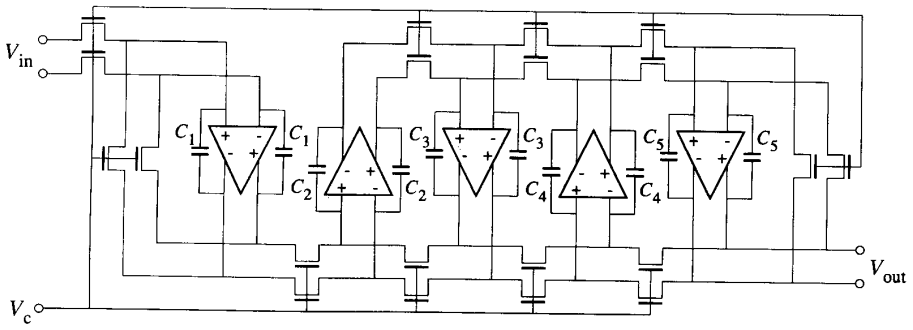

Fig. 16. A fifth-order low-pass filter.

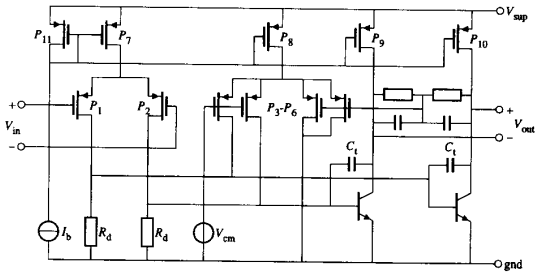

Fig. 17. A balanced op-amp to be used for the filter of Fig. 16.

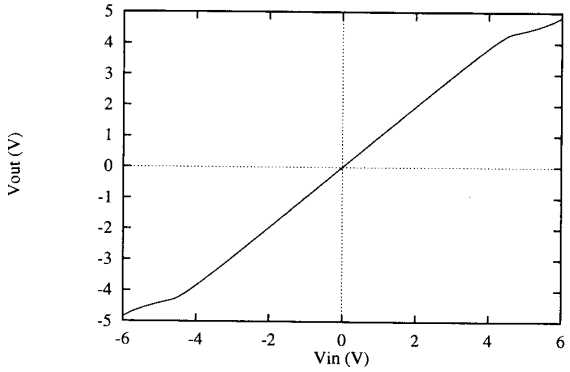

Fig. 18. The dc transfer curve of the filter of Fig. 16.

dynamic-range improvement of 1.7 dB is obtained. Further network optimization is possible, the methods for which are beyond the scope of this paper. If a numerical network optimization is performed, [18] and the capacitance is divided optimally, a dynamic-range improvement of 4 dB is obtained. If all the optimizations of this section are applied, a dynamic range of 110 dB is obtained. This is a fundamental limit to the dynamic range of a fifth-order Butterworth low-pass filter with a supply voltage of 8 V and a total capacitance of 1.078 nF.

XI. Summary and Conclusions

There are many ways to realize integrated integrators. By classification, from all possible integrator configurations, a dynamic-range optimal integrator can be found.

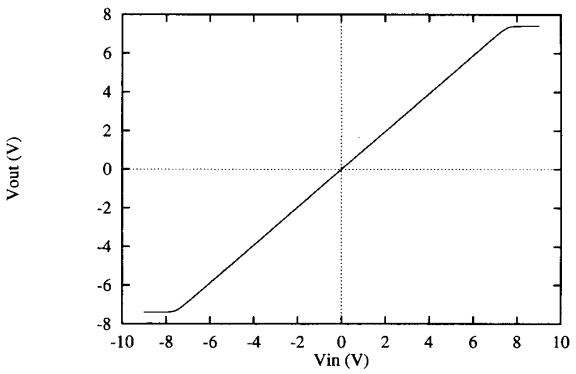

Fig. 19. The dc transfer curve of the filter after improving the signal-handling capacity of the integrators.

The most practical choice for an optimal integrator is an admittance-transimpedance integrator. This type of integrator is usually implemented and known as a MOSFET-C integrator [4], such as shown in Fig. 13. The op-amp that is used should also be designed optimally. An especially attractive property of this type of filter is that it can be constructed such that it has a very low level of $1/f$-noise.

Other optimal integrators, important from a more theoretical point of view, are formed with the transadmittance-impedance stages of Figs. 5 and 9(a) (in class B), in a differential configuration as shown in Fig. 4.

Second best is the integrator based on a triode transconductor, as the one shown in Fig. 10. Its optimal dynamic range is only 1.5 dB below the optimum. It has the advantages above other integrators that it has a very large tuning range, and that it is simple, in the sense that a small amount of components and chip area is needed.

These optimal and nearly optimal integrators conform to two general rules which we derived, namely that transadmittance stages that are floating, and those that have a separate output stage, should not be used when an optimal dynamic range is wanted.

To reach the optimal dynamic range, in most of the cases mentioned here, the MOSFET's that are used should be especially designed for this goal. Specifically, the

threshold voltage must be optimized, which in some of the above mentioned cases means that it must be negative (assuming the use of n-channel devices). This for instance means that the MOSFET-C integrator of Fig. 13 must be realized with depletion-MOSFET's in its admittance part. This can be circumvented by using an on-chip voltage multiplier to lift the gates of these transistors above the supply voltage. The effectiveness of this approach has been demonstrated by redesigning a fifth-order Butterworth low-pass filter in such a way, that its dynamic range has been improved to 5.5 dB below a fundamental maximum. Of the 5.5-dB improvement that can be obtained, 1.6 dB is still due to the integrators.

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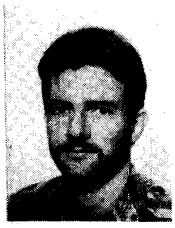

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