Optimal Emitter Cell Geometry in High Power 4H-SiC BJTs

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***Abstract*— Three 4H-SiC BJT designs with different emitter cell geometries (linear interdigitated fingers, square cell geometry, and hexagon cell geometry) are fabricated, analyzed, and compared with respect to current gain, on-resistance, current density, and temperature performance for the first time. Emitter size effect and surface recombination are investigated. Due to a better utilization of the base area, optimal emitter cell geometry significantly increases the current density (J_C) about 42% and reduces the on-resistance (R_{ON}) about 21% at a given current gain, thus making the device more efficient for high-power and high-temperature applications.**

***Index Terms*—Power 4H-SiC BJTs, current density, current gain, on-resistance, surface recombination.**

I. Introduction

SILICON carbide bipolar junction transistors (BJTs) with high current density (J_C) and low on-resistance (R_{ON}) are attractive candidates for power switching due to the absence of a critical gate oxide, fast switching speed, and low loss [1]. However, to completely compete with metal oxide semiconductor field effect transistors (MOSFETs) and insulated gate bipolar transistors (IGBTs), it is important to improve the BJT characteristics. In recent years, there has been considerable interest to improve the breakdown voltage, maximum current gain (β) and J_C, meanwhile, decreasing the R_{ON} [2]-[12]. The progress has been achieved by using continuous epitaxial growth [9], optimized device geometry [10], and improved surface passivation [11], [12]. All 4H-SiC BJTs; hitherto, employ the linear interdigitated fingers to diminish the current crowding at the edge of the emitter. These geometries mostly have an emitter width (W_E) up to 20 µm.

In this work, we report a significant improvement in the J_C and R_{ON} at a given β by utilizing optimal emitter cell geometry. We compare the β, J_C, and R_{ON} in three different SiC BJT geometrical designs with a stable open-base breakdown voltage of 5.65 kV as reported in [4]. The first and reference design uses linear interdigitated fingers, whereas the second and third designs, to the authors' knowledge, square and hexagon cell geometries are investigated for the first time for BJTs, which opens a new design space for improved performance. The emitter size effect, the effect of surface recombination, and also the temperature dependency are investigated for all designs.

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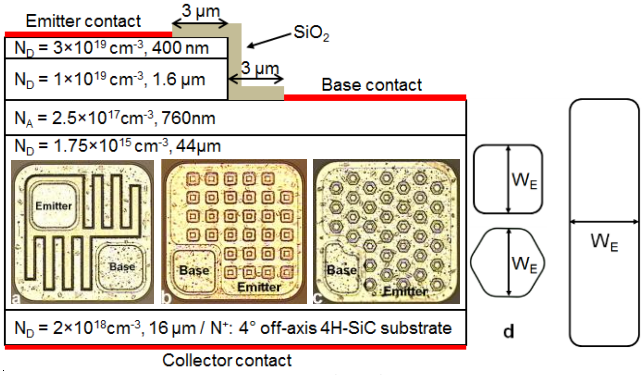

Fig. 1. Schematic cross-sectional view of the fabricated 4H-SiC BJTs. (Inset) Micrograph top views of the fabricated BJTs with a W_E = 20 µm and different cell geometries: (a) linear interdigitated fingers, (b) square cell geometry, (c) hexagon cell geometry. (d) Schematic top view of one cell for different cell geometries.

II. Device Fabrication

Fig. 1 shows a cross-sectional view of the fabricated BJTs with five epitaxial layers grown in one continuous run on a 100-mm 4° off-axis 4H-SiC substrate. The emitter epilayer is 1.6 µm nitrogen doped to 1×10^{19} cm^{-3}, capped by 400-nm-thick 3×10^{19} cm^{-3} to obtain optimum injection efficiency and low-resistive ohmic contact, respectively. The base layer is 760 nm aluminum doped to 2.5×10^{17} cm^{-3}. The drift layer is 44 µm thick and nitrogen doped to 1.75×10^{15} cm^{-3}. Inductively coupled plasma (ICP) etching with an oxide mask was utilized to form the emitter mesa. Reactive ion etching (RIE) with a photoresist mask was used to form the base mesa. A dry sacrificial oxidation at 1100 °C for 1 hour was employed to have the best performance according to [13]. To minimize the interface charges at SiO_2/SiC interface, a surface passivation was deposited with 50-nm PECVD SiO_2 followed by post oxide annealing in N_2O ambient at 1100 °C for 3 hours according to [12]. A 110-nm and 140-nm Ni layer was deposited for emitter and collector contacts respectively, followed by rapid thermal annealing (RTA) at 950 °C for 1 min in Ar ambient to form the ohmic n-contact. A 110-nm stack layer of Ni/Ti/Al with the thickness of 10/15/85 nm was deposited for base p-contacts followed by RTA at 815 °C for 2 min in N_2 ambient. The emitter and base contact resistivities were extracted to 1.4×10^{-5} Ω.cm^2 and 1.5×10^{-4} Ω.cm^2

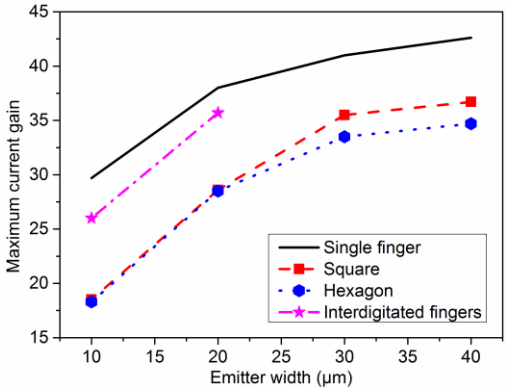

Fig. 2. Maximum current gain for different emitter widths and cell geometries.

respectively, utilizing the TLM structures. Two Al layers were sputtered for current spreading and connecting the linear interdigitated fingers, hexagon and square cells.

The hexagon and square cells have different emitter widths W_E, i.e., 10, 20, 30, and 40 μm. Moreover, two different sets of the finger cell geometries have been fabricated. The first has a single finger cell with an emitter length of 500 μm and different emitter widths W_E, i.e., 10, 20, 30, and 40 μm; the second has interdigitated fingers with a W_E of 10 and 20 μm. The optimum distance between the emitter mesa and base contacts (3 μm) for all cell geometries, was chosen to obtain the maximum value of β according to [14].

III. Results and Discussion

Fig. 2 shows the emitter size effect on β for the different designs. The β is decreasing as the W_E reduces below 40 μm for all emitter cell geometries. The wider emitter (> 40 μm) does not result in higher current gain due to the saturation behavior discussed in [15]. It also shows that the finger design has the highest current gain, because of the smallest emitter periphery over area (P_E/A_E) ratio. Decreasing of this ratio lowers the surface recombination as discussed in [2], [16] - [18]. The effect of surface recombination on the current gain can be expressed as in [18]:

$$\frac{J_C}{\beta} = \left(J_{Bulk} + J_{Scr} + J_{Inj}\right) + K_{b,surf}\frac{P_E}{A_E} \quad (1)$$

where, J_{bulk}, J_{Scr}, and J_{Inj} are the bulk recombination, space-charge recombination, and base-emitter back-injection, respectively. $K_{b,surf} \times P_E$ is the emitter periphery recombination current, and $K_{b,surf}$ (A/cm) is the normalized surface recombination current. Fig. 3 represents the J_C/β as a function of P_E/A_E ratio for square cell geometry as an example. The $K_{b,surf}$ can be calculated by the slope of the lines. It is apparent that the $K_{b,surf}$ increases as the J_C increases due to emitter current crowding, resulting in a decline of the β. All geometries show this behavior as the square cell geometry. The extracted $K_{b,surf}$ are shown in Fig. 4 for all cell geometries. Although the hexagon and square cell geometries have higher $K_{b,surf}$ values leading to a lower β in Fig. 2, these cell geometries can result in higher J_C and lower R_{ON} due to a better utilization of the base area.

There has always been a difference between the estimated values of J_C and R_{ON} for the small- and large-area devices.

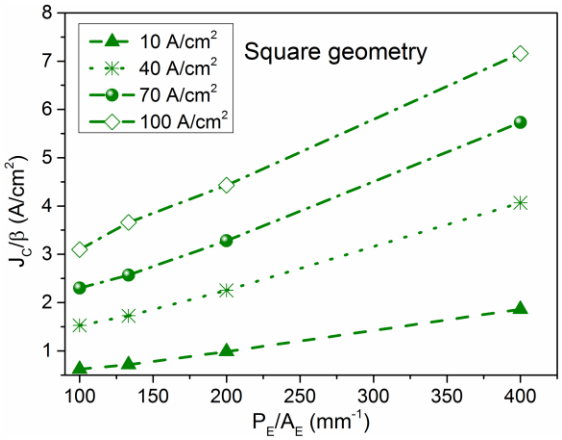

Fig. 3. Emitter size effect for different current densities. W_E varies from 10 to 40 μm. The slope in the graph is the $K_{b,surf}$.

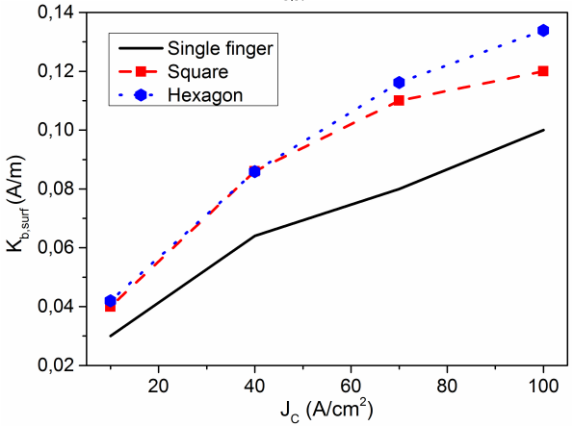

Fig. 4. Normalized periphery surface recombination current as a function of J_C for different cell geometries.

TABLE I. Calculated Active Area for All Cell Geometries.

Emitter width (μm)	Interdigitated fingers (×10⁻³ mm²)	Square (×10⁻³ mm²)	Hexagon (×10⁻³ mm²)
10	96	92	86
20	113	84	82
30	---	82	80
40	---	80	78

Therefore, to precisely estimate the J_C and R_{ON}, an actual value for active area is needed. The active areas were calculated by considering two aspects; Firstly, the current flow in the thick collector layer which was simulated by Sentaurus TCAD. Secondly, the calculation method based on the simulation results were applied to the previous fabricated BJTs [19], [20], and a good agreement was achieved for the R_{ON} and J_C of the small- and large- area BJTs. Table I shows the calculated active area for all cell geometries with different emitter widths.

Fig. 5 and 6 illustrate the J_C (at the maximum current gain) and R_{ON} (at collector current I_C = 0.1 A) for all cell geometries with different emitter widths as a function of β. At the maximum current gain (~35), about 42% higher J_C and about 21% lower R_{ON} was resulted for the hexagon cell geometry, and about 21% higher J_C and about 23% lower R_{ON} was resulted for the square cell geometry compared to the linear interdigitated finger geometry. It can be concluded that at a given β, the hexagon and square cell geometries are more suited for high-power SiC BJTs in order to obtain a higher J_C and a lower R_{ON}.

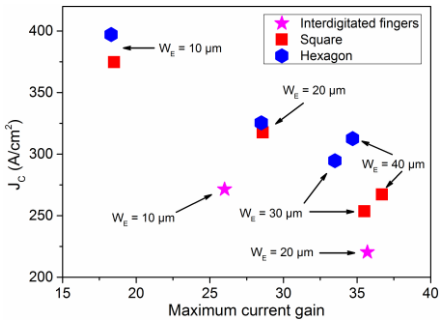

Fig. 5. Collector current density as a function of maximum current gain for the fabricated BJTs with different cell geometries.

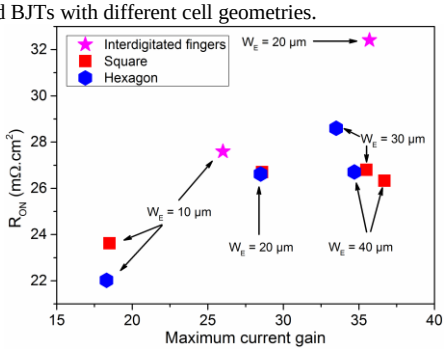

Fig. 6. On-resistance as a function of maximum current gain for the fabricated BJTs with different cell geometries.

Fig. 7 shows the high temperature performance of the different fabricated BJTs with a W_E = 40 µm. All cell geometries show a negative temperature dependence of the β with the same trend because of increasing acceptor ionization, resulting in reduction of the emitter efficiency. This trend is in a good agreement with the modeling in [21].

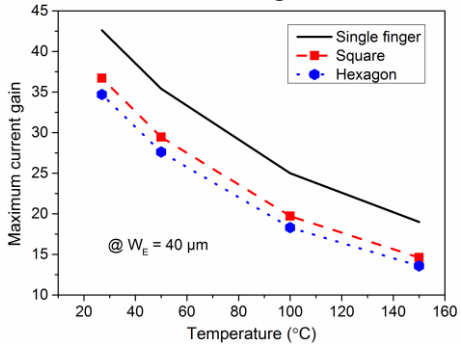

Fig. 7. Temperature dependency of the β for the different fabricated BJT cell geometries.

IV. Conclusion

The influence of the cell geometrical design on the three fabricated 4H-SiC BJTs (linear interdigitated fingers, square cell geometry, and hexagon cell geometry) on the maximum current gain (β), current density (J_C), and on-resistance (R_{ON}) has been compared. All cell geometries showed a negative temperature dependence of the β with the same trend. The emitter size effect played a key role in determining the β for all designs. The linear interdigitated fingers showed the highest β, due to a lower periphery over area P_E/A_E ratio and consequently a lower surface recombination. However, at a given current gain, about 42% higher J_C and about 21% lower R_{ON} was seen for the hexagon cell geometry, and about 21% higher J_C and about 23% lower R_{ON} was observed for the square cell geometry in comparison to the traditional linear interdigitated finger geometry due to a better utilization of the base area. This significant improvement in the J_C and R_{ON} makes the device more suited for high-power and high-temperature applications.

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