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Optimal Neutral Point Voltage Balancing Algorithm for Three-phase Three-level Converters with Hybrid Zero-sequence Signal Injection and Virtual Zero-level Modulation

Jun Wang, *Member, IEEE*, Xibo Yuan, *Senior Member, IEEE,* Kfir J. Dagan and Andrew Bloor

***Abstract*—This paper presents an optimal carrier-based voltage balancing scheme for three-phase, three-level converters. The proposed scheme utilizes two available degrees of freedom, i.e. Zero-sequence Signal Injection (ZSI) and Virtual Zero-level Modulation (VZM), to eliminate the low-frequency neutral point voltage oscillation. It is universally effective over the full power factor and modulation index range and easy to implement in digital controllers. The hybrid algorithm combines the merits of both approaches, which offers the optimal performance regarding controllability, switching device power losses and output harmonics. The main drawbacks of VZM, i.e. the increased switching loss and high-frequency harmonics due to additional switching transitions, have been minimized in the proposed scheme. The performance of the proposed scheme is evaluated through simulation and experiment.**

***Index Terms*—DC-AC power converters, three level converters, voltage balancing, Pulse Width Modulation**

I. Introduction

THREE-LEVEL converters, such as three-level Neutral Point Clamped [1] and T-type [2] converters, have drawn increased attention in recent years for medium-voltage or low-voltage applications. As one of the inherent issue of three-level converters, the Neutral Point (NP) voltage balancing has been a hot research topic [3]–[13]. There are mainly two known modulation-based approaches to suppress the NP voltage oscillation while avoiding bulky low-frequency filtering capacitors. One is the Zero-sequence Signal Injection (ZSI) approach [5], [10], [14], which has been widely accepted and implemented. However, according to [5], [7], [10], [14], this approach is unable to completely remove the NP voltage oscillation when the converter operates at high modulation indexes and low power factors. This limitation becomes problematic for certain applications, such as Static Synchronous Compensators (STATCOM) since they mainly operate at low power factors. The other approach is the Virtual Zero-level Modulation (VZM) [15] which utilizes redundant voltage levels in each switching window. The VZM is effective in eliminating the low frequency oscillations at low power factors and high modulation indexes. With regard to utilizing the redundant voltage level, VZM is equivalent to the Nearest Three Virtual Vector (NTV^2) modulation [4], [8], Partial Bipolar PWM (PDPWM) [16], Disassembly of Zero Level [13], Double Signal PWM (DSPWM) [17], and the modulation strategies in [9], [12]. However, the main drawback of this technique is introducing extra switching events, which leads to significantly increased switching loss of the switching devices [9], [15]. Therefore, it is undesirable to activate VZM constantly, especially when ZSI is capable already to balance the NP voltage in certain cases.

Hence, this paper proposes a novel carrier-based voltage balancing scheme, an optimal combination of ZSI and VZM, which is effective over the whole operating range of the power converter. To fully utilize these two degrees of freedom, a logic coordinating the use of VZM and ZSI is developed. To minimize the main drawback of VZM, i.e. the increased switching loss and high-frequency output harmonics, VZM is activated only when necessary. The introduction and preliminary results of this work have been presented in [18].

The main contribution of this paper is the proposed hybrid voltage balancing algorithm that offers the optimal performance regarding switching loss and output harmonics while eliminating the low-frequency NP oscillation over the full operating range. The main idea of this hybrid approach is combining the merits of the two available degrees of freedom, ZSI and VZM, to gain the maximum controllability and moderate the negative side effects. The proposed voltage balancing scheme features the following merits:

(a) Closed-loop precise control of the NP potential on carrier cycle basis
(b) Elimination of the low-frequency NP voltage oscillation over the full converter operating range with regards to power factors ($\cos\varphi = 0 \sim 1$) and modulation indexes ($M = 0 \sim 1.15$)
(c) No reduction of converter output voltage/capacity at any operating point
(d) No PI/PID controllers involved, which simplifies parameter tuning and prototyping process
(e) Simple implementation with level-shifted carriers

In the following paper, an introduction of the two existing approaches, ZSI and VZM, is presented regarding their principles and implementations. The ZSI approach is based on the existing approach [19], which performs iterations to find the optimal zero-sequence signal for voltage balancing purpose.

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The VZM approach is a simplified algorithm based on the modulation strategy presented in [12]. A hybrid approach is then proposed and compared with representative existing approaches. An evaluation of the controllability, voltage ripple amplitude and output harmonic content are conducted across various voltage balancing schemes to compare their performances. Finally, experimental results are presented.

II. Neutral Point Voltage Balancing

A. Three-phase three-level converter and neutral point voltage oscillation

This section introduces the NP voltage oscillation issue of a three-phase, three-level converter. As an example, a three-phase, three-level T-type converter is shown in Fig. 1.

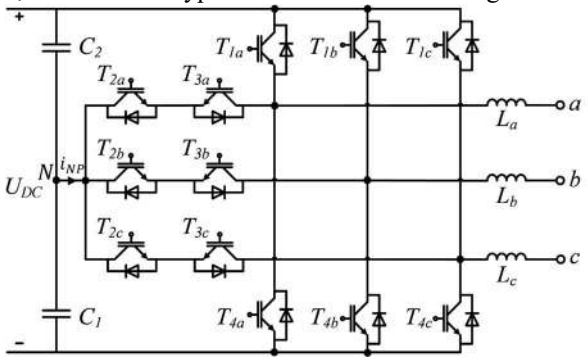


Fig. 1. Three-phase three-level T-type converter topology

A three-level converter outputs three voltage levels: positive DC rail (+1), neutral point voltage (0) and negative DC rail (−1). With conventional Sinusoidal Pulse Width Modulation (SPWM), the output voltage in each switching window is synthesised by only two voltage levels: +1/0 when the reference voltage is positive; −1/0 when the reference voltage is negative. The mathematical model of the converter is expressed in (1) and (2), where $U_{a,b,c}$ are the phase reference voltages; $I_{a,b,c}$ are the load currents; θ is the phase angle; M is the modulation index; φ is the power factor angle (lagging) and I_m is the amplitude of load currents.

$$\begin{cases} U_a = M \cdot \sin\theta \\ U_b = M \cdot \sin(\theta - \frac{2}{3}\pi) \\ U_c = M \cdot \sin(\theta + \frac{2}{3}\pi) \end{cases} \quad (1)$$

$$\begin{cases} I_a = I_m \sin(\theta - \varphi) \\ I_b = I_m \sin(\theta - \frac{2}{3}\pi - \varphi) \\ I_c = I_m \sin(\theta + \frac{2}{3}\pi - \varphi) \end{cases} \quad (2)$$

Assuming the switching frequency is much higher than the fundamental frequency, the reference voltage can be treated as constant in each switching window. The duty ratios of phase x ($x = a, b, c$) can be calculated from the normalised reference voltage as expressed in (3)-(5), where $D_{+1\text{-}x}$ is the duty ratio of state +1, $D_{-1\text{-}x}$ is the duty ratio of state −1, and $D_{NP\text{-}x}$ is the duty ratio of state 0.

$$D_{+1-x} = \begin{cases} U_x, if\ U_x > 0 \\ 0, if\ U_x \le 0 \end{cases} \quad (3)$$

$$D_{-1-x} = \begin{cases} -U_x, if\ U_x < 0 \\ 0, if\ U_x \ge 0 \end{cases} \quad (4)$$

$$D_{NP-x} = 1 - D_{+1x} - D_{-1x} = 1 - |U_x| \quad (5)$$

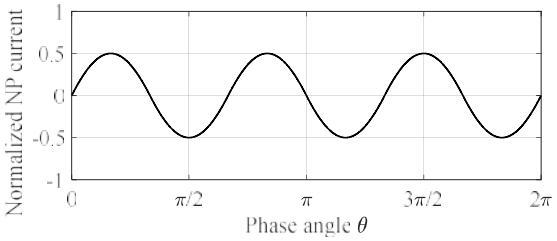
Then, the average NP current over one switching period can be expressed as (6), which is contributed from three phases, where $i_{a,b,c}$ are measured load currents. The positive reference direction of i_{NP} is defined as flowing out from the neutral point.

$$i_{NP} = i_a D_{NP-a} + i_b D_{NP-b} + i_c D_{NP-c} \quad (6)$$

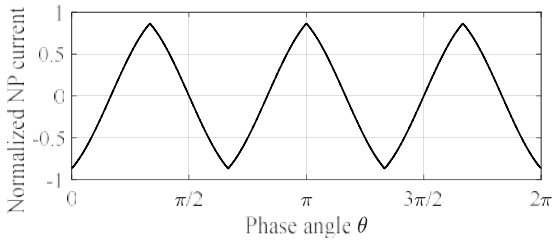
Substituting (1)(2)(5) into (6), the analytical expression of NP current from the fundamental frequency point of view can be derived as (7) as a function of the phase angle θ.

$$i_{NP}(\theta) = I_m \begin{bmatrix} \sin(\varphi - \theta)\left(|M\sin(\theta)| - 1\right) \\ +\sin\left(\varphi - \theta + \frac{2}{3}\pi\right)\left(\left|M\sin\left(\theta - \frac{2}{3}\pi\right)\right| - 1\right) \\ -\sin\left(\theta - \varphi + \frac{2}{3}\pi\right)\left(\left|M\sin\left(\theta + \frac{2}{3}\pi\right)\right| - 1\right) \end{bmatrix} \quad (7)$$

Plotted from (7), Fig. 2 illustrate the uncontrolled NP current over a fundamental cycle, with the amplitude normalized to the peak load current. Two observations can be made in the plot: (1) the NP current is in the frequency of three times the fundamental frequency (2) the amplitudes of the NP current are 0.50 and 0.87 in Fig. 2(a) and Fig. 2(b) respectively, which indicates that the NP voltage oscillation is more severe in the case of a low power factor.



(a) M = 1, φ = 0°



(b) M = 1, φ = 90°

Fig. 2. Analytically derived neutral point current normalized to peak load current

From the NP current point of view, the two capacitors are virtually in parallel [6]. The deviation of NP voltage Δu_{NP} over a period of time T is determined by i_{NP} and the DC-link capacitances as expressed in (8), assuming two identical capacitors ($C = C1 = C2$).

$$\Delta u_{NP} = \frac{i_{NP} \cdot T}{2C} \quad (8)$$

To balance the NP voltage, a desired NP current i^*_{NP} in one switching cycle is calculated through (9). The ΔU_{NP} is the measured, signed deviation of NP voltage referenced to half the DC-link voltage, i.e. $U_{C1}-(U_{C1}+U_{C2})/2$; f_{sw} is the switching frequency; C is the capacitance of each capacitors.

$$i^*_{NP} = \Delta U_{NP} \cdot f_{sw} \cdot 2C \quad (9)$$

To balance the capacitor voltages, the NP current needs to be manipulated to track the desired value. To achieve this goal, there are two degrees of freedom that can be utilized in modulation, which are the Zero-sequence Signal Injection (ZSI) and the Virtual Zero-level Modulation (VZM).

B. Zero-sequence Signal Injection (ZSI)

In a three-phase converter, the injection of zero-sequence signal is one degree of freedom to suppress the NP voltage oscillation. It is realized by adding a zero-sequence component to the reference voltages of three phases at the same time, as expressed in (10). The injected zero-sequence signal will be cancelled out and not show in the line-to-line voltages.

$$\begin{cases} U_{a-ZSI} = U_a + U_{ZSI} \\ U_{b-ZSI} = U_b + U_{ZSI} \\ U_{c-ZSI} = U_c + U_{ZSI} \end{cases} \tag{10}$$

The allowable range of U_{VZI} is constrained by keeping the modified reference voltages $U_{a\text{-}ZSI}$, $U_{b\text{-}ZSI}$ and $U_{c\text{-}ZSI}$ within the linear modulation range ($|U| \leq 1$). Therefore, the upper and lower boundaries of U_{VZI} [$U_{ZSI\text{-}low}$, $U_{ZSI\text{-}up}$] are found by (11).

$$\begin{aligned} U_{ZSI-up} &= 1 - \max(U_a, U_b, U_c) \\ U_{ZSI-low} &= -1 - \min(U_a, U_b, U_c) \end{aligned} \tag{11}$$

The effect of the zero-sequence signal U_{ZSI} regarding the neutral point voltage/current is not straightforward [19], as it changes $D_{NP\text{-}a}$, $D_{NP\text{-}b}$ and $D_{NP\text{-}c}$ in (6) all at the same time. Therefore, an iterative approach to find the optimal U_{VZI} for the balancing is illustrated in Fig. 3, based on the approach presented in [19]. In each switching cycle, this approach performs trials (iterations) to search the optimal U_{VZI} that is within the allowable range (11) and pulls the NP current towards the desired value i^*_{NP}. The searching iterations are performed with a fixed step, for which the selected U_{VZI} can be considered optimal when the step size is sufficiently small.

At the end of the algorithm, the selected optimal U_{VZI} is injected through (10) to take effect in balancing the NP voltage. As the main constrain of ZSI, (11) limits the usable margin of U_{VZI}, which is mostly narrowed when one phase voltage reaches its peak. As a result, a limited balancing performance is observed in ZSI, which will be demonstrated in Section IV.

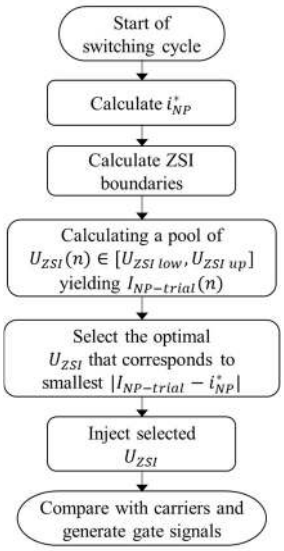


Fig. 3. Block diagram of the ZSI based voltage balancing algorithm

C. Virtual Zero-level Modulation (VZM)

As the other degree of freedom, the controllability of NP current can be gained by introducing an additional voltage level, which alters the NP duty ratios $D_{NP\text{-}x}$ in (6). In one switching window, this approach replaces part of the output zero-level voltage with "virtual zero level" synthesized by "+1" and "−1", which is illustrated as u_{xo} shown in Fig. 4. Therefore, this approach is referred as Virtual Zero-level Modulation. It can be seen that, from Fig. 4(a) to Fig. 4(b), the D_{NP} is effectively reduced to D'_{NP}. Note the volt-time products of the output voltage u_{xo} in Fig. 4(a) and Fig. 4(b) are equal, which means the VZM does not affect the synthesized low-frequency output voltage. This approach will double the switching transitions in one switching window, i.e. four instead of two. By adjusting the duration of the replaced zero-level, the precise control of the NP duty ratio D'_{NP} can be achieved. It should be highlighted that the modified D'_{NP} can only be smaller than the original NP duty ratio D_{NP} to avoid undermining the output voltage amplitude. Subsequently, VZM can only reduce one phase's contribution of NP current, i.e. one term $D_{NP\text{-}x}I_x$ in (6).

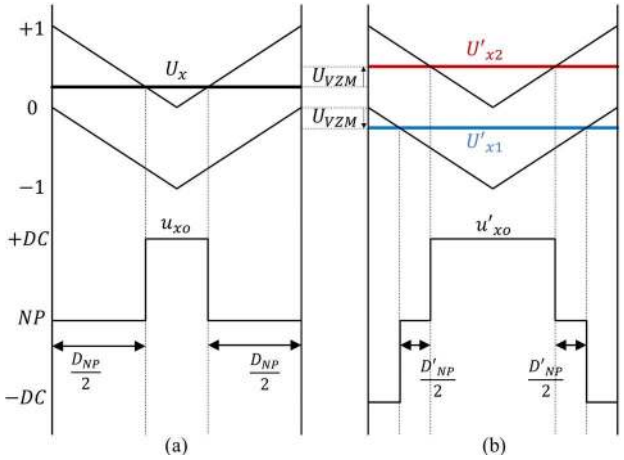


Fig. 4. Illustration of level-shifted-carrier modulation and converter output voltage u_o when reference voltage $U_x > 0$ (a) SPWM (b) VZM

The VZM can be realized in various modulation schemes. This paper demonstrates the implementation of VZM with level-shifted carriers due to its simplicity. The additional voltage level is introduced by split and alter the modulating waves, which is similar to the DSPWM [17]. Firstly, the original sinusoidal modulating wave (Fig. 5(a)) is split into two parts, U_{x2} and U_{x1}, through (12). The split modulating waves shown in Fig. 5(b) is still equivalent to the original sinusoidal waves in the modulation.

$$U_{x2} = \begin{cases} U_x, \ if \ U_x > 0 \\ 0, \ if \ U_x \leq 0 \end{cases} \text{ and } U_{x1} = \begin{cases} 0, \ if \ U_x > 0 \\ U_x, \ if \ U_x \leq 0 \end{cases} \tag{12}$$

The second step is to "space away" the two modulating waves through (14), which will result in an additional output voltage level as shown in Fig. 4(b). This step changes the duty ratios of the altered phase without changing the total voltage-time product of the switching window. Based on the target $D'_{NP\text{-}x}$, a offset value $U_{VZM} > 0$ can be calculated through (13), which is derived from the geometrical relationship in Fig. 4(b).

$$U_{VZM} = (D_{NP-x} - D'_{NP-x})/2 \tag{13}$$

The calculated offset value U_{VZM} is then injected through (14) to "space away" the two split modulating waves.

$$U'_{x2} = U_{x2} + U_{VZM}$$
$$U'_{x1} = U_{x1} - U_{VZM} \quad (14)$$

At this point, the VZM is realized through the above series of numerical and logical operations, which modifies the D_{NP} to the target D'_{NP}.

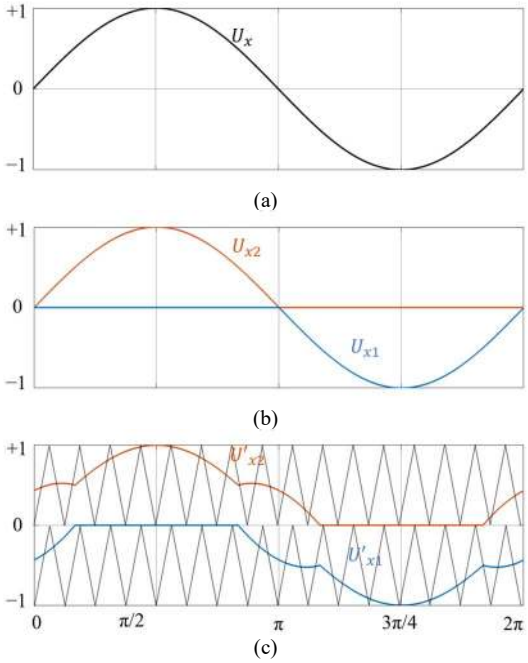


Fig. 5. Implementation of VZM with split modulation wave method ($M = 1$) (a) original sinusoidal wave (b) split waves (c) altered split waves with U_{VZM} injected and level-shifted carriers

D. VZM based voltage balancing scheme

The scheme using VZM to balance the NP voltage is shown in Fig. 6. As proved in [12], only one phase leg needs to activate VZM to eliminate the low-frequency NP oscillation in a three-phase three-level converter. This one phase is referred as the dominant phase y, which is selected out from the three phases x ($x = a,b,c$). To find the dominant phase y, a selection logic is required as shown in Fig. 6, which is a simplified logic based on the approach in [12]. When the aim is to increase the NP current ($I_{NP}^* > I_{NP}$), the $I_yD_{NP\text{-}y}$ of the dominant phase with the most negative contribution in (6) will be reduced by VZM. Vice versa, when the aim is to decrease the NP current ($I_{NP}^* < I_{NP}$), VZM undermines the $I_yD_{NP\text{-}y}$ of the dominant phase with the most positive contribution.

To force the NP current to track the desired value i^*_{NP}, the desired duty ratio D^*_{NP} is calculated through (15).

$$D^*_{NP-y} = \left[i^*_{NP} - (i_{NP} - i_y D_{NP-y})\right]/i_y \quad (15)$$

Note the desired D^*_{NP} can be unfeasible because it attempts to pull back the NP voltage deviation in one switching cycle. Therefore, D^*_{NP} must be "trimmed" into a feasible D'_{NP}, as shown in Fig. 6, to avoid modulation errors. The feasible boundaries of D'_{NP} are given in (16), which ensures the volt-time area in the switching window unaffected and the modified reference voltage to remain in the linear modulation range.

$$0 \le D'_{NP} < D_{NP} \quad (16)$$

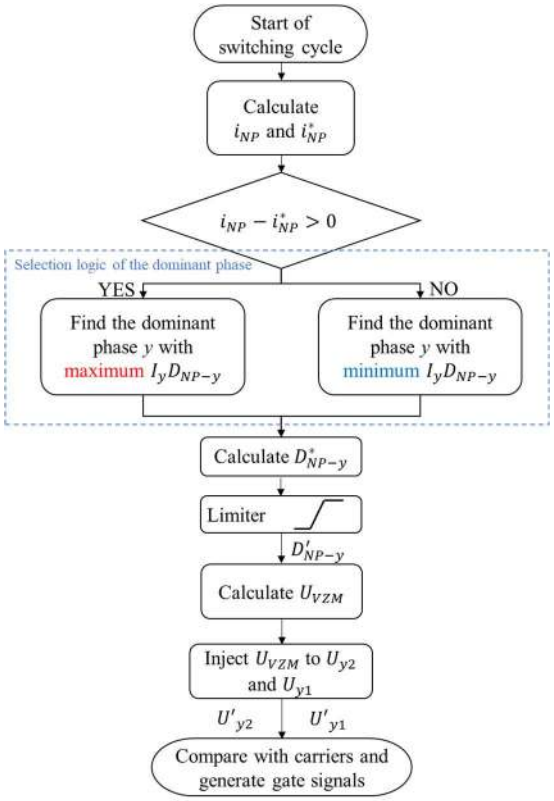


Fig. 6. Illustration of VZM based voltage balancing algorithm

Note when D'_{NP} is reduced to zero, the output voltage skips the middle level and jumps straight between +DC and −DC, which is equivalent to a two-level converter. Therefore, if the converter is preferred to operate as a multilevel converter with reduced dV/dt, a nonzero minimum boundary of D'_{NP} can be set as a "dwell time" [20] to keep the existence of the middle level. In the implementation of this work, the dwell time is set as the power device deadtime.

To summarize, the VZM approach utilizes the redundant voltage level to alter the duty ratios and gain the controllability of the NP current. Following the demanded NP current, the VZM requires the dominant phase selection logic and the implementation in the modulation. This whole process achieves the closed-loop voltage balancing on switching window basis.

E. Hybrid Voltage Balancing Scheme

As analyzed in [15], VZM increases the switching loss significantly due to the extra switching transitions. In the case of high-switching-frequency power electronics systems, the switching loss is the main contributor of converter power loss, where the drawback of VZM becomes significant. Additionally, VZM also increases the high-frequency harmonics [12]. Therefore, it is undesirable to activate VZM constantly, especially when ZSI is capable already to suppress the NP voltage oscillation. This concept leads to the following hybrid modulation scheme with a strategy deciding how/when to utilize the two degrees of freedom, ZSI and VZM. The main idea of this hybrid approach is to moderate the negative side effects of VZM while still eliminating the low-frequency NP oscillation over full range of converter operating point. A top-level flow of the proposed control scheme is shown in Fig. 7.

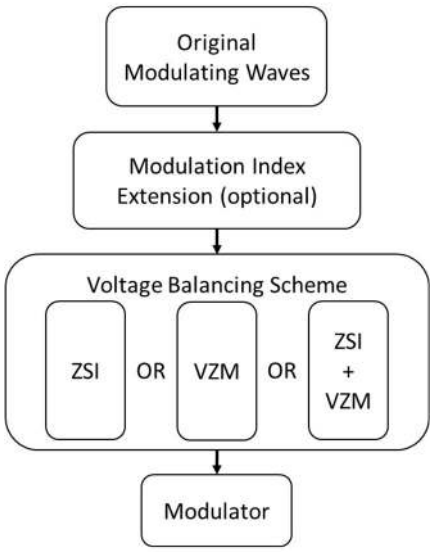


Fig. 7. Top-level flow of the modulating waves

The original sinusoidal modulating waves firstly go through an optional step for Modulation Index Extension (MIE) by injecting a third-order harmonic, which expands the maximum modulation index M from 1 to 1.15. An option of this third-order zero-sequence signal is (17) as used in [12]. Note the voltage balancing strategy presented in [12] should be considered as "MIE + VZM" when M $\leqslant$ 1, where the MIE step is optional.

$$U_{off} = -[\max(U_a, U_b, U_c) + \min(U_a, U_b, U_c)]/2 \quad (17)$$

Next, the modulating waves flow through the voltage balancing block. The detailed process of the voltage balancing block is presented in Fig. 8. In this scheme, the ZSI block and the VZM block is placed in series. ZSI acts as the first-stage compensation and yields altered reference voltages $U_{\text{abc-ZSI}}$ and compensated $i_{\text{NP-ZSI}}$ by calculation. Then these variables are fed into VZM block for a second-stage compensation and yields the final altered reference voltages for the generation of gate signal. In the second-stage VZM block, the duty ratios are still calculated through (3)-(5) with U_x replaced with $U_{\text{abc-ZSI}}$, and the i_{NP} in (15) is replaced by $i'_{\text{NP-ZSI}}$.

Between the first stage and second stage, a judgement step is placed comparing the ZSI compensated $i_{\text{NP-ZSI}}$ and desired i^*_{NP}. If $i_{\text{NP-ZSI}}$ equals to i^*_{NP}, it means the control objective is already satisfied by ZSI, and VZM at the second stage will be bypassed. This step ensures that the activation of VZM is only activated when necessary. In practice, due to limited decimal precision and achievable number of iterations, it is more feasible to set a threshold value (e.g. $|i_{\text{NP1}} - i^*_{\text{NP}}| < 0.01$ p.u.) as the criteria, rather than strictly requiring $i_{\text{NP1}} - i^*_{\text{NP}} = 0$. From another perspective, this threshold value can be treated as sacrificing the controllability in exchange for less power loss. The larger the threshold value is, the less VZM will be used, resulting in less power loss and potentially higher NP voltage ripple amplitude.

If the judgement step rules that the ZSI cannot satisfy the control objective, there are two options for the following action: Option 1: Keep the alterations made by ZSI stage and activate VZM on top of modified modulating waves $U_{\text{abc-ZSI}}$, which is referred as "ZSI + VZM"; Option 2: Discard the calculated U_{ZSI} and activate VZM based on the original U_{abc}, for which the balancing scheme is referred as "ZSI or VZM". "ZSI + VZM" is preferred in this work because it can achieve the optimal balancing controllability. The analysis of these two options regarding the dynamic balancing performance is presented in the next section.

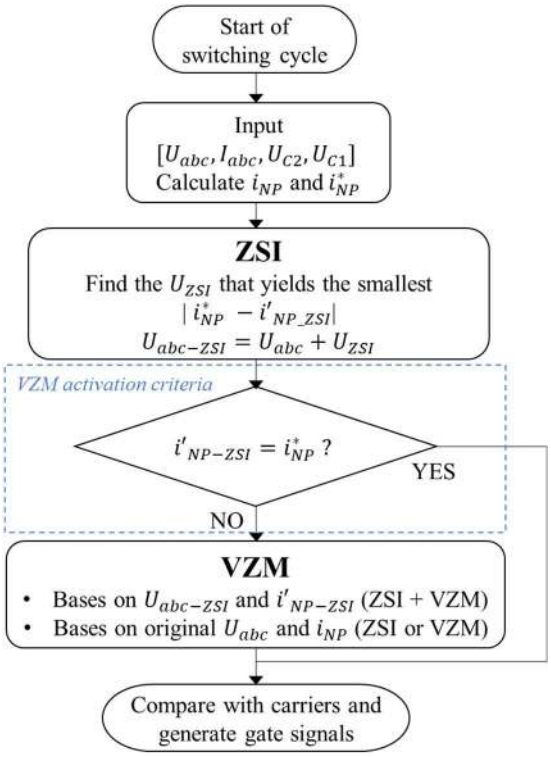


Fig. 8. Proposed hybrid voltage balancing algorithm

III. Comparison with Existing Approaches

This section compares the proposed scheme and the existing approaches reported in literatures. To show a straightforward comparison, the following parameters are defined to describe the utilization of VZM across various approaches.

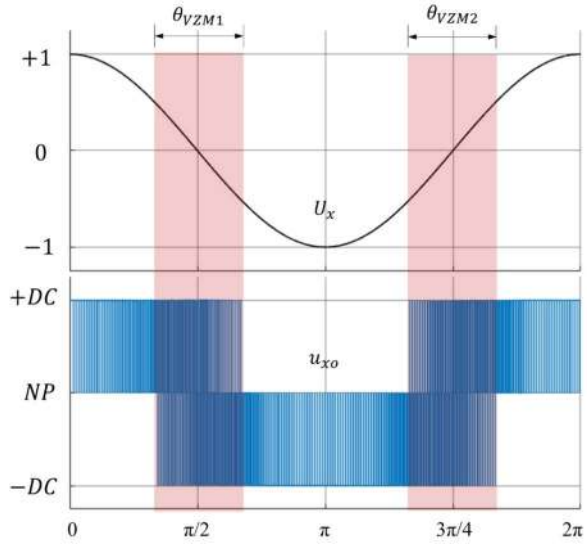


Fig. 9. VZM activated intervals for one phase leg (non-optimized), $\theta_{\text{VZM1}} = \theta_{\text{VZM2}} = 60°$ ($M = 1$, $\varphi = 90°$)

Firstly, in the scope of a fundamental cycle, parameter α is defined as the proportion of the VZM activated intervals. Fig. 9 shows the VZM activated intervals θ_{VZM} with the non-optimized VZM, e.g. the DSPWM presented in [17]. In Fig. 9, VZM is activated in the intervals θ_{VZM1} and θ_{VZM2}, which adds up to α = 33%. In this case, in one third of the time, this phase output voltage jumps between three voltage levels and the total switching events in the converter increases for 33%.

In the proposed approach, the VZM intervals are dynamically determined in a close loop by the *VZM activation criteria* in Fig. 8, which considers the unbalance of the capacitor voltages ΔU_{NP} (see equation(9)) and the ZSI compensated NP current $i'_{NP\text{-}ZSI}$. α can be minimized in the proposed hybrid approach to reduce the additional switching events. The quantified evaluation of α will be presented in Section IV.D.

Secondly, in the scope of a carrier cycle, parameter β is defined as the compensation strength of VZM, which is determined by

$$\beta = (D_{NP} - D'_{NP})/D_{NP} \quad (18)$$

β ranges between 0 and 1, which corresponds to the achievable range of modified NP duty ratio D'_{NP} defined in (16). Fig. 10 shows the effect of β on the phase output voltage in a carrier cycle. The larger β is, the more zero-level is replaced by +1/−1 levels, which leads to a less duration of clamping to the neutral point. Note the volt-time products are equal in all three cases in Fig. 10. As the extreme case, in Fig. 10(c), β equals to 1 and the NP duration is reduced to zero, which leads to the output voltage skipping the middle zero level. As introduced, a "dwell time" can be programmed to avoid $\beta = 1$.

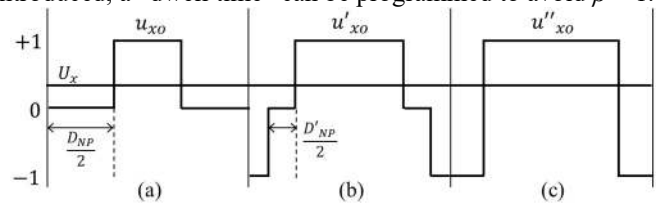


Fig. 10. Effect of the VZM compensation strength (a) $\beta = 0$ (regular PWM) (b) $\beta = 0.6$ (c) $\beta = 1$

In the proposed approach, the compensation strength β is precisely determined by the unbalance of the capacitor voltages, reference voltages and load currents in every carrier cycle (see (9) and (15)). β is implemented as U_{VZM} as shown in Fig. 4.

In short, both α (θ_{VZM}) and β are determined in a dynamic close loop in the proposed approach. As a comparison, in [21], the compensation strength β is determined by forcing the NP current to zero without considering the measured unbalance of the NP voltage. In [17], the VZM activated intervals are determined by the reference voltage and α is fixed at 33% regardless of the operating point. In [9], [21], the VZM activated intervals are determined by a predefined parameter.

Regarding ZSI, in the proposed ZSI + VZM approach, the optimal ZSI is constantly applied regardless of whether the VZM is turned on, in order to gain the maximum controllability on the NP voltage. In [21], equivalently, the ZSI intervals and VZM intervals are separated without any overlap. In [12], the injected zero-sequence voltage is the MIE (17), which is generated open-loop and is not intended as the optimal selection towards NP balancing.

Regarding the voltage balancing performance, the proposed approach can effectively eliminate the low-frequency NP oscillation over the full range of modulation index and power factor ($cos\ \varphi$ = 0 ~ 1; M = 0 ~ 1.15). This versatility is not verified or achieved in several existing approaches, such as [9], [21].

Based on the above key concepts, a comparison with several representative approaches reported in literatures is presented in TABLE I.

TABLE I. COMPARISON OF KEY CONCEPTS OF VZM BASED VOLTAGE BALANCING SCHEMES

	VZM intervals θ_{VZM} and α	VZM compensation strength	Dynamic hybrid of ZSI and VZM	Verified effective in full range of M and φ
[9]	Open-loop, predefined	Open-loop, predefined	No	No
[21]	Open-loop, predefined	Open-loop, predefined	No	No
[22]	Open-loop, predefined	Closed-loop, dynamic	No	No
[23]	Open-loop, predefined	Closed-loop, dynamic	No	No
[12]	Closed-loop, dynamic	Closed-loop, dynamic	No	Yes
This paper	**Closed-loop, dynamic**	**Closed-loop, dynamic**	**Yes**	**Yes**

IV. PERFORMANCE EVALUATION BY SIMULATION

A. Voltage balancing performance

The above introduced scheme is implemented in Matlab/Simulink on a three-phase inverter system with the specifications listed in TABLE II.

TABLE II SPECIFICATIONS OF THE SIMULATED SYSTEM

Power Rating	54 kVA	Current	150 Arms
DC-link Voltage	350 V	DC-link Capacitance	$C_1 = C_2 =$ 2 mF
Switching frequency	50 kHz	Fundamental frequency	50 Hz
Modulation Index	0 ~ 1.15	Power Factor φ	**[-90°, +90°]**

Firstly, Fig. 11 shows the converter performance when a step change in modulation index and power factor is assumed. It can be seen that the proposed algorithm offers a seamless transition when the operating point changes, with the low-frequency NP oscillation completely attenuated.

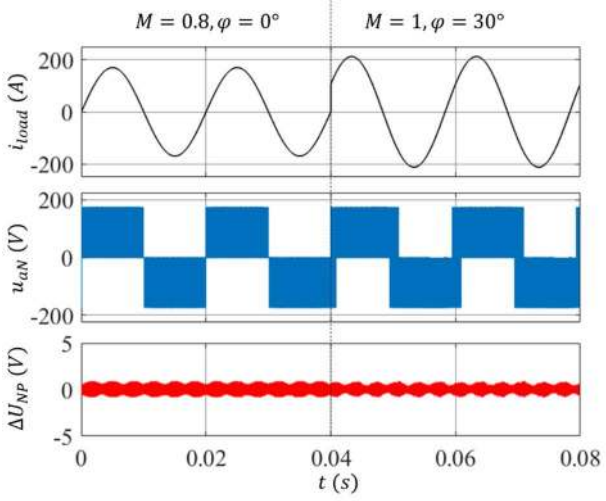


Fig. 11. Performance with step change of modulation index and power factor

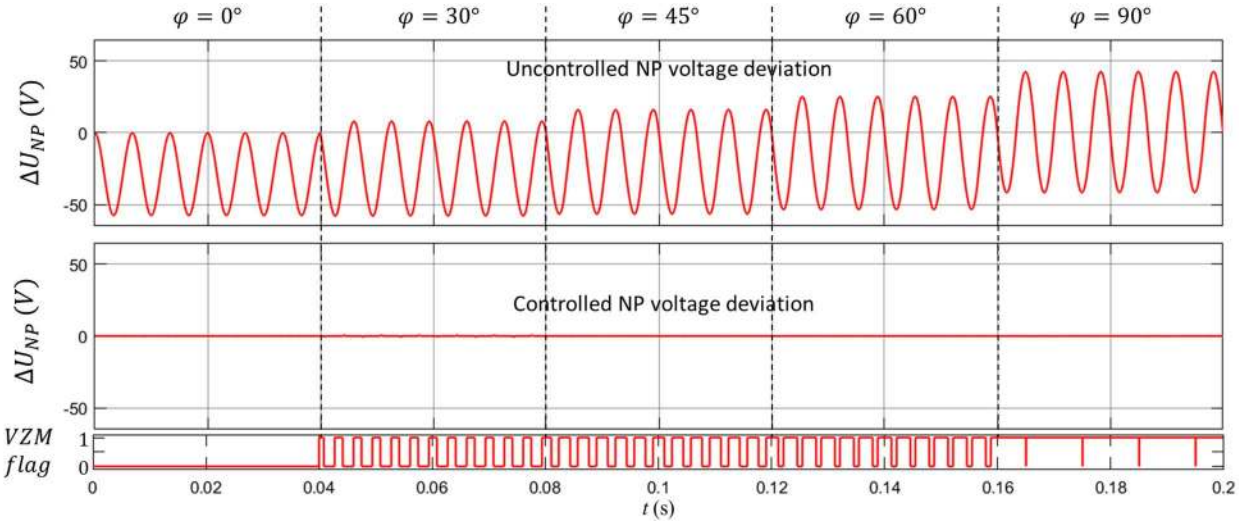


Fig. 12. Uncontrolled NP voltage deviation; controlled NP voltage deviation with ZSI + VZM; VZM activation flag. M = 1 with sinusoidal modulating waves

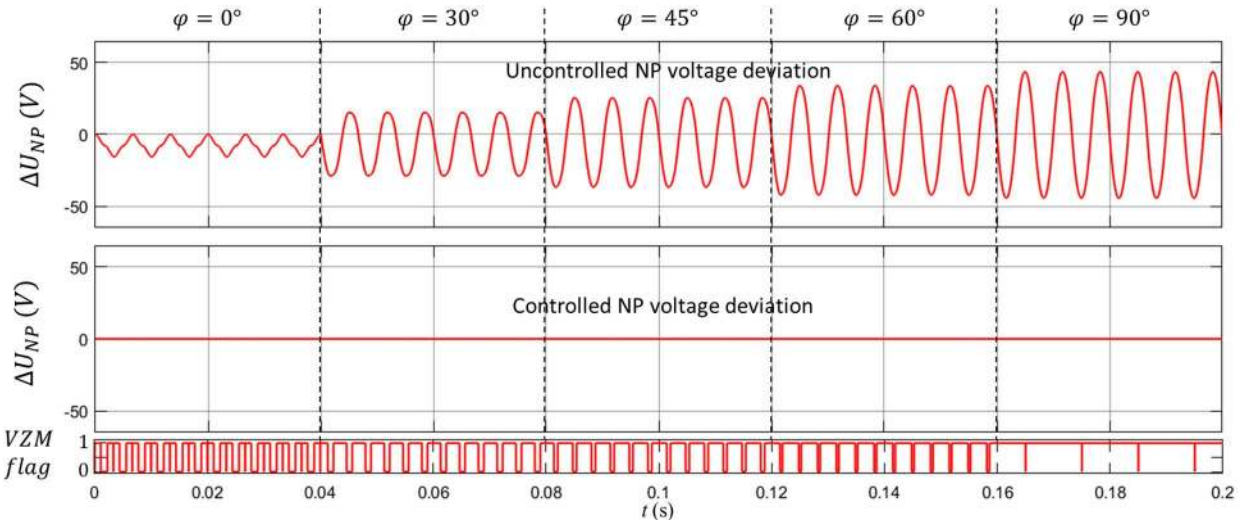


Fig. 13. Uncontrolled NP voltage deviation; controlled NP voltage deviation with ZSI + VZM; VZM activation flag. M = 1.15 with modulation index extension (17)

Secondly, the steady-state voltage balancing performance of the proposed scheme is evaluated over various power factor and modulation index. The results are shown in Fig. 12 and Fig. 13. The "VZM flag" indicates if the VZM operation is turned on: when the flag is 0, VZM is turned off, where ZSI is sufficient in achieving voltage balancing; when the flag is 1, VZM is turn on for extended balancing capability, where the switching events will be doubled.

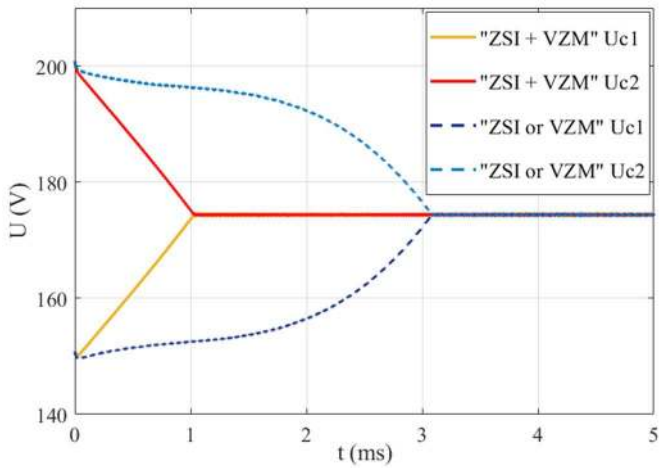


Fig. 14. Dynamic balancing performace, "ZSI + VZM" vs. "ZSI or VZM" M = 0.9, φ = 30°, with modulation index extension (17)

As can be seen in Fig. 12 and Fig. 13, the proposed ZSI+VZM algorithm is effective in eliminating the low-frequency NP oscillation over full power factor range in the cases of $M = 1$ and $M = 1.15$. Note when the power factor equals to 90°, the ZSI + VZM mode will be constantly activated as shown in Fig. 12 and Fig. 13. This is because the ZSI loses the NP controllability at low power factor.

The performances of "ZSI or VZM" or "ZSI + VZM" are also compared in simulation. Given an initial unbalance of voltages, the balancing performance of the two options are presented in Fig. 14. As shown in the figure, the unbalance of capacitor voltages can be successfully compensated by both options. It is visible that "ZSI + VZM" offers quicker dynamic performance compared to "ZSI or VZM". This is because "ZSI or VZM" does not improve the controllability compared to individual ZSI or VZM, while "ZSI + VZM" combines the merits of both.

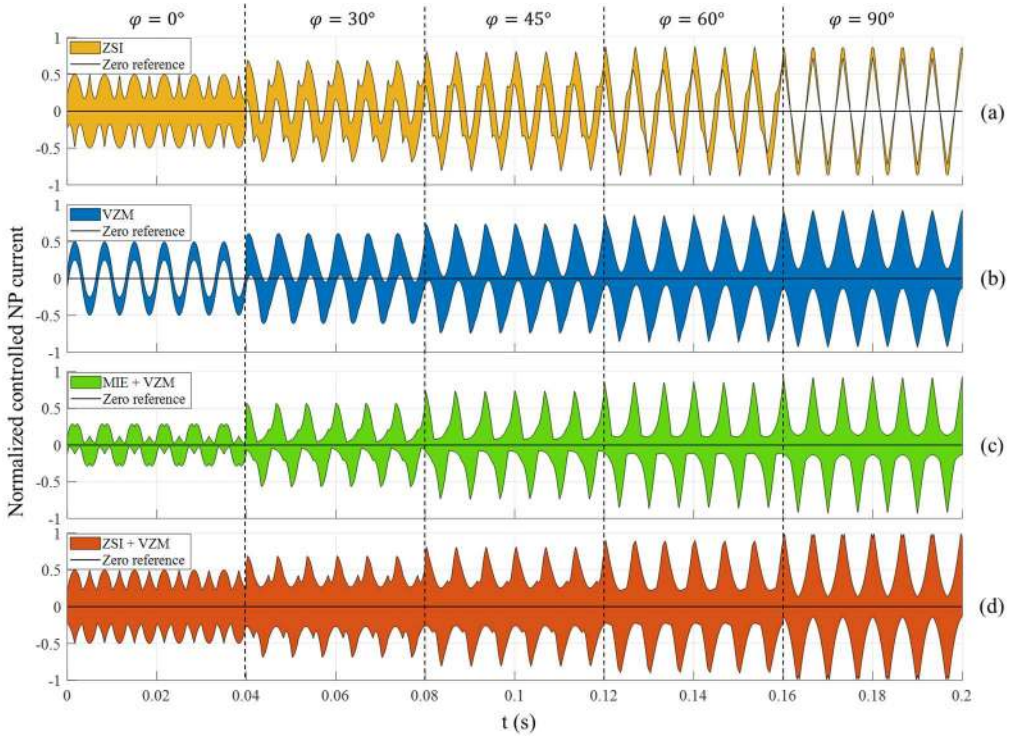


Fig. 15. Achievable NP current range under various control schemes, M = 1

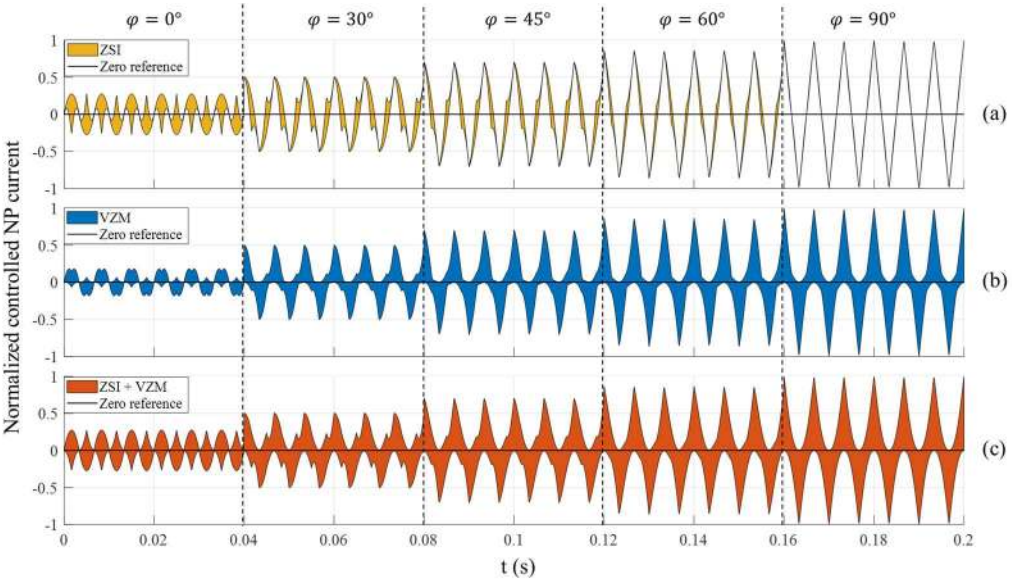


Fig. 16. Achievable NP current range under various control schemes with MIE (17) injected, M = 1.15

B. Controllability analysis

This section compares the controllability of the introduced balancing methods: (1) ZSI (2) VZM (3) MIE + VZM when M $\leqslant$ 1 (4) proposed ZSI + VZM. The achievable NP current is proposed as an indicator of the controllability and is investigated through simulation. In each switching window, the simulation is programmed to record the range of achievable NP current of each control scheme through numerical calculation.

As introduced, the ZSI method is based on optimal searching iterations, in which a pool of achievable NP current can be easily recorded in each switching cycle. For VZM, the achievable NP current range can be found through the following simplified method. As elaborated in section II.C, the VZM can only reduce the NP duty ratio of one phase ($D_{\text{NP-x}}$). Therefore, assuming the minimum $D'_{\text{NP-x}}$ to be zero, the maximum achievable NP current can be found by removing the minimum negative phase term ($D_{\text{NP-x}}I_{\text{x}}$) in (6), and vice versa.

The achievable NP current for the evaluated modulation schemes is plotted in Fig. 15 and Fig. 16, which should be interpreted as:

- If the shaded area does not cover zero, it indicates that the NP potential will suffer a low-frequency oscillation. If the shaded area covers zero, it indicates that the NP deviation can be maintained at zero from the low-frequency point of view.
- If the shaded area is unidirectional, it indicates that the

balancing scheme loses the ability to pull back the NP potential when the imbalance demands an opposite i^*_{NP}.

- The larger vertical amplitude at any moment (larger shaded area over time) indicates faster dynamic balancing performance. For example, when $U_{C2} < U_{C1}$, a positive NP current is desirable to pull down the NP voltage. In this case, a larger NP current will be able to achieve the control objective in a shorter period.

With the converter operating at full modulation index $M = 1$, the following conclusions can be drawn from Fig. 15

- As Fig. 15(a) shows, ZSI works well under unity power factor. But, ZSI loses its effectiveness once there are reactive loads introduced, and it reaches its worst case at zero power factor. This limitation of ZSI is in line with the previous research [6], [10].
- As Fig. 15(b) shows, VZM works the best at zero power factor. However, VZM loses the full bidirectional controllability at unity power factor.
- As Fig. 15(c) shows, if the MIE (17) is injected when $M \leqslant 1$, the VZM is then able to achieve the balancing throughout the whole modulation index/power factor range. This is equivalent to the approach reported in [12], [17]. It indicates that the optional third-order harmonic moderates the NP oscillation when $M \leqslant 1$. However, (17) is not the optimal zero-sequence voltage towards the voltage balancing because it is intended for extending the modulation index.
- As Fig. 15(d) shows, ZSI + VZM combines the achievable range of both approaches and offers the widest controllable range among all approaches, which is considered as the optimal.

With the converter operating at extended modulation index $M = 1.15$, Fig. 16 shows that the ZSI+VZM still offers the widest shaded area compared to either ZSI or VZM alone. It is also visible that the controllable range of ZSI+VZM well covers zero reference across all power factors.

Note that the proposed ZSI + VZM approach is implemented in two separate stages in series, where the VZM in the second stage does not undermine the efforts made by ZSI. By design, VZM only closes the gap between the ZSI compensated NP current $i'_{NP\text{-}ZSI}$ and the reference NP current i^*_{NP}. As shown in Fig. 8, the VZM block is applied on top of $i'_{NP\text{-}ZSI}$ and $U_{abc\text{-}ZSI}$.

It is possible to combine the two approaches in a single stage and search for the optimal combination of U_{ZSI} and U_{VZM} for maximum voltage balancing controllability. However, because the ZSI is based on iterations, the combined stage will require significant computation resource. Additionally, if the ZSI does not make the efforts as much as possible in the proposed first stage, there might be the need to use VZM more, which is against the intention of reducing the usage of VZM.

Therefore, this paper considers the proposed two-stage hybrid of ZSI+VZM as the optimal hybrid implementation.

C. Evaluations on NP voltage ripple amplitude and output voltage harmonics

This section evaluates the amplitude of the NP voltage ripples/oscillations and the output voltage harmonics across the modulation schemes. Following [6], [9], [10], a normalized amplitude of the low-frequency NP voltage oscillation is defined as (19) to quantify the issue across various systems against a base value ΔU_{Nf0} that is associated with the fundamental-frequency f_0, the load current I_{rms} and the capacitance C.

$$\Delta U_{NPn-f0} = \frac{\Delta U_{NP}}{\Delta U_{Nf0}} = \Delta U_{NP} \div \frac{I_{rms}}{f_0 \cdot C} \tag{19}$$

Where ΔU_{NP} is the peak-to-peak value of NP voltage deviation. When the low-frequency NP voltage ripple is successfully eliminated, the remaining high-frequency ripple is proposed to be normalized through (20), which is defined similarly to [24].

$$\Delta U_{NPn-fsw} = \frac{\Delta U_{NP}}{\Delta U_{Nfsw}} = \Delta U_{NP} \div \frac{I_{rms}}{f_{sw} \cdot C} \tag{20}$$

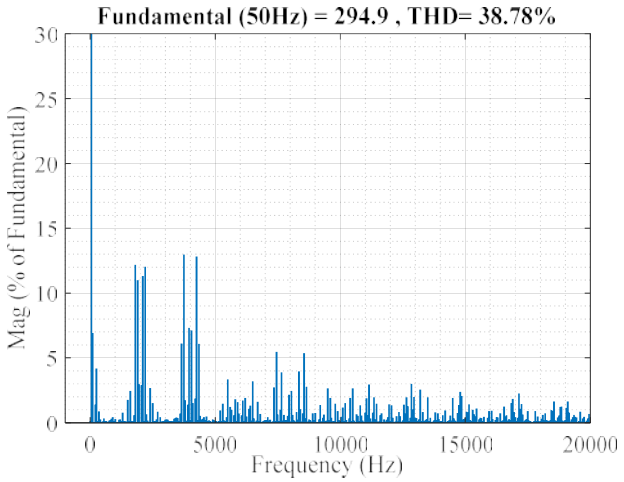
The worst-case normalized voltage ripple amplitude is useful for the determination of the required capacitances in the virtual prototyping/optimization of a power converter [25]. The evaluated voltage ripple is presented in TABLE III, where the red cases suffers the low-frequency oscillation and the green cases only contains high-frequency ripples.

TABLE III. NP VOLTAGE RIPPLE/OSCILLATION AMPLITUDE ($M = 1$, $f_{sw} = 50$ kHz)

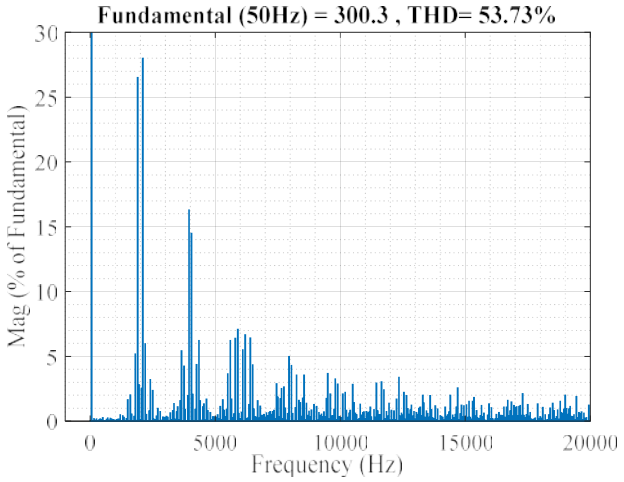
	$\varphi = 0°$	$\varphi = 30°$	$\varphi = 90°$
No balancing	58 V (0.0387 $\Delta U_{NPn\text{-}f0}$)	66 V (0.0440 $\Delta U_{NPn\text{-}f0}$)	84 V (0.0563 $\Delta U_{NPn\text{-}f0}$)
ZSI	0.26V (0.1733 $\Delta U_{NPn\text{-}fsw}$)	12 V (0.0080 $\Delta U_{NPn\text{-}f0}$)	64 V (0.0427 $\Delta U_{NPn\text{-}f0}$)
VZM	38 V (0.0253 $\Delta U_{NPn\text{-}f0}$)	4 V (0.0027 $\Delta U_{NPn\text{-}f0}$)	0.16 V (0.1067 $\Delta U_{NPn\text{-}fsw}$)
HYB	0.26 V (0.1733 $\Delta U_{NPn\text{-}fsw}$)	0.34 V (0.2267 $\Delta U_{NPn\text{-}fsw}$)	0.16 V (0.1067 $\Delta U_{NPn\text{-}fsw}$)

In terms of the harmonics, a case study is conducted with the converter operating at $M = 1$ and $\varphi = 30°$. As analyzed, the ZSI cannot eliminate the low-frequency NP oscillation in this operating point. Therefore, only the VZM and the proposed hybrid schemes are compared. For better illustration, the switching frequency is lowered to 2 kHz. The spectrum results are shown in Fig. 17, with the THD calculated up to 20 kHz.

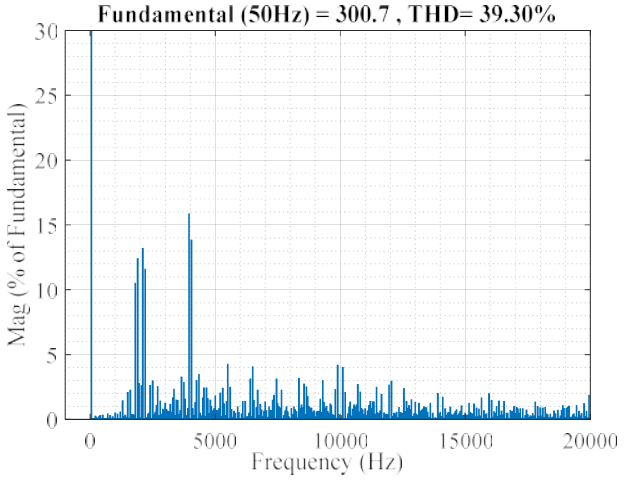
As can be seen from Fig. 17 (a), without any voltage balancing scheme applied, the output line-to-line voltage suffers low-frequency harmonics as a result of the oscillating DC-link neutral point, with harmonic contents of 6.93% at 100 Hz (2nd), 1.39% at 200 Hz (4th) and 4.19% at 250 Hz (5th). In Fig. 17 (b), the VZM completely eliminates the low-frequency harmonics. But, as the negative side effect, significantly increased high-frequency harmonics are observed as a result of increased switching transitions. The THD with the VZM increases to 53.73% because of the high-frequency harmonics. In Fig. 17 (c), the proposed hybrid scheme also eliminates the low-frequency harmonics, while the high-frequency harmonics are moderated compared to VZM. The THD with the hybrid scheme is improved to 39.30% compared to VZM. It can be concluded that the proposed hybrid scheme can effectively improve the high-frequency harmonic contents while eliminating the low-frequency harmonics.



(a) No balancing



(b) VZM



(c) Proposed hybrid scheme (ZSI+VZM)

Fig. 17. FFT of converter output line-to-line voltage (M =1 and φ = 30°)

As the special case, the THD analysis is conducted in the extended modulation index range of M = 1 ~ 1.15. The results plotted in Fig. 18 shows that the proposed ZSI + VZM still offers improved harmonics compared to VZM. At M = 1.15, the gap between the THD of VZM and the hybrid is closing, because VZM is nearly turned on constantly in ZSI+VZM as presented in Fig. 13. The THD in the "no balancing" case is less due to the absence of VZM, while it contains large low-order harmonics that is similar to Fig. 17 (a).

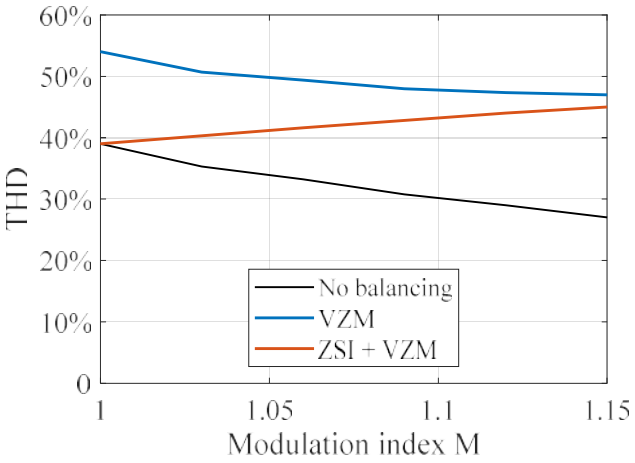


Fig. 18. THD of output line-to-line voltage (M = 1 ~ 1.15, φ = 30°)

D. Evaluations on device power losses

As introduced, there is always one phase with the VZM activated for voltage balancing purpose. Whenever VZM is activated, it leads to doubled switching transitions and hence significantly increased switching loss. In a three-phase converter, there are 33% more switching events with VZM constantly activated in the dominant phase y. To demonstrate the benefit of the proposed hybrid scheme, the proportion of VZM activated intervals α is plotted against the load power factor in Fig. 19. As introduced in Section III, parameter α also indicates the increase of switching events.

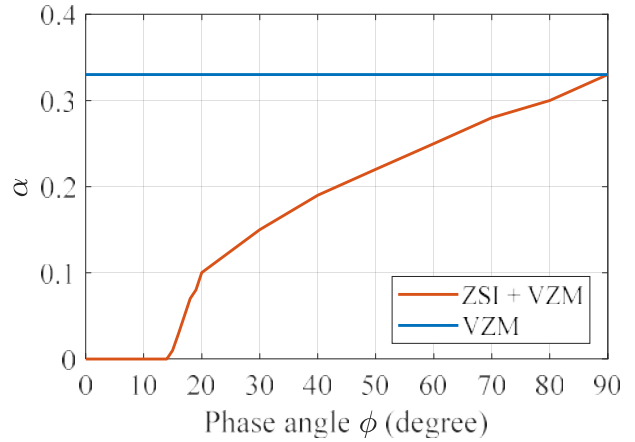


Fig. 19. Comparison of proportion of the VZM activated intervals α (M = 1)

Fig. 19 shows that the parameter α keeps constant at 33% with un-optimized VZM, while it shows a significant reduction in high power factor cases with the proposed hybrid scheme. For example, the additional switching events is lowered from 33% to 15% at φ = 30° by applying the hybrid scheme over the regular VZM. Fig. 20 shows the phase output voltage in this case, where clearly VZM activated intervals shrink in the case of ZSI + VZM. In Fig. 19, it is also visible that VZM is not activated at all if the phase angle is below approximately 14°, because ZSI is already fully sufficient in this case.

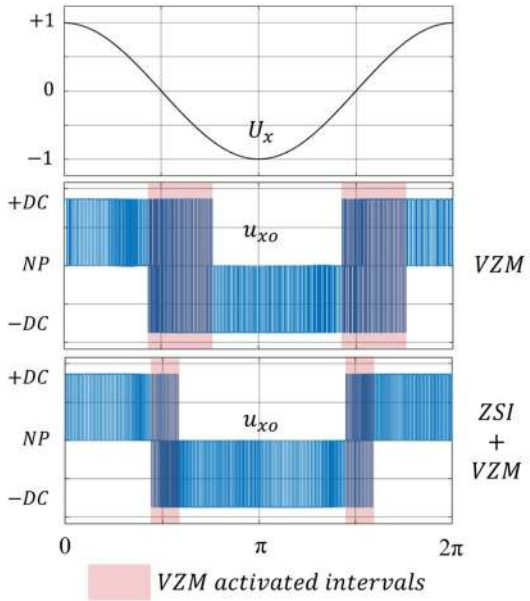


Fig. 20. Phase output voltage ($\varphi = 30°$, $M = 1$)

This comparison demonstrates that the hybrid scheme reduces the increase of switching events due to VZM, especially at higher power factor. It should be highlighted that this benefit is achieved without sacrificing the voltage balancing capability. The low-frequency oscillation is still completely attenuated as shown in Fig. 12.

Apart from the activated intervals, the VZM associated increase of switching loss also depends on the load current level where VZM is activated. An analytical analysis of the power losses of un-optimized VZM is conducted in [15], which shows the increase of the converter switching loss can reach 41% in the case where the power factor is zero.

In the proposed hybrid algorithm, the VZM is activated only when it is necessary. Hence, the additional switching loss associated with VZM can be moderated. Due to the nonlinearity of the hybrid scheme, the power loss evaluation is conducted in experiments that will be presented in the next section.

V. Experimental Verification

To verify and evaluate the proposed control scheme, a downscaled test rig is built with the components listed in Table IV. The control scheme is programmed in a Digital Signal Processor (DSP), TMS320F28335. A picture of the test rig is shown in Fig. 21.

TABLE IV. Components in the Downscaled Test Rig

DC-link voltage supply	Elektro-Automatik TS 8000 T	***Power Analyzer***	Norma 4000
Power device	SKiM301TMLI12E4B from Semikron	***Load inductance***	6.23 mH per phase
DC-link Capacitance	$C_1 = C_2 = 220$ µF	***Load resistance***	2.2 Ω per phase

Firstly, the voltage balancing performances of the control schemes are assessed. As shown in Fig. 22, without the voltage balancing control, the NP voltage oscillation reaches ± 20 V with a frequency of $3 \cdot f_0$, and the output current is clearly distorted. Because the ZSI is not effective at this operating point of the test rig ($\cos \varphi = 0.747$, $M = 1.15$), only the VZM and the proposed hybrid scheme (HYB) are compared. In Fig. 23 and Fig. 24, it is clear that both VZM and proposed hybrid scheme can successfully suppress the low-frequency NP voltage oscillation. The NP oscillation is suppressed to switching-frequency ripples with an amplitude of less than ± 1V.

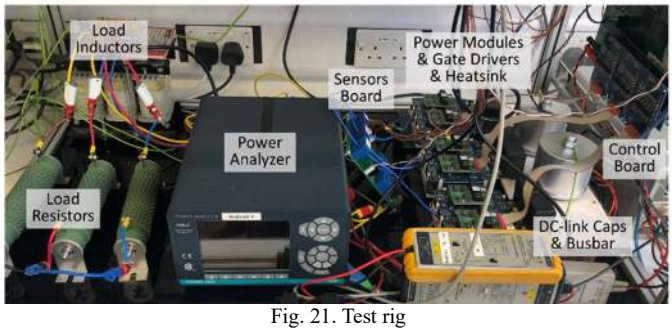


Fig. 21. Test rig

In Fig. 23, it is visible that the output phase voltage jumps between three voltage levels in the boxed part, which is a result of the activation of VZM. In Fig. 24, part of the output voltage

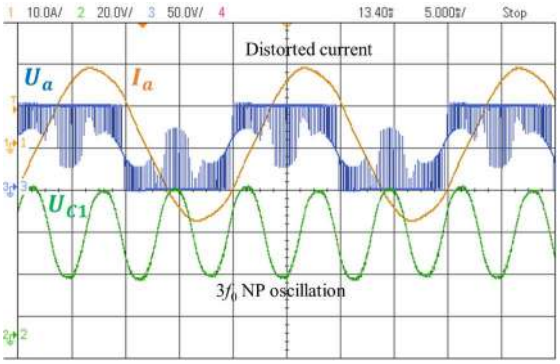


Fig. 22. Experimental waveforms with SPWM
(U_{DC} = 100V, M = 1.15, f_0 = 50 Hz, R = 2.2 Ω, L = 6.32 mH per phase)

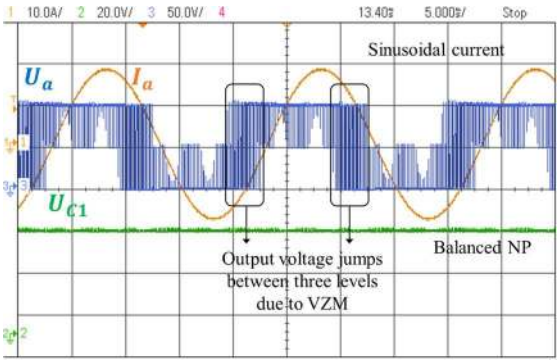


Fig. 23. Experimental waveforms with VZM
(U_{DC} = 100V, M = 1.15, f_0 = 50 Hz, R = 2.2 Ω, L = 6.32 mH per phase)

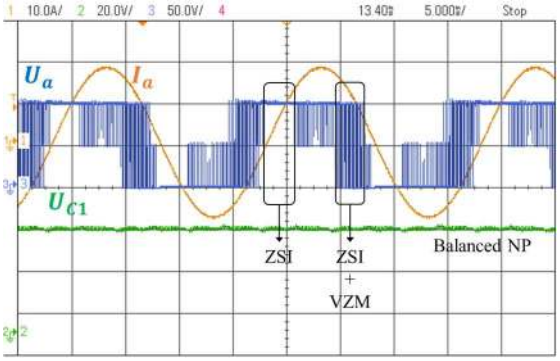


Fig. 24. Experimental waveforms with proposed ZSI + VZM
(U_{DC} = 100 V, M = 1.15, f_0 = 50 Hz, R = 2.2 Ω, L = 6.32 mH per phase)

shows the sign of ZSI, and part of it shows the sign of VZM, which shows a hybrid operation with two approaches.

The operating point shown in the figures is at full modulation index (M = 1.15), which shows that the balancing scheme does not undermine the output capacity of the power converter. Note in practice, the delays in the close-loop NP control, e.g. sampling delays, can result in nonideal suppression of NP oscillation. In the presented test rig, the delays are minimized by (a) adjust the filter parameters in the sampling loop for less delays (b) optimizing the algorithm to ensure the computation time of the whole scheme shorter than one switching period.

The power loss of power conversion stage is measured as (21) by instruments listed in TABLE IV with the converter operating at various switching frequencies.

$$P_{loss} = P_{DC} - P_{AC} \tag{21}$$

The results and fitted curves are plotted in Fig. 25. It is visible that the proposed hybrid NP balancing scheme (red) has reduced switching loss compared to VZM (blue), as the gradient of its power loss curve is smaller. This merit of the proposed hybrid balancing scheme is expected because it reduces the usage of VZM.

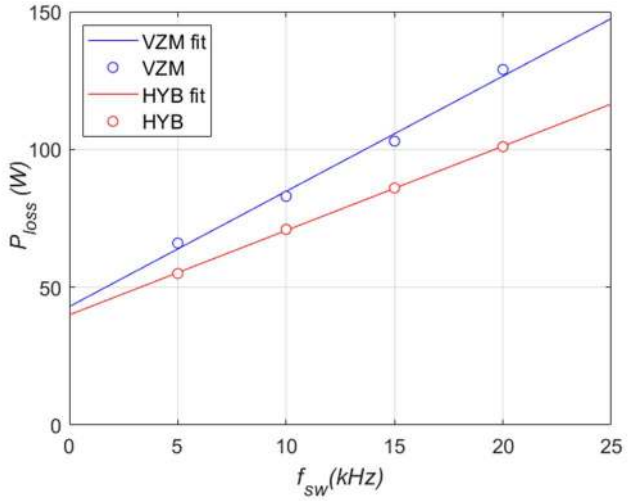


Fig. 25. Comparison of power loss measured experimentally
(U_{DC} = 100V, M = 1.15, f_0 = 50 Hz, R = 2.2 Ω, L = 6.32 mH per phase)

VI. CONCLUSION

This paper proposes a hybrid voltage balancing algorithm for three-phase, three-level converters. The proposed algorithm utilizes and coordinates the two available voltage balancing methods in modulation, ZSI and VZM. It is proven that the proposed algorithm can effectively eliminate the low-frequency neutral point voltage oscillation over the full power factor/modulation range. Additionally, the closed-loop voltage balancing is conducted on switching cycle basis and does not undermine the converter output capacity.

Evaluations are conducted regarding the controllability, voltage ripple amplitude and harmonic content to compare the various modulation schemes. The "VZM + ZSI" hybrid combines the merits of both the ZSI and VZM, which offers the optimal performance as demonstrated. The side effects of VZM, the increased switching loss and high-frequency output harmonics, are moderated in the hybrid scheme, because the VZM is programmed to activate only when necessary.

The proposed voltage balancing algorithm is fully based on numerical and logical operations and level-shifted carriers, which is easy to implement in modern digital controllers. The concept of combining the two degrees of freedom can be applied to other multilevel topologies for voltage balancing.

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REFERENCES

[1] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Transactions on Industry Applications*, vol. 1A-17, no. 5, pp. 518–523, 1981.

[2] M. Schweizer and J. W. Kolar, "Design and implementation of a highly efficient three-level T-type converter for low-voltage applications," *IEEE Transactions on Power Electronics*, vol. 28, no. 2, pp. 899–907, 2013.

[3] S. Ogasawara and H. Akagi, "Analysis of variation of neutral point potential in neutral-point-clamped voltage source PWM inverters," *Proc. IEEE Industry Applications Conf.*, pp. 965–970, 1993.

[4] S. Busquets-Monge, J. Bordonau, D. Boroyevich, and S. Somavilla, "The nearest three virtual space vector PWM—a modulation for the comprehensive neutral-point balancing in the three-level NPC inverter," *IEEE Power Electronics Letters*, vol. 2, no. 1, pp. 11–15, 2004.

[5] I. Lopez *et al.*, "Generalized PWM-based method for multiphase neutral-point-clamped converters with capacitor voltage balance capability," *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4878–4890, 2017.

[6] J. Pou, R. Pindado, D. Boroyevich, and P. Rodríguez, "Evaluation of the low-frequency neutral-point voltage oscillations in the three-level inverter," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 6, pp. 1582–1588, 2005.

[7] N. Celanovic and D. Borojevic, "A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters," *IEEE Transactions on Power Electronics*, vol. 15, no. 2, pp. 242–249, 2000.

[8] S. Busquets Monge, S. Somavilla, J. Bordonau, and D. Boroyevich, "Capacitor voltage balance for the neutral-point-clamped converter using the virtual space vector concept with optimized spectral performance," *IEEE Transactions on Power Electronics*, vol. 22, no. 4, pp. 1128–1135, 2007.

[9] J. Zaragoza, J. Pou, S. Ceballos, E. Robles, P. Ibáñez, and J. L. Villate, "A comprehensive study of a hybrid modulation technique for the neutral-point-clamped converter," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 2, pp. 294–304, 2009.

[10] C. Wang and Y. Li, "Analysis and calculation of zero-sequence voltage considering neutral-point potential balancing in three-level NPC converters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2262–2271, 2010.

[11] J. Chivite-Zabalza, P. Izurza-Moreno, D. Madariaga, G. Calvo, and M. A. Rodríguez, "Voltage balancing control in 3-level neutral-point clamped inverters using triangular carrier PWM modulation for FACTS applications," *IEEE Transactions on Power Electronics*, vol. 28, no. 10, pp. 4473–4484, 2013.

[12] I. Lopez, S. Ceballos, and J. Pou, "Modulation strategy for multiphase neutral-point-clamped converters," *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 928–941, 2016.

[13] C. Wang, X. Si, and H. Xin, "Control of neutral-point voltage in three-phase four-wire three-level NPC inverter based on the disassembly of zero level," in *Proc. IEEE Energy Conversion Congress and Exposition*, 2016.

[14] X. Yuan, J. Yon, and P. Mellor, "Common-mode voltage reduction in three-level neutral-point-clamped converters with neutral point voltage balance," in *Proc. IEEE International Symposium on Industrial Electronics Conf.*, 2013.

[15] J. Wang *et al.*, "Analytical averaged loss model of three-phase T-type STATCOM with virtual zero level modulation," in *Proc. IEEE Energy Conversion Congress and Exposition*, 2017.

[16] R. M. Tallam, R. Naik, and T. A. Nondahl, "A carrier-based PWM scheme for neutral-point voltage balancing in three-level inverters," *IEEE Transactions on Industry Applications*, vol. 41, no. 6, pp. 1734–1743, 2005.
[17] J. Pou *et al.*, "Fast-processing modulation strategy for the neutral-point-clamped converter with total elimination of low-frequency voltage oscillations in the neutral point," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 4, pp. 2288–2294, 2007.
[18] J. Wang, X. Yuan, K. J. Dagan, P. Mellor, D. Drury, and A. Bloor, "Universal neutral point balancing algorithm for three-phase three-level converters with hybrid of zero-sequence signal injection and virtual zero-level modulation," in *IEEE Proc. Energy Conversion Congress and Exposition*, 2018.
[19] X. Yuan, Y. Li, and C. Wang, "Objective optimisation for multilevel neutral-point-clamped converters with zero-sequence signal control," *IET Power Electronics*, vol. 3, no. 5, pp. 755–763, 2010.
[20] H. Tian and Y. W. Li, "Carrier-based stair edge PWM (SEPWM) for capacitor balancing in multilevel converters with floating capacitors," *IEEE Transactions on Industry Applications*, vol. 54, no. 4, pp. 3440–3452, 2018.
[21] C. Xia, H. Shao, Y. Zhang, and X. He, "Adjustable proportional hybrid SVPWM strategy for neutral-point-clamped three-level inverters," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 10, pp. 4234–4242, 2013.
[22] S. Wang, W. Song, J. Zhao, and X. Feng, "Hybrid single-carrier-based pulse width modulation scheme for single-phase three-level neutral-point-clamped grid-side converters in electric railway traction," *IET Power Electronics*, vol. 9, no. 13, pp. 2500–2509, 2016.
[23] S. Mukherjee, S. K. Giri, and S. Banerjee, "An improved adjustable modulation strategy for three-level NPC inverters considering dynamic loading applications," *IEEE Transactions on Industry Applications*, vol. 55, no. 4, pp. 3915–3925, 2019.
[24] P. A. Dahono, Y. Sato, and T. Kataoka, "Analysis and minimization of ripple components of input current and voltage of PWM inverters," *IEEE Transactions on Industry Applications*, vol. 32, no. 4, pp. 945–950, 1996.
[25] I. Laird, X. Yuan, J. Scoltock, and A. Forsyth, "A design optimisation tool for maximising the power density of 3-phase DC-AC converters using Silicon Carbide (SiC) devices," *IEEE Transactions on Power Electronics*, vol. 33, no. 4, pp. 2913–2932, May 2017.

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