

Optimal Stack Layout in a Sea Container Terminal with Automated Lifting Vehicles

Abstract

Container terminal performance is largely determined by its design decisions, which include the number and type of quay cranes (QCs), stack cranes (SCs), transport vehicles, vehicle travel path, and stack layout. The terminal design process is complex because it is affected by factors such as topological constraints, stochastic interactions among the quayside, vehicle transport and stackside operations. Further, the orientation of the stack layout (parallel or perpendicular to the quayside) plays an important role in the throughput time performance of the terminals. Previous studies in this area typically use deterministic optimization or probabilistic travel time models to analyze the effect of stack layout on terminal throughput times, and ignore the stochastic interactions among the resources. It is unclear if stochastic interactions have an impact on the optimal stack layout. In this research, we capture the stochasticity with an integrated queuing network modeling approach to analyze the performance of container terminals with parallel stack layout using automated lifting vehicles (ALVs). Using this model, we investigate 1008 parallel stack layout configurations in terms of throughput times and determine the optimal stack layout configuration. We also find that, assuming an identical width of the internal transport area, container terminals with parallel stack layout perform better (from 4% - 12% in terms of container throughput times) than terminals with a perpendicular stack layout.

Keywords: Container terminals, Optimal stack layout, Parallel vs. perpendicular stack orientation, Seaside operations, Queuing model

1 Introduction

With over 90% of the global trade carried over sea, the maritime containerization market is projected to reach 731 Million TEU by 2017 (Jose [2012]). To cope with increased demand in maritime transportation, several new terminal development and expansion projects are underway. For instance, APM terminals are building new terminals in the Americas, Asia-Pacific, and Europe region such as in Moin, Costa Rica (Moin Container Terminal), Ningbo, China (Meishan Container Terminal Berths 3, 4, and 5), Rotterdam, Netherlands (Maasvlakte 2) (see *www.apmterminals.com*). Terminal expansion projects are also underway in Africa/Middle-east, Pacific Asia and the European region. The development costs of constructing or expanding a new deep water container terminal is significant (upto a billion euros depending on the number of berthing positions and degree of automation, Wiegmans et al. [2002]).

New terminals are adopting latest technology innovations, such as Quay Cranes (QCs) with a multi-trolley system at the quayside, Automated Lifting Vehicles (ALVs) or lift-automated guided vehicles (Lift-AGVs) for internal transport, and multiple RMG cranes per stack block at the stackside. Due to high investments and less flexibility to alter the terminal design at a later point, efficient designs of container terminals should be analyzed a-priori to achieve a high throughput performance. We limit the scope of this study to the three seaside processes: quayside, vehicle transport, and stackside.

The throughput performance of a terminal depends on multiple design and operational factors. The design factors include the topology of the vehicle travel path, overall area of the terminal, berthing capacity, terminal layout, stack layout, container handling equipment technology (such as the QC and SC technology used on the quayside and stackside respectively, and the yard vehicles used to transport the containers between the quayside and stackside). The operational factors include the container storage policies in the stack blocks, number of QCs and vehicles assigned for loading and discharge operations, equipment assignment rules for loading and discharging operations, and job dispatching policies. In this research, we particularly study the efficiency of stack layout designs that include multiple aspects such as 1) *orientation* of the stack blocks (parallel to the quay or perpendicular to the quay), 2) *number* of stack blocks for a fixed number of storage locations, 3) *organization* of the stack blocks (number of horizontal and vertical modules for the parallel stack layout), and 4) *dimensions* of each stack block, which is expressed as a function of number of rows per block, bays per block, and tiers per block.

Figure 1 illustrates a terminal with parallel and perpendicular stack layouts. While

some terminals in Asia (such as the terminal in Pusan, Korea) have parallel orientation of the stack blocks, other terminals in Europe (such as the ECT Delta terminal in Rotterdam) have perpendicular stack block orientation. The choice of the SC may also affect the choice of the layout. For instance, due to safety reasons, Rubber Tyred Gantry (RTGs) cranes are preferred for parallel stack layouts whereas RMG cranes are preferred for perpendicular layouts. Perpendicular layouts are good in decoupling the manual land-side from the automated seaside operations. One layout may also be preferred over the other depending on the performance measure of interest. For instance, Liu et al. [2004] show that the perpendicular layout is superior with respect to QC moves and the number of horizontal transporters needed whereas Kim et al. [2008] conclude that parallel layouts are superior to perpendicular layouts in respect to their objective which considers the costs for the expected average travelling distance of trucks and the costs for performing the expected number of container rehandles.

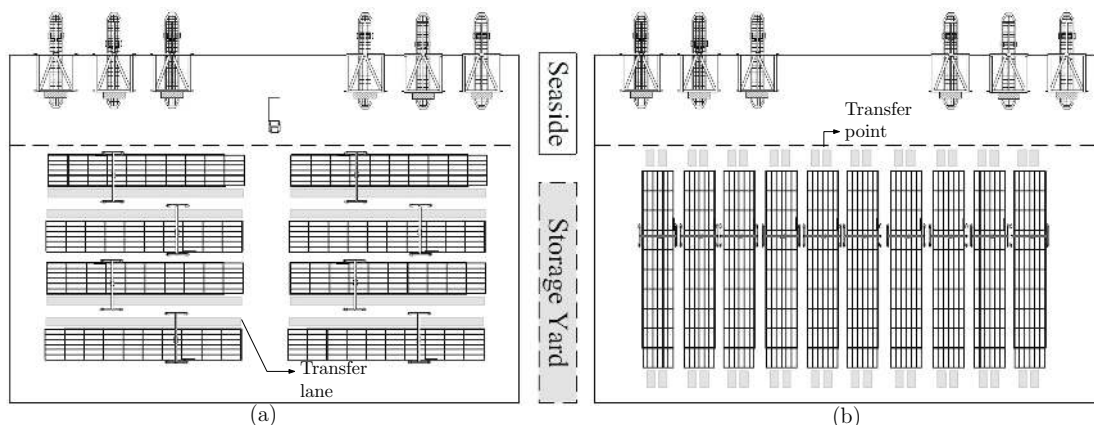


Figure 1: (a) Parallel stack layout with transfer lanes and (b) Perpendicular stack layout with transfer points (adapted from Wiese et al. [2011b])

In practice, the topological relationships between the stackside and the vehicle transport area may have a dominating effect on the stack layout performance. For instance, in Figure 2, we show two parallel stack layouts with the same number of container storage locations but with a different number of modules in the x-direction. If we have a parallel stack layout with a small number of short stack modules along the X-axis, then the number of blocks along the Y-axis increases. In this situation, vehicle travel time along the x-axis is short but the vehicle travel time along the Y-axis to either store or retrieve a container is long. On the other hand, in the second layout where we have a relatively large number of stack modules along the X-axis, vehicle travel time along the

X-axis is longer but the vehicle travel time along the Y-axis is shorter. Hence, there is a trade-off between the vehicle travel time along the X- and the Y-axis, which merits a detailed integrated analysis.

On arrival, the containers wait in the vessels for the discharge operation. The container is unloaded from the vessel by the QC and repositioned to a QC buffer lane for internal transport. The ALV picks up the load and transports it to the destination SC buffer lane. From the buffer lane, the SC transports the container to the stack storage location. During the discharge operations, the process output from the QCs for the unload operation forms the process input to the vehicle transport process. Likewise, the process output from the vehicle transport process forms the process input to the stackside process. These stochastic interactions can be captured in a queuing network model, which can handle process variabilities (in operation times and transaction inter-arrival times). We develop individual models of the quayside, the stackside, and the vehicle transport process for terminals with a parallel stack layout, and then integrate the sub-models using a parametric decomposition approach that relies on the first and the second moments of the inter-arrival and inter-departure times from the stations. Using this model, stack layout configurations with minimum container throughput times are obtained. Using the analytical model developed by Roy and De Koster [2012] for perpendicular stack layout, we compare the throughput time performance between a parallel and a perpendicular stack layout with the same number of storage locations while maintaining the same width for the internal transport area (see Figure 2). Two research questions, important for terminal design and management, are:

1. What is the optimal stack layout (number of bays, number of rows per bay, number of tiers) for a parallel stack layout?
2. Given a fixed number of storage locations and an identical width of the transport area, how does the throughput performance of a terminal with parallel stack layout compare with a terminal with perpendicular stack layout?

While the two research questions have been mostly studied using optimization formulations in a deterministic setting (Kim et al. [2008] and Lee and Kim [2010]), or using discrete-event simulation (Petering and Murty [2009] and Liu et al. [2004]) in a stochastic setting, we use integrated analytical models to determine efficient stack layouts using a stylized vehicle transport path. These analytical models allow for design factor optimization, which is difficult to perform using simulation. Our main contribution is the development of expressions for the transport times, and development of the analytical model for the container terminal operations that allows both stack layout optimization,

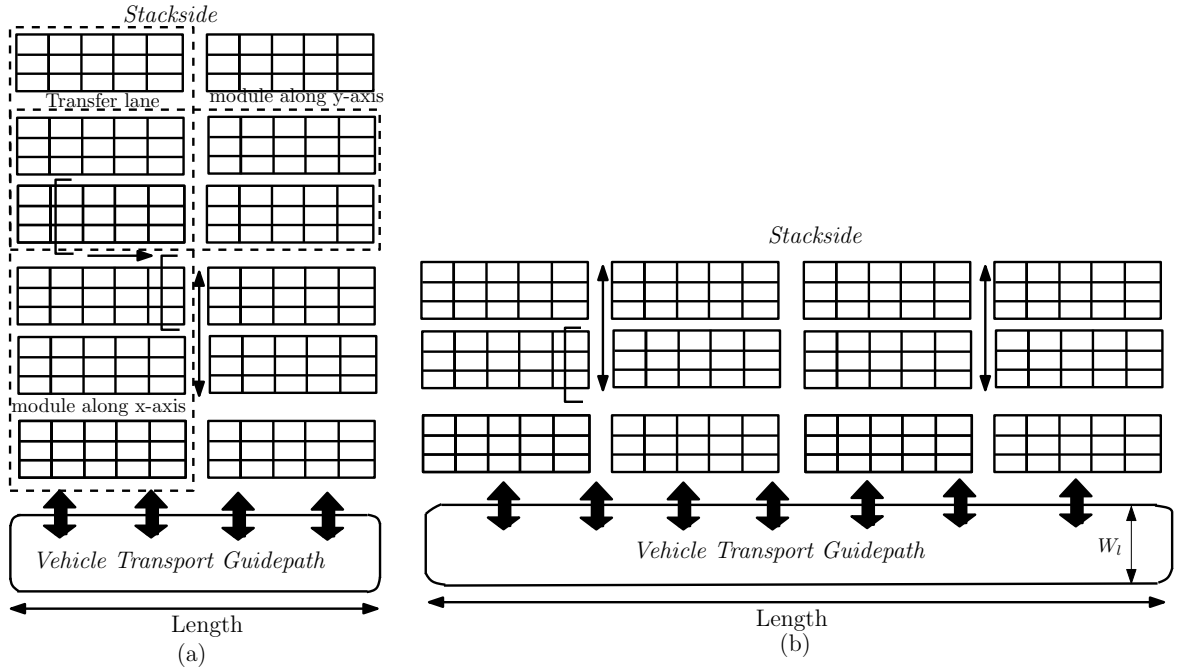


Figure 2: Top view of two parallel stack layouts (a) two modules in the x-direction and (b) four modules in the x-direction

and comparison of parallel and perpendicular stack layout performance. The rest of this paper is organized as follows. Section 2 reviews existing literature on layout optimization. In Section 3, the container terminal layout is described, which is followed by an explanation of the system model assumptions. The queuing network models for all the three isolated processes as well as the queuing model for the integrated system, are described in Section 4. Section 5 reports numerical experiments, using the model developed, which are validated using simulation models. Finally in Section 6, the research findings are summarized.

2 Literature Review

The contribution of our paper lies in two main areas: 1) obtaining efficient stack block layout designs, and 2) analyzing the performance of container terminals with parallel stack layouts using integrated analytical models. In this section, we review literature in these two areas.

Stack layout organization: Although several studies analyze stack layouts, the focus has mostly been restricted to space planning in the yards (Han et al. [2008]), container rehandling operations in yards (also known as the remarshaling problem, Caserta et al. [2011]), estimating SC handling times for different height, width, and block length (Lee et al. [2011]). Kim et al. [2008] develop an integer programming model to determine the layout type (parallel and perpendicular stack layouts), the yard layout, and the number of vertical and horizontal aisles in the stack by considering the stack layout interaction with both landside and seaside operations. With several numerical evaluations, they conclude that parallel layouts are superior to perpendicular layouts when the attempt is to minimize expected travel cost and expected container relocation (number of rehandles) costs using RTG cranes.

Liu et al. [2004] show that the perpendicular layout is superior with respect to QC moves and the number of horizontal transport vehicles needed. Petering and Murty [2009] develop a simulation model for a transshipment yard. They find out that in order to keep QCs busy and minimize the makespan of the schedule of ships, the block length should be limited between 56 and 72 TEU. Furthermore, the movements of the SC should be restricted to one block. Petering [2009a] extended the simulation study to include decision support for yard capacity, fleet composition, truck substitutability, and scalability issues. Wiese et al. [2011b] develop a decision support model to study parallel vs perpendicular stack layouts with different driving and compensation (loss of ground area due to additional transfer lanes) strategies. They conclude that both parallel and perpendicular layout may outperform each other under different design parameter settings. Kemme [2012] develops a simulation study to evaluate the effects of four RMG crane systems and 385 yard block layouts, differing in block length, width, and height, on the yard and terminal performance. Lee and Kim [2013] compare a perpendicular layout with a parallel layout considering different cost factors such as construction cost of the ground space, fixed overhead cost of yard cranes and the operating costs of yard cranes and transporters. They find that an optimal parallel stack layout has a large number of bays and a small number of rows in each stack block. They also determine that shorter and wider blocks are more efficient in a perpendicular layout. In addition, Lee and Kim [2013] state that a parallel layout requires a lower number of SCs and it performs superior to a perpendicular layout in terms of cost.

Performance models of container terminals: The existing models for container terminals are mostly limited to isolated systems, where the three major processes: quayside, vehicle transport and stackside operations, are analyzed as separate sub-systems. The studies typically use optimization and simulation models to address operational issues

such as scheduling of container storage and retrieval operations (Vis and Roodbergen [2009]). Some studies also evaluate decisions related to the design of isolated systems such as cost-tradeoffs and vehicle choice for internal transport (AGVs, ALVs, multiple trailers etc.). An overview of literature on container terminal modeling can be obtained from (Vis and De Koster [2003], Steenken et al. [2004], Gharehgozli et al. [2013], and Gorman et al. [2014]).

Integrated system models span over the entire seaside operation. In seaport container terminals, berth allocation, QC assignment, and QC scheduling problems are typically solved sequentially, which may not provide good quality solutions. To bridge this gap, Meisel and Bierwirth [2013] provide a framework for aligning all decisions in an integrated fashion. Vacca et al. [2013] present an exact branch and price algorithm for both the berth allocation problem and the berth allocation problem with QC assignment. Chen [2000] develops simulation models to analyze the impact of vehicle dispatching policies on the operation of a terminal. For example, Hoshino et al. [2005] use a combination of a closed queuing network and simulation model to propose an optimal design methodology of container terminals using AGVs for transportation. Bae et al. [2011] and Roy and De Koster [2012] compare the operational performance of an integrated system with two types of vehicles (ALVs and AGVs). In both researches, the authors show that an ALV network requires fewer vehicles than an AGV network for the same level of throughput as the former has self-lifting capacities. Simulation has been used often to design new terminals and to improve the efficiency of the existing terminals. TBA BV, a container terminal simulation and consultancy company uses 3D detailed simulation model for real terminal implementations across continents. However, optimizing design parameters using simulations is time consuming (see Edmond and Maggs [1978]).

In Table 1, we classify the literature on the impact of stack layout organization on performance, based on the choice of stackside equipment, scope of the research, performance measures, research outcome, and broad area of the solution approach. The paper closest to our work is that by Wiese et al. [2011b], as they also compare parallel and perpendicular stack layouts. They find the design configuration (terminal length, depth, vehicle velocity, and possible driving strategies) substantially affects the layout preference and show that the parallel stack layout outperforms the perpendicular stack layout for most parameter settings.

However, our work differs both in terms of scope and analysis approach. They minimize the estimated average straddle carrier cycle time i.e., the sum of the vehicle's time needed for stacking and for travelling from the quay to the designated storage block. However, we consider the new generation automated terminals with ALVs for internal

Table 1: Classification of stack layout literature where outcomes are *1: orientation, 2: number of stack blocks, 3: organization, and 4: dimension*

Article	Stackside equipment	Scope	Performance measures	Outcome	Approach
Liu et al. [2004]	Yard cranes with AGVs for both parallel and perpendicular stack	Seaside, Loading and Unloading	Throughput time	1,2,3	Simulation
Kim et al. [2008]	Transfer Crane (TCs) for both parallel and perpendicular stack	Seaside and Landside, Loading and Unloading	Expected travel distance of yard trucks	1,3,4	Optimization
Lee and Kim [2010]	RTGs or RMGs for both parallel and perpendicular stack	Seaside, Loading and Unloading	Optimal block size (Length, Height and Width of block)	1,4	Optimization
Petering [2009b]	RMGs for parallel stack	Seaside, Loading and Unloading	Gross Crane Rate (GCR): Average numbers of containers lift per hour by each QC	3,4	Simulation
Petering and Murty [2009]	RMGs for parallel stack	Seaside, Loading and Unloading	GCR	2,3	Simulation
Wiese et al. [2011a]	RMGs or RTGs for both parallel and perpendicular stack	Seaside and Landside Loading and Unloading	Minimize the time needed to store the containers into blocks	1,2	Optimization
Wiese et al. [2011b]	Straddle Carrier for both parallel and perpendicular	Seaside and Landside, Unloading	Minimize the estimated average straddle carrier cycle time for loading/unloading operation	1,2,3,4	Optimization
Lee and Kim [2013]	RMGs or RTGs for perpendicular and parallel stack	Seaside and Landside, Loading and Unloading	Installation cost and cycle time for loading/unloading operation	3,4	Optimization
<i>Our research</i>	RMGs for both parallel and perpendicular stack	Seaside, Unloading	Throughput time	1,2,3,4	Queuing, optimization

transport which are decoupled from the stackside process, and minimize the expected unload throughput time, which is the sum of the throughput times at the quayside, internal transport, and stackside processes. Further, they use a deterministic optimization approach whereas we use a queuing modeling approach combined with optimization in order to capture the impact of stochastic interaction (waiting times) between different systems.

3 Sea Container Terminal Layout Description

In this section, we describe the container handling operations and explain the integrated terminal layout considered for this research. We focus on seaside operations sketched in Figure 1. Seaside operations are common at all terminals, while landside operations do not always occur and can differ between terminals.

3.1 Seaside Operations

The transport between the QCs and the stack blocks is carried out by automated lifting vehicles (ALVs). We focus on the vessel unloading process and develop queuing models to determine overall terminal performance. The loading process is similar to unloading, except that the occurrence of events in this operation is reversed. Hence, terminals optimized for the unloading process are also optimal for the loading process.

The container unload operation at the seaside process consists of three steps: quayside, vehicle transport and stackside operations. In the quayside process, the QCs unload

the containers from the vessels and place them on a buffer location near the QC. These containers are then picked up by the ALVs and are transported to the stack yard where they are dropped off at the stackside buffer areas. The SCs then transfer these containers from the buffer locations and store them in stack blocks. The total throughput time taken to complete the transfer of one transaction (i.e., one container) includes both the waiting as well as the movement time incurred in all the three steps. At each process step, the containers may have to wait for resource availability. Most of the processes involve stochasticity. For example, the instants at which containers in the vessel are available for pickup by the QC are determined by operators on the deck, who have to remove container locks, container supports, and deck covers, and by the sequence in which containers are unloaded (determined by the schedule and the QC operator). Hence, a deterministic model to analyze the integrated operations may be intractable or lead to loss in solution accuracy. We therefore analyze the integrated operations using open queuing network models. We also develop customized travel time expressions for internal transport along the travel guide paths that include multiple shortcuts from quayside to stackside.

3.2 Integrated Terminal Layout

The layout studied is given in Figure 3. For the purpose of illustration, we consider a terminal with six QCs, 24 stack blocks and a main guide-path with six shortcut paths between the quayside and the stackside. The vehicle travel path topology along the stack blocks is based on data provided in Zhen [2013] and discussions with container terminal designers from two companies. We use only a single uni-directional horizontal transfer lane to reduce congestion. However, we use two uni-directional driving lanes along the y-axis to allow shortcuts and reduce travel times.

The stack yard is composed of several stack blocks that are arranged parallel to the quayside. The stacks are made accessible from the main travel loop by both the transfer lanes and the vertical driving lanes.

To develop the travel time expressions for internal transport, the stack blocks are grouped into stack modules along the X-axis and along the Y-axis. A stack module along the X-axis represents all stack blocks that align in a column along the X-axis while a stack module along the Y-axis includes two (or one) adjacent stack blocks taken along the Y-axis that share a common transfer lane as shown in Figure 3. Note that the first and the last module (along the Y-axis) have an exclusive transfer path and do not share this with other modules along the Y-axis (see Figures 2 and 3). In this container terminal layout, the total number of stack blocks, N_s equals 24. There are four stack modules

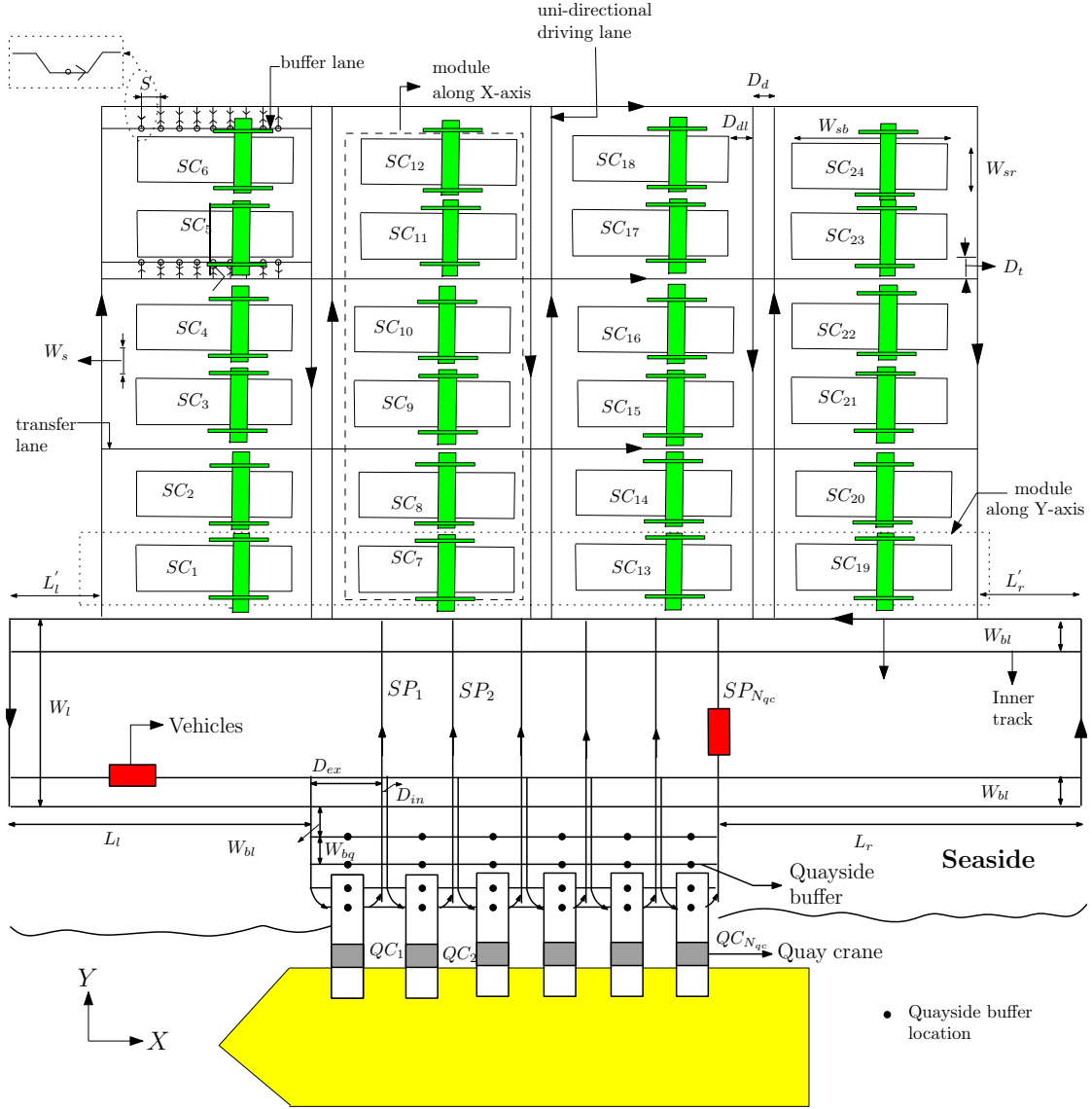


Figure 3: Illustration of the container terminal with parallel layout

along the X-axis ($N_{smx} = 4$) and four stack modules along the Y-axis ($N_{smy} = 4$). Note that the second and the third stack module along the Y-axis have a shared transfer lane.

Let N_{qc} be the number of QCs deployed to operate upon any one vessel. Each crane is denoted by QC_k where k represents the QC number. Also, each QC has its corresponding shortcut path connecting the main path between the quayside and the stackside. Both the stack blocks as well as the QCs have a set of buffer lanes that are used by the vehicles

or cranes to deposit the containers during the loading or unloading operations. Let N_{bq} and N_{bs} represent the number of buffer lanes for each QC and SC respectively. The other notations that are used to develop the vehicle travel time expressions are included in Table 2.

The next section describes the queuing network model for the unloading process when ALVs are used as the transport vehicles.

4 Queuing Network Model for Integrated Operations using ALVs and Parallel Stack Blocks

This section first describes the modeling assumptions and then define the queuing network models for the three different processes of quayside, vehicle transport and stackside operations. The integrated network model, which links the arrival and the departure process information from the three processes by a parametric decomposition approach, is described in the last subsection.

4.1 Model Assumptions

Quayside Process

We assume QCs are assigned to do only one type of operation (unloading). Each QC has only one trolley. The trolley has the capacity to unload one container at a time. Several sources of uncertainties influence the container availability at the quayside (for unloading); for instance, the time to unlash the containers on the vessel before discharging is highly variable (typically outsourced to a third-party company), the time to remove the hatch covers and open the twist locks varies, or a poor stowage plan at the port of origin can increase the number of container restows before the target container can be discharged. The large variability in the timing of individual container availability can be modeled using general inter-arrival process with λ_a denoting the arrival rate at the quayside for unloading containers. In addition, there is large variation in the QC service times. QC factors such as handling non-standard containers (such as 45 ft containers, reefer containers, tank containers, or flat-racks), the position of the container in the vessel, QC break-downs, and differences in skills between the crane crews, add to the discharge time variability. The QCs dwell at the point of service completion. Arriving containers are assigned to the QC with uniform probability.

Table 2: Notations used in the service time expressions for the vehicle transport (Refer Figure 3)

Term	Description
i	Index for an origin or destination stack module taken along X-axis
j	Index for an origin or destination stack module taken along Y-axis
k	Index for an origin or destination QC (shortcut path)
l	Index for an origin or destination buffer lane for the stack under consideration
W_{sb}	Length of a stack block along X-axis
W_{sr}	Length of a stack block along Y-axis
W_s	Distance between adjacent stacks belonging to different modules along the Y-axis
D_{dl}	Distance from the stack end taken horizontally to the adjoining driving lane along the X-axis
D_d	Distance between the two driving lanes within a pair along
D_t	Distance from the stack end to the adjoining transfer lane, taken along the Y-axis
W_l	Distance between the outer tracks of adjacent parallel lanes, one each on quayside and stackside along the Y-axis
W_{bl}	Distance between the outer and inner track along the Y-axis
W_{bq}	Distance between the adjacent buffer lanes at quayside
N_{bq}	Number of buffer lanes on quayside
N_{bs}	Number of buffer lanes corresponding to each stack
$N_{lbs}[k]$	Number of buffer lanes of the parallel stack that lies towards the left of the shortcut path k where $k \in \{1, \dots, N_{qc}\}$
X_e	Distance between the first buffer lane corresponding to a stack and the beginning of the stack or the distance between the last buffer lane corresponding to a stack and the stack end (along the X-axis)
L_r	Horizontal distance from the last shortcut path to the travel path on the right side
L_l	Horizontal distance from the first shortcut path to the travel path on the left side
L'_r	Distance from the last stack to the edge on the right side
L'_l	Distance between the first stack and the edge on the left side
D_{ex}	Distance between the entrance and exit of a shortcut path
D_{in}	Distance between the exit of one shortcut path and entrance to the consecutive path
N_{smx}	Number of stack modules taken along X-axis
N_{smy}	Number of stack modules taken along Y-axis
N_{qc}	Number of QCs, which is also the number of SP (assuming one shortcut path per QC)
$N_{srmx}[k]$	Number of stack modules taken along X-axis to the right of the shortcut path corresponding to origin QC taken along the X-axis
$kx[i][l]$	An index that gives the value of the shortcut path closest to the destination buffer lane, it depends on the value of i and l
$ky[i]$	An index that gives the value of the first shortcut path connected with any stack block, it depends on the value of i
S	The length of a buffer location on the stackside, it is given by the expression $(\frac{W_{sb}-2X_e}{N_{bs}})$
h_v	Vehicle velocity
N_s	Number of stack blocks
N_b	Number of bays per stack block
N_r	Number of rows per stack block
N_t	Number of tiers per stack block
L_q	The expected number of containers waiting at quayside
L_v	The expected number of ALVs waiting at quayside
L_s	The expected number of containers waiting at stackside
U_q	The expected utilization of quay cranes
U_v	The expected utilization of ALVs
U_s	The expected utilization of stack cranes
$\mathbb{E}[T_q]$	The expected throughput time for quayside operations
$\mathbb{E}[T_v]$	The expected throughput time for vehicle transfer process
$\mathbb{E}[T_s]$	The expected throughput time for stackside operations
$\mathbb{E}[CT_u]$	The expected throughput time to unload a container

Vehicle Transport

Though the QC buffer lane has finite capacity in practice, the ALVs park at a nearby location if they find a full QC buffer lane. Hence, we model the QCs with infinite buffer

capacity. Each vehicle transports only one container at a time. The vehicles dwell at the stackside buffer lanes after completing the unload transaction. The vehicles are dispatched on a first-come-first-serve policy. All travel paths are uni-directional. We also assume a stylized topology for the shortcut paths in which the number of shortcuts equals the number of QCs.

Stackside Process

The total number of storage locations is fixed; only the number of stack blocks N_s , the number of bays per stack N_b , the number of rows per stack N_r , and the number of tiers per stack N_t are varied to obtain a different stack configuration. Thus, a storage location for storing or retrieving a container is uniquely defined by a combination of four parameters. Similar to the QC, the SCs are assumed to dwell at the point of service completion. The SC stores or retrieves containers from the stack pile in a random fashion. Each stack block has only one SC. Similar to the QC buffer lane, we model the SC buffer lanes with infinite buffer capacity. Although we have made several seemingly limiting assumptions such as random storage of containers; our model can be extended in several directions such as considering skewed distribution of container assignment to the QCs, skewed storage location assignment etc.

4.2 Model Description

We develop the queuing models for the three sub-processes and then integrate these models using the arrival and departure information from the three sub-processes. Note that for a fair comparison between parallel and perpendicular stack layout analysis, we develop the integrated model using a similar approach that was adopted for a sea container terminal with perpendicular stack layout by [Roy and De Koster, 2012]).

Quayside Process

The objective of this queuing model is to estimate the performance measures and the squared coefficient of variation (SCV) of the inter-departure times ($c_{dq_i}^2$) from the QCs. The inputs provided to the model are: 1- The first and second moments of the inter-arrival times of containers to the QCs denoted by $\lambda_{aq_i}^{-1}$ and $c_{aq_i}^2$ respectively, 2- The first and second moments of QC service times denoted by $\mu_{q_i}^{-1}$ and $c_{sq_i}^2$ respectively. Each QC is modeled as a $GI/G/1$ queue with these input parameters. The performance measures such as utilization (U_{q_i}), time estimates of the number of containers waiting in queue (L_{q_i}), the expected throughput times for quayside operation ($E[T_{q_i}]$) and SCV of inter-departure times are evaluated using two moment approximation results of Whitt [1983].

Let the overall container arrival rate is λ_a ; due to the thinning process, the arrival

process to each QC is

$$\lambda_{a_{q_i}} = \frac{\lambda_a}{N_{qc}} \quad (1)$$

where N_{qc} is the number of QCs.

The QC utilization is given by

$$U_{q_i} = \frac{\lambda_{a_{q_i}}}{\mu_{q_i}} \quad (2)$$

The expected waiting time at the QC buffer lanes (corresponding to QC_i) is given by [Roy and De Koster, 2012]

$$WT_{q_i} = \left(\frac{\mu_{q_i}^{-1} U_{q_i}}{1 - U_{q_i}} \right) \left(\frac{c_{a_{q_i}}^2 + c_{s_{q_i}}^2}{2} \right) \quad (3)$$

The expected number of containers waiting in queue can be estimated using Little's law as

$$L_{q_i} = WT_{q_i} \lambda_{a_{q_i}} \quad (4)$$

The expected QC throughput time $\mathbb{E}[T_{q_i}]$ is given by

$$\mathbb{E}[T_{q_i}] = \mu_{q_i}^{-1} + WT_{q_i} \quad (5)$$

The SCV of inter-departure times from the QC_i is given by

$$c_{d_{q_i}}^2 = U_{q_i}^2 c_{s_{q_i}}^2 + (1 - U_{q_i}^2) c_{a_{q_i}}^2 \quad (6)$$

where $i = \{1, 2, \dots, N_{qc}\}$

Vehicle Transport Process

A fleet of ALVs transport the containers between the quayside and stackside through defined guide paths. The layout in Figure 3 has two tracks on the main guide path circuit. The outer track is used by the ALVs when they approach the buffer areas on the stackside or quayside while the inner tracks are used for intermediate travel and are provided to reduce congestion and to facilitate higher travel speeds. The objective of the vehicle transport queuing model is similar to that of the previous model except that the performance measures (utilization (U_v), time estimates of the number of containers waiting for the vehicles (L_v) and the expected throughput times for vehicle transport ($\mathbb{E}[T_v]$)) are estimated for the ALV network, the input parameters being the mean ($\lambda_{a_t}^{-1}$) and SCV ($c_{a_t}^2$) of container inter-arrival times and the mean (μ_t^{-1}) and SCV ($c_{s_t}^2$) of the

vehicle service times. The throughput time ($\mathbb{E}[T_v]$) of the vehicle transport includes travel time from stackside to quayside, waiting time for container at quayside, loading time of container, travel time from quayside to stackside and unloading time of container. First, the travel time expressions will be described. This is later followed by a description of the queuing network model.

Let the service time to complete one travel cycle be denoted by a random variable χ_t . Then, χ_t is given by the Equation 7.

$$\chi_t = \chi_{sq} + \chi_{lu} + \chi_{qs} \quad (7)$$

where, χ_{sq} , χ_{lu} , and χ_{qs} are the random variables corresponding to the travel between stackside to quayside, load or unload times, and travel time between quayside and stackside respectively.

Let μ_t^{-1} represent the mean service time to complete one travel cycle, where the service time is the sum of the expected travel time from stackside to quayside (T^{sq}), the container pick-up and drop-off time, L_t^v and U_t^v , which are deterministic in nature, and the expected travel time from quayside to stackside (T^{qs}). As stated earlier, the guide paths are uni-directional, refer Figure 3. Therefore, while travelling from the stackside to quayside only the main guide paths are used, whereas while travelling from the quayside to the stackside, the shortcut paths are also used. Further, in this model, the vehicle adopts the *shortest path* permissible to reach its destination.

The notations used in the service time expressions are listed in Table 2. We now discuss the approach to estimate the expected vehicle travel times. We first discuss the approach for estimating the travel times from stackside to quayside and then present the expressions for different travel time scenarios for travel between the quayside to the stackside. Note that the stack blocks present in the first stack module along the Y-axis are accessible directly from the main guide path and hence the vehicles do not travel an extra distance (along the Y-axis) of one stack module for reaching the stack buffer location. Further, to reach any of the stack blocks in modules other than the first stack module along the Y-axis, a distance of at least one stack module (along the Y-axis) has to be traversed, which is not required when the destination stack block is present in the first stack module along the Y-axis. Therefore, we develop the travel time expressions separately for stack blocks that are present in first stack module along the Y-axis and for the remaining stack blocks present in other stack modules. Also note that the travel time expression to reach any stack buffer location that belong to a particular stack module is the same even if they belong to different stack blocks. This relationship holds true

because stack blocks that belong to a module share the same transfer lane as shown in Figure 3.

Travel Time from Stackside to Quayside:

In this subsection, we explain the travel time expressions for an ALV to move from stackside to quayside. An ALV moves from stackside to quayside only via the main guide path. Depending on the stack block position, travel time expressions are derived.

As described earlier, all stack blocks are grouped in modules along the X and Y axis. From Figure 3, it can be seen that first stack module along the Y-axis is directly accessed via main guide path, while other stack modules require clockwise movement of ALVs. Hence, we develop the travel time expressions for these two cases separately. In Case I, the destination stack block lies other than the first stack module along the Y-axis and in Case II, the destination stack block lies in the first stack module along the Y-axis. The time expressions ($T_{c_1}^{sq}$ and $T_{c_2}^{sq}$ for Case I and Case II respectively) include the sum of travel time taken by possible travel routes (corresponding to the particular case) to reach the destination QC from a SC. After estimating the sum of travel times for all cases, we determine the average travel time by dividing the sum of total travel time by the number of all possible travel routes from stackside to the quayside.

Case I: When the stack blocks lie in the stack modules other than the first stack module along the Y-axis

Here, the range of the indices i, j, l and k indicates the stack module position along the X-axis, Y-axis, the buffer position at the stack block, and the QC index respectively ($i \in \{1, \dots, N_{smx}\}$, $j \in \{2, \dots, N_{smy}\}$, $l \in \{1, \dots, N_{bs}\}$ and $k \in \{1, \dots, N_{qc}\}$).

$$\begin{aligned}
T_{c_1}^{sq} = & \sum_{i=1}^{N_{smx}} \sum_{j=2}^{N_{smy}} \sum_{k=1}^{N_{qc}} \sum_{l=1}^{N_{bs}} \left(\frac{D_t}{2} + (N_{bs} - l)S + X_e + D_{dl} + i(W_{sb} + 2D_{dl} + D_d) - D_d \right. \\
& + (j - 1)(2D_t + 2W_{sr} + W_s) + L'_l + W_l + L_l + W_{bl} + W_{bq} \frac{(N_{bq} - 1)}{2} + (k - 1) \\
& \left. (D_{ex} + D_{in}) + \frac{D_{ex}}{2} + \frac{S}{2} \right) \frac{1}{h_v} \tag{8}
\end{aligned}$$

For instance, we consider the movement of an ALV from the l^{th} buffer of SC_{10} (that lies in the third stack module along the Y-axis) to QC_3 as shown in the layout (Figure 3). For this particular instance, the travel time expression is derived from Equation 8 (shown in Equation 9). In this scenario, the position of the origin stack block is in the second stack module ($i = 2$) along the X-axis and in the third stack module ($j = 3$) along the Y-axis respectively. The destination QC is QC_3 that implies $k = 3$. After unloading

the container at the stackside, the ALV travels $(\frac{D_t}{2} + \frac{S}{2} + (N_{bs} - l)S + X_e + D_{dl})$ units, right of the originating buffer lane, to reach the bi-directional driving lane. Now the ALV moves $(2(2D_t + 2W_{sr} + W_s))$ units along Y-axis and reach to main guide path. Now the ALV follows the main guide path and travels $(2(W_{sb} + 2D_{dl} + D_d) - D_d + L'_l + W_l + L_l)$ units along the guide path. Finally, the ALV reaches the assigned QC_3 after travelling $(2(D_{ex} + D_{in}) + W_{bq} \frac{(N_{bq}-1)}{2} + \frac{D_{ex}}{2})$ units.

$$T_{c_1}^{QC_{10}, SC_3} = \left(\frac{D_t}{2} + (N_{bs} - l)S + X_e + D_{dl} + 2(W_{sb} + 2D_{dl} + D_d) - D_d + 2(2D_t + 2W_{sr} + W_s) + L'_l + W_l + L_l + W_{bl} + 2(D_{ex} + D_{in}) + W_{bq} \frac{(N_{bq} - 1)}{2} + \frac{D_{ex}}{2} + \frac{S}{2} \right) \frac{1}{h_v} \quad (9)$$

Case II: When the stack blocks lie in the first stack module along the Y-axis

Here, the range of the indices i, j, l and k is $i = \{1, \dots, N_{smx}\}$, $j = 1$, $l = \{1, \dots, N_{bs}\}$, and $k \in \{1, \dots, N_{qc}\}$ respectively.

$$T_{c_2}^{sq} = \sum_{i=1}^{N_{smx}} \sum_{k=1}^{N_{qc}} \sum_{l=1}^{N_{bs}} \left(\frac{D_t}{2} + (l-1)S + X_e + D_{dl} + (i-1)(W_{sb} + 2D_{dl} + D_d) + L'_l + W_l + L_l + W_{bl} + W_{bq} \frac{(N_{bq}-1)}{2} + (k-1)(D_{ex} + D_{in}) + \frac{D_{ex}}{2} + \frac{S}{2} \right) \frac{1}{h_v} \quad (10)$$

For illustration, we consider the movement of an ALV from the l^{th} buffer of SC_7 that lies in the first stack module along the Y-axis to QC_3 with respect to the layout shown in Figure 3. For this particular instance, travel time expression can be derived from Equation 10 (as shown in Equation 11.)

In this case, the position of the origin stack block defined by the value of the indices i and j is 2 and 1 along the X and Y axes respectively. The k index takes the value 3 because the destination QC is QC_3 . Since first stack module along the Y-axis has a direct access to the main guide path, the ALV travels $(\frac{D_t}{2} + (l-1)S + X_e + D_{dl})$ units to reach to main guide path and then follows the guide path and travels $((W_{sb} + 2D_{dl} + D_d) + L'_l + W_l + L_l)$ units. Finally, the ALV arrives at the assigned QC_3 after travelling

$(2(D_{ex} + D_{in}) + W_{bq} \frac{(N_{bq}-1)}{2} + \frac{D_{ex}}{2})$ units.

$$T_{c_2}^{QC_7, SC_3} = \left(\frac{D_t}{2} + (l-1)S + X_e + D_{dl} + (W_{sb} + 2D_{dl} + D_d) + L'_l + W_l + L_l + W_{bl} + W_{bq} \frac{(N_{bq}-1)}{2} + 2(D_{ex} + D_{in}) + \frac{D_{ex}}{2} + \frac{S}{2} \right) \frac{1}{h_v} \quad (11)$$

To obtain T^{sq} , we need to take the average travel time over possible routes from all stack modules along X and Y-axis, buffer positions and QCs QC_n ($n \in \{1, 2, \dots, 6\}$).

Hence, the expected travel time by an ALV from a SC to a QC is given by Equation 12.

$$T^{sq} = \frac{1}{(N_{smx} \times N_{smy} \times N_{bs} \times N_{qc})} (T_{c_1}^{sq} + T_{c_2}^{sq}) \quad (12)$$

The approach to estimate the expected travel time from quayside to the stackside (T^{qs}) is presented in Appendix A.

Let μ_t^{-1} denotes the mean service time to complete one travel cycle, i.e, the cumulative sum of the expected travel time from the stackside to the quayside (T^{sq}), deterministic container pickup and drop time (deterministic times L_t^v and U_t^v), and expected travel time from quayside to the stackside T^{qs} . Note that we consider shortest path route information (from origin to destination location) to develop the service time expressions. Therefore, μ_t^{-1} , includes the minimum expected travel time required to travel from origin (quayside to stackside and return).

The final expression to estimate the expected vehicle travel time μ_t^{-1} is given by Equation 13.

$$\mu_t^{-1} = T^{sq} + T^{lu} + T^{qs} \quad (13)$$

where $T^{lu} = L_t^v + U_t^v$. The SCV of service time (c_{st}^2) is determined using Equation 14.

$$c_{st}^2 = \frac{\mathbb{E}[\chi_{sq} + \chi_{lu} + \chi_{qs}]^2 - (\mathbb{E}[\chi_{sq} + \chi_{lu} + \chi_{qs}])^2}{(\mathbb{E}[\chi_{sq} + \chi_{lu} + \chi_{qs}])^2} \quad (14)$$

For transporting the container from quayside to stackside, the container may wait for an ALV at the quayside. However, due to the capacity constraints of the QC, an ALV may also wait for container arrival. The interaction between ALVs and containers is precisely modeled using a $GI/G/V$ queue with V vehicles dedicated to internal transport between the quayside and the stackside. The SCV of the inter-departure times from the vehicle

transfer process is evaluated using two moment approximation results, Whitt [1983].

Other performance measures for vehicle transport such as vehicle utilization (U_v), expected container waiting time in the queue (W_v) and the expected throughput times ($\mathbb{E}[T_v]$) for vehicle transfer process, are estimated as follows.

The expected waiting time in queue is

$$W_v = \phi(U_v, c_{st}^2, c_{at}^2, V) \left(\frac{u^V U_v}{V! \lambda_{at} (1 - U_v)^2} \right) \left(\frac{c_{st}^2 + c_{at}^2}{2} \right) p_o, \quad (15)$$

where the terms p_o, u , and U_v are expressed as $\left(\frac{u^V}{V!(1-U_v)} + \sum_{n=0}^{V-1} \frac{u^n}{n!} \right)^{-1}$, $\frac{\lambda_{at}}{\mu_t}$, and $\frac{\lambda_{at}}{V\mu_t}$, respectively. The expression for ϕ can be found in Whitt [1983].

The expected throughput time $\mathbb{E}[T_v]$ is given by

$$\mathbb{E}[T_v] = \mu_t^{-1} + W_v \quad (16)$$

Note that the inter-departure time information from the vehicle transport process is required to determine the container inter-arrival times information to the stackside process. Hence, we also determine c_{dt}^2 using Equation 17.

$$c_{dt}^2 = 1 + (1 - U_v^2)(c_{at}^2 - 1) + \frac{U_v^2}{\sqrt{V}}(c_{st}^2 - 1) \quad (17)$$

Stackside Process

Let N_s , N_b , N_r and N_{bs} denote the number of SCs, number of bays per stack, number of rows per stack, and number of buffer lanes per stack. When ALVs set down the containers at the stackside, the containers wait at the destination stack buffer lanes for the SC to be available. Once the SC becomes available, the total time, the SC takes to store the container includes the movement time from the dwell point of the crane to the pick-up location, the container pick-up, movement time from the pick-up point to the drop-off location, and drop-off times.

The objective of the stackside process queuing model is to estimate the performance measures. The inputs are the first moment and the SCV of the container inter-arrival times to the SC queue denoted by $\lambda_{as_i}^{-1}$ and $c_{as_i}^2$ respectively, and the mean and SCV of the SC service times. The mean inter-arrival time to each SC ($\lambda_{as_i}^{-1}$) is $(\frac{\lambda_a}{N_s})^{-1}$; where N_s is number of SCs.

Let γ_s represent the random variable of service time for one SC cycle. Thus γ_s is given by the Equation 18

$$\gamma_s = \gamma_{sb} + \gamma_{lu} + \gamma_{bs} \quad (18)$$

where γ_{sb} , γ_{lu} and γ_{bs} are the random variables corresponding to the horizontal travel time from the dwell point to the pick-up point i.e., a stack buffer lane, the container pick-up and drop-off time and the horizontal travel time from the buffer lane to the container drop-off point.

The container storage location and the container pickup location (stack buffer lane) are assigned randomly. Thus the random selection of storage location follows a uniform distribution. Let x_{n_i} , y_{m_i} and x_{n_j} , y_{m_j} be the coordinates of origin and destination location corresponding to any particular stack block. Due to simultaneous movement of the crane along both the X and Y axis as shown in Figure 4, the horizontal travel time is given by the expression : $\max\left(\frac{|x_{n_i}-x_{n_j}|}{v_{sx}}, \frac{|y_{m_i}-y_{m_j}|}{v_{sy}}\right)$, where v_{sx} and v_{sy} denote the crane and the trolley velocity along the X- and Y- axis respectively.

Further, the value of the coordinates of the SC origin depends upon its dwell point, which is characterized by the indices (n_i) and (m_i) representing the bay number and the row number respectively. Similarly, the value of the coordinates of the pickup location is characterized by n_j and m_j where n_j denotes the buffer lane number and m_j takes a value of 1.

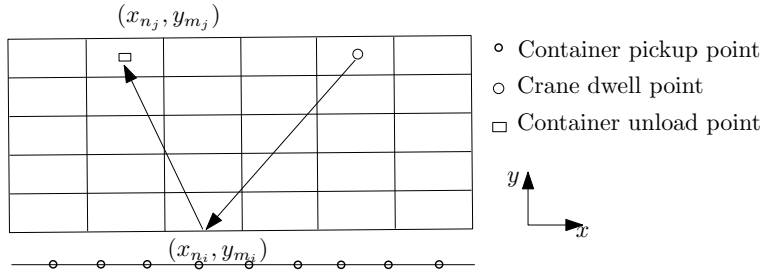


Figure 4: Travel trajectory of a SC during a container unload process

The container pick-up and drop-off times denoted by L_t^s and U_t^s , take into account the vertical travel time of the crane. The service time for the SCs has a mean $\mu_{s_i}^{-1}$, which depends upon the travel trajectory of the crane. The second moment of the service time is given by the expression $\mathbb{E}[\gamma_{sb} + \gamma_{lu} + \gamma_{bs}]^2$ and the SCV of service time ($c_{s_s}^2$) is given by the relation $\frac{\mathbb{E}[\gamma_{sb} + \gamma_{lu} + \gamma_{bs}]^2 - (2\mathbb{E}[\gamma_{sb}] + \mathbb{E}[\gamma_{lu}])^2}{(2\mathbb{E}[\gamma_{sb}] + \mathbb{E}[\gamma_{lu}])^2}$. Note that the random variables are assumed to be independent of each other. Since $\mathbb{E}[\gamma_{sb}] = \mathbb{E}[\gamma_{bs}]$, $\mu_{s_i}^{-1}$ can be written as:

$$\mu_{s_i}^{-1} = 2\mathbb{E}[\gamma_{sb}] + \mathbb{E}[\gamma_{lu}] \quad (19)$$

$$\mathbb{E}[\gamma_{sb}] = \sum_{n_i=1, m_i=1}^{n_i=N_b, m_i=N_r} \sum_{n_j=1, m_j=1}^{n_j=N_{bs}, m_j=1} \frac{1}{N_b N_r N_{bs}} \max\left(\frac{|x_{n_i} - x_{n_j}|}{v_{sx}}, \frac{|y_{m_i} - y_{m_j}|}{v_{sy}}\right) \quad (20)$$

$$\mathbb{E}[\gamma_{lu}] = L_t^s + U_t^s \quad (21)$$

Each SC is modeled as a $GI/G/1$ queue where the inter-arrival times are independent and identically distributed. Let $\mathbb{E}[T_s]$ represent the SC throughput time. The performance measures such as utilization (U_s), time estimates of the number of containers waiting in queue (L_s), the expected throughput times for the stackside operation ($\mathbb{E}[T_q]$) and SCV of inter-departure times are evaluated using two moment approximation results of Whitt [1983].

The SC utilization is determined by Equation 22.

$$U_{s_i} = \frac{\lambda_{a_{s_i}}}{\mu_{a_{s_i}}} \quad (22)$$

The expected waiting time at the SC is given by Equation 23.

$$WT_{s_i} = \left(\frac{\mu_{s_i}^{-1} U_{s_i}}{1 - U_{s_i}}\right) \left(\frac{c_{a_{s_i}}^2 + c_{s_{s_i}}^2}{2}\right) \quad (23)$$

The expected number of containers waiting in queue can be estimated using Little's law as expressed in Equation 24.

$$L_{s_i} = WT_{s_i} \lambda_{a_{s_i}} \quad (24)$$

The expected SC throughput time $\mathbb{E}[T_{s_i}]$ is given as

$$\mathbb{E}[T_{s_i}] = \mu_{s_i}^{-1} + WT_{s_i} \quad (25)$$

where $i = \{1, 2, \dots, N_s\}$

4.3 Integrated Model, Solution Approach, and Performance Measures

The integrated model is described in Figure 5. The containers are assigned to a $GI/G/1$ QC queue upon their arrival (in the vessel) and wait in the vessel until the QC becomes available. The mean and SCV of the inter-arrival times of the containers form the input

to this sub-queuing network. After this, the container is transported to the QC buffer lane (vehicle queue). The SCV of the inter-arrival times for the multi-server vehicle ($c_{a_t}^2$) queue is the aggregated SCV of the inter-departure times from the QC queues. The SCV of inter-departure times ($c_{d_{q_i}}^2$) from the QC queue is estimated using Equation 6. If there are N_{qc} QC queues, the departures from each of these queues are merged together to form the arrival stream to the vehicle queue (Equation 26). Once a vehicle is available, the vehicle is assigned to transport a container from the quayside to the stacks. Upon completion of the vehicle transport process, the container arrives at a $GI/G/1$ SC queue for storage in the stack block. The SCV of inter-arrival times for the SC equals the SCV of inter-departure times from the multi-server vehicle queue. The SCV of inter-departure times ($c_{d_t}^2$) from the vehicle queue is estimated using Equation 17. Since there are N_s SCs, the departures from the vehicle stations are split into N_s arrival streams (Equation 27 provides the SCV of inter-arrival time at each SC). The container unloading operation is completed once the SC stores the container in the stack block.

$$c_{a_t}^2 = \sum_{i=1}^{N_{qc}} \frac{\lambda_{a_{q_i}}}{\lambda_a} c_{d_{q_i}}^2 \quad (26)$$

$$c_{a_{s_i}}^2 = c_{d_t}^2 \left(\frac{1}{N_s} \right) + \left(1 - \frac{1}{N_s} \right) \quad (27)$$

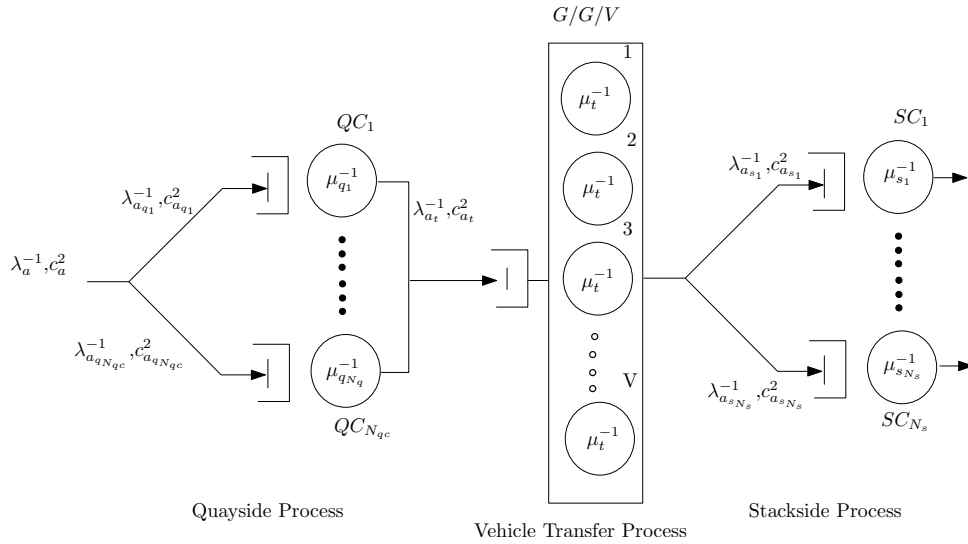


Figure 5: Integrated queuing network model for container unload process with ALVs

Table 3: Design of experiments for model validation (input)

Quayside	Vehicle Transport	Stackside
6 QCs	18, 20 ALVs	16 stacks ($1149 \times 110 \text{ m}^2$), 24 stacks ($1149 \times 170 \text{ m}^2$),
Service time: 120 sec (CV=0.3)	velocity: 6 m/s	Trolley velocity: 1 m/s and Crane velocity: 4 m/s
4 buffer lanes per QC		8 buffer lanes per SC

The expected throughput time to unload a container $\mathbb{E}[CT_u]$ is given by Equation 28.

$$\mathbb{E}[CT_u] = WT_{q_i} + \mu_q^{-1} + W_v + \mu_t^{-1} + WT_{s_i} + \mu_s^{-1} \quad (28)$$

5 Numerical Experiments and Layout Comparison

The data behind the terminal layout with parallel stacks, which include the speed of the ALVs, SCs, QCs, clearance between the stack blocks etc., are obtained from the APM Terminal operation in Rotterdam. The input data for our numerical experiments are included in Table 3. The analytical model is validated using a simulation model, which is developed using ARENA 12.0. The simulation has a run time of 50 days with a 2 day warmup period. The warmup period is taken such that any initial bias, due to system startup conditions such as the starting location of vehicles and cranes, is eliminated. The detailed flowchart of the simulation model is explained in Appendix B. The container arrival rates vary at 10 different levels such that vehicle/QC utilization lies between 60%-90%. Results can be found in Table 4- 7. Each simulation experiment is run for 15 replications with a 1 day warmup period and 20 day run time. The confidence intervals for the performance measures are within 3% of the means.

The performance measures considered are the expected throughput time for each of the three processes of quayside ($\mathbb{E}[T_q]$), vehicle transport ($\mathbb{E}[T_v]$) and stackside ($\mathbb{E}[T_s]$) operations, the utilizations of the QCs (U_q), vehicles (U_v) and SCs (U_s) and the average number of containers waiting in the queues at the quayside (L_q), at quay buffer lanes (L_v) and at the stackside buffer lanes (L_s). The percentage error in each of the performance measures was obtained by the expression $\left(\left| \frac{A-S}{S} \right| \times 100 \right)$ where A and S correspond to the measures obtained from the analytical and simulation models respectively. The average percentage errors for all of the performance measures are taken over all the different configurations.

From Tables 4-7, we see that the percentage errors are quite lower (upto 5%) for the expected throughput times and resource utilization. However, the errors are somewhat

larger upto 10% for expected queue length measures. The average errors in expected queue length at the quayside and the stackside are about 2.8% and 5.1% respectively. The average errors in the QC, vehicle, and SC utilizations are about 0.5%, 0.5%, and 0.9% respectively. The average errors in the expected throughput times for the quay, vehicle transport, and stack operations are 1.8%, 0.7% and, 0.9% respectively.

Table 4: Comparison of analytical and simulation results for a layout with 24 stack blocks and 20 vehicles

Parameters $\lambda(\text{containers/hr})$	Analytical Results												Simulation Results												Error											
	Quayside				Vehicle Transfer				Stackside				Quayside				Vehicle Transfer				Stackside				Quayside				Vehicle Transfer				Stackside			
	L_q	U_q	$\mathbb{E}[T_q]$	$\mathbb{E}[CT_q]$	L_v	U_v	$\mathbb{E}[T_v]$	$\mathbb{E}[CT_v]$	L_s	U_s	$\mathbb{E}[T_s]$	$\mathbb{E}[CT_s]$	L_q	U_q	$\mathbb{E}[T_q]$	$\mathbb{E}[CT_q]$	L_v	U_v	$\mathbb{E}[T_v]$	$\mathbb{E}[CT_v]$	L_s	U_s	$\mathbb{E}[T_s]$	$\mathbb{E}[CT_s]$	L_q	U_q	$\mathbb{E}[T_q]$	$\mathbb{E}[CT_q]$	L_v	U_v	$\mathbb{E}[T_v]$	$\mathbb{E}[CT_v]$	L_s	U_s	$\mathbb{E}[T_s]$	$\mathbb{E}[CT_s]$
126	4.90	70%	260.0	0.08	72%	412.6	0.12	11%	76.4	749.0	4.92	70%	257.7	0.01	73%	412.5	0.12	10%	76.9	747.0	0.41%	0.00%	0.91%	0.96%	0.02%	0.41%	0.00%	0.91%	0.96%	0.02%	7.03%	6.23%	0.64%	0.26%		
129	5.38	72%	270.5	0.10	73%	413.1	0.13	11%	76.4	760.0	5.20	71%	268.6	0.02	74%	412.5	0.12	11%	76.8	757.8	3.49%	0.70%	0.72%	0.34%	0.14%	7.26%	0.47%	0.40%	0.53%	0.29%						
131	5.92	73%	282.2	0.12	75%	413.6	0.13	11%	76.5	772.3	6.06	73%	286.3	0.03	76%	413.1	0.15	11%	76.9	776.3	2.29%	0.00%	1.41%	0.81%	0.11%	7.24%	0.71%	0.53%	0.52%							
134	6.53	75%	295.3	0.14	76%	414.2	0.14	11%	76.6	786.1	6.30	74%	287.1	0.04	76%	413.3	0.15	11%	77.1	777.5	3.65%	0.68%	2.85%	0.63%	0.22%	7.13%	0.95%	0.66%	1.11%							
137	7.22	76%	310.0	0.17	78%	414.9	0.15	12%	76.7	801.6	7.32	76%	308.7	0.05	79%	413.4	0.16	11%	77.1	799.2	1.37%	0.66%	0.41%	0.68%	0.37%	7.27%	3.91%	0.55%	0.30%							
140	8.01	78%	326.7	0.21	80%	415.6	0.15	12%	76.8	819.1	8.70	77%	333.0	0.07	80%	414.4	0.16	12%	77.3	824.7	7.95%	0.65%	1.91%	0.62%	0.31%	6.41%	3.33%	0.67%	0.68%							
142	8.92	79%	345.7	0.25	81%	416.5	0.16	12%	76.9	839.1	9.00	79%	344.8	0.09	82%	414.2	0.18	12%	77.4	836.5	0.94%	0.00%	0.26%	0.56%	0.56%	9.07%	0.92%	0.73%	0.31%							
145	9.97	81%	367.7	0.29	83%	417.6	0.17	12%	77.0	862.2	9.36	80%	357.3	0.11	83%	414.9	0.18	12%	77.6	849.7	6.51%	0.63%	2.91%	0.03%	0.65%	6.39%	0.14%	0.79%	1.47%							
148	11.21	82%	393.3	0.34	84%	418.7	0.17	12%	77.0	889.1	10.80	82%	397.7	0.17	85%	416.4	0.18	12%	77.6	891.7	3.77%	0.00%	1.10%	0.57%	0.56%	5.40%	0.36%	0.75%	0.29%							
150	12.68	84%	423.6	0.41	86%	420.1	0.18	13%	77.1	920.8	12.60	84%	424.4	0.26	86%	418.2	0.19	13%	77.7	920.3	0.61%	0.00%	0.19%	0.75%	0.46%	5.45%	0.22%	0.70%	0.06%							
153	14.45	85%	460.0	0.48	87%	421.6	0.19	13%	77.2	958.9	14.40	85%	476.6	0.32	88%	420.0	0.20	13%	77.7	974.3	0.35%	0.00%	3.48%	0.92%	0.39%	5.33%	0.00%	0.58%	1.58%							

Table 5: Comparison of analytical and simulation results for a layout with 24 stack blocks and 18 vehicles

Parameters $\lambda(\text{containers/hr})$	Analytical Results												Simulation Results												Error											
	Quayside				Vehicle Transfer				Stackside				Quayside				Vehicle Transfer				Stackside				Quayside				Vehicle Transfer				Stackside			
	L_q	U_q	$\mathbb{E}[T_q]$	$\mathbb{E}[CT_q]$	L_v	U_v	$\mathbb{E}[T_v]$	$\mathbb{E}[CT_v]$	L_s	U_s	$\mathbb{E}[T_s]$	$\mathbb{E}[CT_s]$	L_q	U_q	$\mathbb{E}[T_q]$	$\mathbb{E}[CT_q]$	L_v	U_v	$\mathbb{E}[T_v]$	$\mathbb{E}[CT_v]$	L_s	U_s	$\mathbb{E}[T_s]$	$\mathbb{E}[CT_s]$	L_q	U_q	$\mathbb{E}[T_q]$	$\mathbb{E}[CT_q]$	L_v	U_v	$\mathbb{E}[T_v]$	$\mathbb{E}[CT_v]$	L_s	U_s	$\mathbb{E}[T_s]$	$\mathbb{E}[CT_s]$
108	2.70	60%	210.0	0.07	68%	412.6	0.09	9%	75.8	698.4	2.64	60%	209.5	0.03	69%	413.9	0.10	9%	76.2	699.1	2.22%	0.00%	0.24%	0.87%	0.33%	6.56%	0.49%	0.51%	0.10%							
112	3.03	62%	217.9	0.09	71%	413.3	0.10	9%	75.9	707.1	2.94	62%	216.0	0.03	71%	413.5	0.10	9%	76.3	705.8	3.12%	0.00%	0.24%	0.87%	0.33%	6.84%	0.10%	0.50%	0.18%							
115	3.41	64%	226.7	0.13	73%	414.2	0.10	10%	76.0	716.9	3.40	64%	227.1	0.06	74%	414.3	0.11	10%	76.4	717.8	0.39%	0.00%	0.18%	1.17%	0.01%	6.83%	0.90%	0.48%	0.11%							
119	3.84	66%	236.5	0.17	75%	415.4	0.11	10%	76.1	728.0	3.78	66%	237.4	0.08	75%	414.8	0.12	10%	76.6	728.8	1.65%	0.00%	0.38%	0.94%	0.14%	8.04%	0.84%	0.56%	0.10%							
122	4.34	68%	247.5	0.22	78%	416.9	0.12	10%	76.3	740.6	4.47	68%	251.9	0.11	78%	415.5	0.12	10%	76.7	742.1	3.11%	0.00%	1.76%	0.92%	0.32%	6.97%	1.16%	0.55%	0.46%							
126	4.90	70%	260.0	0.29	80%	418.7	0.12	11%	76.4	755.1	4.80	70%	258.9	0.17	80%	417.0	0.14	11%	76.8	754.8	2.04%	0.71%	0.41%	0.27%	0.41%	9.54%	0.22%	0.61%	0.31%							
130	5.55	72%	274.3	0.39	82%	421.1	0.13	11%	76.5	771.9	5.55	72%	273.6	0.29	83%	420.0	0.14	11%	76.9	770.5	0.08%	0.00%	0.25%	0.65%	0.26%	3.19%	0.24%	0.56%	0.18%							
133	6.32	74%	290.8	0.51	84%	424.1	0.14	11%	76.6	791.5	6.24	74%	283.4	0.36	84%	421.8	0.15	11%	77.1	782.2	1.24%	0.68%	2.54%	0.17%	0.55%	6.72%	0.27%	0.61%	1.17%							
137	7.22	76%	310.0	0.68	87%	428.1	0.15	12%	76.7	814.8	6.90	75%	307.4	0.58	87%	427.4	0.15	11%	77.2	812.0	4.43%	0.79%	0.83%	0.03%	0.16%	3.53%	2.03%	0.58%	0.34%							
140	8.30	78%	332.7	0.91	89%	433.6	0.16	12%	76.8	843.1	8.22	78%	332.3	0.95	89%	438.9	0.17	12%	77.3	848.4	0.92%	0.64%	0.13%	0.11%	1.23%	2.00%	0.57%	0.63%								
144	9.60	80%	360.0	1.25	91%	441.6	0.16	12%	76.8	878.5	9.00	79%	342.1	1.32	91%	445.3	0.17	12%	77.3	864.7	6.25%	1.23%	4.98%	0.20%	0.84%	5.40%	0.48%	1.58%								

Table 6: Comparison of analytical and simulation results for a layout with 16 stack blocks and 20 vehicles

Parameters $\lambda(\text{containers/hr})$	Analytical Results												Simulation Results												Error											
	Quayside				Vehicle Transfer				Stackside				Quayside				Vehicle Transfer				Stackside				Quayside				Vehicle Transfer				Stackside			
	L_q	U_q	$\mathbb{E}[T_q]$	$\mathbb{E}[C_{T,q}]$	L_s	U_s	$\mathbb{E}[T_s]$	$\mathbb{E}[C_{T,s}]$	L_q	U_q	$\mathbb{E}[T_q]$	$\mathbb{E}[C_{T,q}](\text{sec})$	L_s	U_s	$\mathbb{E}[T_s]$	$\mathbb{E}[C_{T,s}](\text{sec})$	L_q	U_q	$\mathbb{E}[T_q]$	$\mathbb{E}[C_{T,q}](\text{sec})$	L_s	U_s	$\mathbb{E}[T_s]$	$\mathbb{E}[C_{T,s}](\text{sec})$	L_q	U_q	$\mathbb{E}[T_q]$	$\mathbb{E}[C_{T,q}](\text{sec})$	L_s	U_s	$\mathbb{E}[T_s]$	$\mathbb{E}[C_{T,s}](\text{sec})$				
126	4.90	70%	260.0	0.06	70%	400.1	0.19	16%	78.4	738.5	4.50	69%	253.3	0.01	69%	399.4	0.19	16%	79.0	731.7	8.89%	1.45%	2.63%	1.05%	0.17%	1.25%	2.47%	0.75%	0.92%							
130	5.55	72%	274.3	0.07	72%	400.5	0.21	16%	78.6	753.4	5.52	73%	276.2	0.02	73%	400.2	0.22	17%	79.5	773.5	0.65%	0.00%	0.69%	1.08%	0.07%	2.14%	0.55%	0.96%	6.74%							
133	6.32	74%	290.8	0.10	74%	401.0	0.22	17%	78.8	770.6	6.36	74%	291.2	0.02	74%	400.3	0.22	17%	79.5	773.5	0.65%	0.00%	0.69%	1.08%	0.07%	2.14%	0.55%	0.96%	6.74%							
137	7.22	76%	310.0	0.12	76%	401.7	0.23	17%	79.0	790.6	6.90	75%	304.6	0.02	76%	400.6	0.25	17%	79.6	784.0	4.61%	1.33%	1.76%	1.27%	0.28%	5.57%	0.58%	0.83%	0.85%							
140	8.30	78%	332.7	0.16	78%	402.4	0.25	18%	79.2	814.3	8.28	78%	322.3	0.04	78%	400.9	0.26	18%	80.0	802.7	0.20%	0.05%	3.24%	0.03%	0.39%	6.66%	0.32%	1.06%	1.45%							
144	9.60	80%	360.0	0.19	80%	403.3	0.26	18%	79.4	842.6	8.90	80%	333.3	0.04	79%	400.9	0.28	18%	80.1	819.7	7.87%	0.63%	6.09%	0.36%	0.59%	5.83%	0.61%	0.95%	2.79%							
148	11.21	82%	393.3	0.24	82%	404.3	0.28	19%	79.6	877.2	11.16	82%	393.5	0.07	82%	401.0	0.29	19%	80.3	874.7	4.01%	0.61%	0.03%	0.04%	0.82%	4.36%	0.36%	0.86%	0.28%							
151	13.23	84%	435.0	0.29	84%	405.5	0.29	19%	79.8	920.2	12.72	84%	421.2	0.02	84%	401.7	0.30	19%	80.5	903.5	4.01%	0.48%	3.27%	0.09%	0.93%	4.35%	0.41%	0.89%	1.85%							
155	15.85	86%	488.6	0.36	86%	406.8	0.31	20%	80.0	975.3	15.30	86%	487.5	0.16	86%	404.1	0.34	20%	80.8	971.5	3.59%	0.00%	0.21%	0.56%	0.67%	8.72%	0.12%	1.07%	0.39%							
158	19.36	88%	560.0	0.44	88%	408.4	0.32	20%	80.2	1048.5	18.66	88%	526.6	0.12	87%	404.7	0.35	20%	81.2	1014.8	3.75%	0.00%	0.57%	5.75%	0.41%	0.90%	8.18%	1.17%	1.20%	3.32%						
162	24.30	90%	660.0	0.53	90%	410.2	0.34	20%	80.4	1150.6	24.06	90%	664.0	0.35	90%	407.3	0.37	20%	81.1	1152.5	1.00%	0.00%	0.61%	0.61%	0.70%	7.52%	2.44%	0.85%	0.16%							

Table 7: Comparison of analytical and simulation results for a layout with 16 stack blocks and 18 vehicles

Parameters $\lambda(\text{containers/hr})$	Analytical Results												Simulation Results												Error											
	Quayside				Vehicle Transfer				Stackside				Quayside				Vehicle Transfer				Stackside				Quayside				Vehicle Transfer				Stackside			
	L_q	U_q	$\mathbb{E}[T_q]$	$\mathbb{E}[C_{T,q}]$	L_s	U_s	$\mathbb{E}[T_s]$	$\mathbb{E}[C_{T,s}]$	L_q	U_q	$\mathbb{E}[T_q]$	$\mathbb{E}[C_{T,q}](\text{sec})$	L_s	U_s	$\mathbb{E}[T_s]$	$\mathbb{E}[C_{T,s}](\text{sec})$	L_q	U_q	$\mathbb{E}[T_q]$	$\mathbb{E}[C_{T,q}](\text{sec})$	L_s	U_s	$\mathbb{E}[T_s]$	$\mathbb{E}[C_{T,s}](\text{sec})$	L_q	U_q	$\mathbb{E}[T_q]$	$\mathbb{E}[C_{T,q}](\text{sec})$	L_s	U_s	$\mathbb{E}[T_s]$	$\mathbb{E}[C_{T,s}](\text{sec})$				
112	3.03	62%	217.9	0.07	69%	400.6	0.15	14%	77.7	696.2	2.94	62%	214.4	0.16	68%	399.5	0.16	14%	78.3	692.2	3.22%	0.81%	1.63%	0.91%	0.27%	4.46%	0.81%	0.82%	0.57%							
115	3.41	64%	226.7	0.09	71%	401.3	0.16	15%	77.9	705.8	3.22	63%	222.3	0.03	70%	400.1	0.18	14%	78.5	700.5	6.00%	1.59%	1.59%	1.19%	0.27%	8.88%	1.17%	0.81%	0.76%							
119	3.84	66%	236.5	0.12	73%	402.1	0.17	15%	78.0	716.6	3.78	65%	233.6	0.05	73%	400.5	0.18	15%	78.8	712.9	1.68%	1.54%	1.22%	0.23%	0.40%	5.83%	0.83%	0.92%	0.53%							
122	4.34	68%	247.5	0.16	75%	403.2	0.18	15%	78.2	728.9	4.08	68%	240.9	0.07	75%	401.1	0.20	15%	79.0	721.0	6.25%	0.00%	2.73%	0.43%	0.51%	6.72%	0.51%	0.96%	1.09%							
126	4.90	70%	260.0	0.21	77%	404.5	0.19	16%	78.4	742.9	4.98	70%	261.1	0.10	78%	402.5	0.21	16%	79.3	746.0	1.61%	0.43%	1.57%	0.29%	0.48%	6.37%	0.22%	1.06%	0.41%							
130	5.55	72%	274.3	0.28	80%	406.1	0.21	16%	78.6	759.0	5.52	72%	273.8	0.17	80%	404.6	0.22	17%	79.4	756.8	0.62%	0.00%	0.35%	0.32%	0.38%	7.53%	0.67%	0.95%	0.30%							
133	6.32	74%	290.8	0.36	82%	408.1	0.22	17%	78.8	777.7	6.31	73%	291.0	0.17	82%	404.6	0.24	17%	79.5	792.8	0.10%	1.09%	0.09%	0.12%	0.87%	6.46%	0.27%	0.89%	1.91%							
137	7.22	76%	310.0	0.47	84%	410.7	0.23	17%	79.0	799.7	7.08	76%	305.5	0.29	84%	407.7	0.24	17%	79.7	792.8	1.98%	0.66%	1.49%	0.61%	0.73%	2.76%	0.58%	0.83%	0.86%							
140	8.30	78%	332.7	0.61	86%	414.0	0.25	18%	79.2	825.9	8.40	78%	345.0	0.46	87%	411.8	0.26	18%	79.8	836.7	1.23%	0.00%	3.56%	0.43%	0.52%	5.61%	0.25%	0.80%	1.29%							
144	9.60	80%	360.0	0.80	89%	418.3	0.26	18%	79.4	857.7	9.60	80%	350.0	0.64	88%	416.0	0.28	18%	80.3	855.3	0.00%	0.00%	0.00%	0.28%	0.51%	0.56%	7.19%	1.17%	1.11%	0.28%						
148	11.21	82%	393.3	1.07	91%	424.5	0.28	19%	79.6	897.4	10.60	81%	379.5	1.13	90%	428.0	0.30	18%	80.4	887.9	5.72%	0.86%	3.65%	0.61%	0.82%	6.50%	1.45%	1.00%	1.07%							

5.1 Optimal Terminal Layout with Parallel Stacks

This section describes the numerical experiments to optimize the stackside terminal layout when ALVs are used as the mode of transport from the quayside to stackside. We consider the influence of different stack layout parameters values i.e., N_{smx} , N_{smy} , N_t , N_b and N_s , on throughput times ($\mathbb{E}[CT_u]$) for the parallel stack layout. In all scenarios, we vary these stack layout parameters. Other design parameters such as the number of ALVs and the total number of stack locations remain unchanged. We perform experiments with two levels of the number of ALVs: 15 and 20 and two arrival rates for the containers 108 and 126 containers/hr. We identify efficient stack layouts for: 28800, 36000, and 48000 stack storage locations. Therefore, we consider a design of 12 ($3 \times 2 \times 2$) experiments. For each experiment, we vary the number of stack blocks, the stack modules, and the design parameters of each stack block such as the number of rows, number of tiers, and number of bays per stack block.

The number of stack blocks is varied between 4 and 32 with increments of 4 such that the number of stack modules along the X-axis, N_{smx} is varied between 2 and 8 with increments of 2. The number of rows per stack is varied between 4 and 10 with increments of 1. The number of tiers is varied between 3 and 5 with increments of 1. With these design constraints, different configurations were evaluated using the integrated analytical model. The layout configurations are ranked in an increasing order of expected total throughput times ($\mathbb{E}[CT_u]$).

Table 8 lists five high-performing configurations of container layout based on shortest throughput times ($\mathbb{E}[CT_u]$) and Table 9 lists five low-performing configurations that result in large throughput times ($\mathbb{E}[CT_u]$) with a total of 28,800 stack locations and 15 ALVs. We now summarize the results for the parallel stack layout.

The organization of the stack blocks in X and Y- axis with respect to the quay affects the throughput performance. In Table 8, for the shortest throughput ($\mathbb{E}[CT_u]$) case, the number of stack blocks along the X-axis is 2 and the number of stack blocks along the Y-axis is 9. The throughput time increases as the number of modules along the X-axis increases. In this research, we also estimate the number of stack blocks that are required to store the fixed number of containers. Each stack module along the Y-axis has two stack blocks except the first and the last module, which each contains one stack block. The total number of stack blocks is given by $N_{smx} \times (2N_{smy} - 2)$. For this particular instance ($N_{smx} = 2$ $N_{smy} = 9$) the total number of stack blocks is 32 (2×16).

Each stack block has a specific length, width and height that depends on the number of rows, bays and tiers respectively. The model also provides information about the

impact of different combinations of rows, bays and tiers on throughput time. Here, N_r , N_b and N_t denote the number of rows, the number of bays and the number of tiers respectively.

Table 8, shows that the shortest throughput time ($\mathbb{E}[CT_u]$)=597 sec is given by a stack layout with two modules along the X-axis, nine modules along the Y-axis, and 10, 18, and 5 rows, bays and tiers respectively. Therefore, each block has 900 containers (10). In general, we observe that a smaller number of stack modules along the X-axis and larger number of modules along the Y-axis yields better throughput time performance. From Table 9, we can see that for the low performing stack layout, the expected throughput time is 1592 sec corresponding to six stack modules along the X-axis and three stack modules along the Y-axis respectively.

Tables 10 and 11 list five high performing and five low performing stack layout configurations respectively for 36,000 stack locations. High performance stack layout configuration consists two stack modules along X-axis and nine stack modules along Y-axis. Throughput time for the high configuration is 624 sec. However, throughput time for the low performing stack layout configuration is 1537 sec with two and eight stack modules along X and Y-axis respectively. The main difference between high and low-performing designs is therefore not only determined by the number of modules along the X- or Y-axis, but also by the width and length of the individual blocks. The poor performing layout has long but narrow blocks, whereas the high performing layout has wide, shorter blocks.

Similarly, Tables 12 and 13 list five high performing and five low performing stack layout configurations respectively for 48,000 stack locations. Throughput time for the high stack layout configuration is 664 sec ($N_{smx} = 2$, $N_{smy} = 9$ and $N_r = 10$) while throughput time for the low stack layout configuration is 1286 sec ($N_{smx} = 2$, $N_{smy} = 5$ and $N_r = 9$).

Table 8: Good Terminal Layout Design Choices when the total number of storage locations is 28800 (container arrival rate: 126 containers/hr; 15 ALVs)

N_{smx}	N_{smy}	N_r	N_b	N_t	N_s	L_q	U_q	$\mathbb{E}[T_q]$ (sec)	L_v	U_v	$\mathbb{E}[T_v]$ (sec)	L_s	U_s	$\mathbb{E}[T_s]$ (sec)	$\mathbb{E}[CT_u]$ (sec)
2	9	10	18	5	32	4.9	70%	260	0.05	65%	280.4	0.05	6%	56.7	597.0
2	8	10	21	5	28	4.9	70%	260	0.04	65%	279.1	0.07	7%	59.4	598.5
2	9	9	20	5	32	4.9	70%	260	0.05	65%	281.6	0.06	6%	57.0	598.6
2	7	10	24	5	24	4.9	70%	260	0.04	64%	277.3	0.09	9%	62.5	599.7
4	5	10	18	5	32	4.9	70%	260	0.05	66%	283.3	0.05	6%	56.7	600.0

Table 9: Poor Terminal Layout Design Choices when the total number of storage locations is 28800 (container arrival rate: 126 containers/hr; 15 ALVs)

N_{smx}	N_{smy}	N_r	N_b	N_t	N_s	L_q	U_q	$\mathbb{E}[T_q] (sec)$	L_v	U_v	$\mathbb{E}[T_v] (sec)$	L_s	U_s	$\mathbb{E}[T_s] (sec)$	$\mathbb{E}[CT_u] (sec)$
4	4	10	40	3	24	4.9	70%	260	8.7	97%	666.8	0.1	9%	67.4	994.2
2	9	5	60	3	32	4.9	70%	260	11.9	98%	761.1	0.1	9%	85.9	1107.0
2	5	9	67	3	16	4.9	70%	260	17.2	99%	914.5	0.3	20%	99.1	1273.6
2	8	4	65	4	28	4.9	70%	260	26.3	99%	1174.6	0.2	12%	97.5	1532.1
6	3	8	30	5	24	4.9	70%	260	29.4	99%	1265.7	0.1	9%	66.4	1592.1

Table 10: Good Terminal Layout Design Choices when the total number of storage locations is 36000 (container arrival rate: 126 containers/hr; 15 ALVs)

N_{smx}	N_{smy}	N_r	N_b	N_t	N_s	L_q	U_q	$\mathbb{E}[T_q] (sec)$	L_v	U_v	$\mathbb{E}[T_v] (sec)$	L_s	U_s	$\mathbb{E}[T_s] (sec)$	$\mathbb{E}[CT_u] (sec)$
2	9	10	23	5	32	4.9	70%	260	0.09	70%	303.1	0.06	6%	60.9	624.0
2	8	10	26	5	28	4.9	70%	260	0.09	70%	301.6	0.08	8%	63.9	625.5
2	9	9	25	5	32	4.9	70%	260	0.10	70%	304.2	0.06	7%	61.6	625.8
2	7	10	30	5	24	4.9	70%	260	0.10	70%	304.2	0.10	10%	68.2	632.4
2	8	9	29	5	28	4.9	70%	260	0.11	71%	308.1	0.08	8%	65.8	633.9

Table 11: Poor Terminal Layout Design Choices when the total number of storage locations is 36000 (container arrival rate: 126 containers/hr; 15 ALVs)

N_{smx}	N_{smy}	N_r	N_b	N_t	N_s	L_q	U_q	$\mathbb{E}[T_q] (sec)$	L_v	U_v	$\mathbb{E}[T_v] (sec)$	L_s	U_s	$\mathbb{E}[T_s] (sec)$	$\mathbb{E}[CT_u] (sec)$
2	6	10	60	3	20	4.9	70%	260	6.1	96%	587.2	0.2	15%	89.8	937.1
2	7	6	63	4	24	4.9	70%	260	9.7	98%	694.8	0.2	13%	96.3	1051.1
4	5	10	38	3	32	4.9	70%	260	11.6	98%	750.3	0.1	7%	64.6	1074.9
2	6	7	65	4	20	4.9	70%	260	11.6	98%	751.4	0.2	16%	100.2	1111.5
2	8	4	65	5	28	4.9	70%	260	26.3	99%	1174.6	0.2	12%	103.2	1537.8

Table 12: Good Terminal Layout Design Choices when the total number of storage locations is 48000 (container arrival rate: 126 containers/hr; 15 ALVs)

N_{smx}	N_{smy}	N_r	N_b	N_t	N_s	L_q	U_q	$\mathbb{E}[T_q] (sec)$	L_v	U_v	$\mathbb{E}[T_v] (sec)$	L_s	U_s	$\mathbb{E}[T_s] (sec)$	$\mathbb{E}[CT_u] (sec)$
2	9	10	30	5	32	4.9	70%	260	0.24	77%	337.0	0.07	7%	67.5	664.4
2	8	10	35	5	28	4.9	70%	260	0.29	79%	345.2	0.10	9%	72.8	678.0
2	9	9	34	5	32	4.9	70%	260	0.32	79%	348.5	0.08	7%	70.5	679.0
2	7	10	40	5	24	4.9	70%	260	0.37	80%	354.6	0.13	11%	78.5	693.1
2	8	9	39	5	28	4.9	70%	260	0.41	81%	359.6	0.10	9%	76.1	695.7

Table 13: Poor Terminal Layout Design Choices when the total number of storage locations is 48000 (container arrival rate: 126 containers/hr; 15 ALVs)

N_{smx}	N_{smy}	N_r	N_b	N_t	N_s	L_q	U_q	$\mathbb{E}[T_q] (sec)$	L_v	U_v	$\mathbb{E}[T_v] (sec)$	L_s	U_s	$\mathbb{E}[T_s] (sec)$	$\mathbb{E}[CT_u] (sec)$
2	9	10	50	3	32	4.9	70%	260	7.5	97%	630.2	0.01	8%	77.1	967.3
4	4	10	40	5	24	4.9	70%	260	8.7	97%	666.8	0.13	11%	78.5	1005.3
4	5	10	38	4	32	4.9	70%	260	11.6	98%	750.3	0.08	7%	70.0	1080.3
2	9	5	60	5	32	4.9	70%	260	11.9	98%	761.1	0.14	10%	97.0	1118.1
2	5	9	67	5	16	4.9	70%	260	17.2	99%	914.5	0.37	22%	112.0	1286.5

5.2 Comparison between Parallel and Perpendicular Stack Layout

In this subsection, we compare parallel stack layout configurations to perpendicular stack layout configurations based on throughput times ($E[CT_u]$). The analytical model for the perpendicular stack layout is adopted from Roy and De Koster [2012]. We perform 12 experiments based on the design parameters discussed in the previous section. Since the stack blocks are perpendicular to quay, we use a wide range for varying the number of stack blocks: from 10 to 120. The other design settings remain the same. Table 14 lists five high-performing perpendicular stack layout configurations and Table 15 lists five low-performing perpendicular stack layout configurations based on throughput times ($E[CT_u]$) with a total of 28,800 stack locations and 15 ALVs. For the same number of storage locations and ALVs, Tables 8 and 9 list five high-performing and five low-performing parallel stack layout configuration respectively.

For the best parallel layout configuration, the throughput time is 597 sec (Table 8), while for the best perpendicular stack layout configuration, the throughput time is 624 sec (Table 14) i.e, a difference of 4%. Thus, the throughput time performance for the parallel stack layout is marginally better than the perpendicular stack layout. However, as evident from Table 16, this percentage difference go upto 12% when the number of storage locations is 48000 and the container arrival rate is 108/hr.

Our results are consistent with the finding obtained by Wiese et al. [2011b]. The straddle carrier cycle time, which is defined as the sum of the time needed for stacking operations and the round-trip travel time (from quayside to the stackside and back), is about 2.3% less in the case of parallel stack layout than perpendicular stack layout. However, we expect that by also including the landside operations, the throughput time in the case of parallel stack layout may increase due to additional congestion along the driving lanes.

Table 14: Best configurations for perpendicular layout of stack blocks with container arrival rate of 126 containers/hr and 15 ALVs

N_r	N_b	N_t	N_s	L_q	U_q	$\mathbb{E}[T_q]$ (sec)	L_v	U_v	$\mathbb{E}[T_v]$ (sec)	L_s	U_s	$\mathbb{E}[T_s]$ (sec)	$\mathbb{E}[CT_u]$ (sec)
10	29	5	20	2.5	59%	172.7	0.02	57%	246.0	2.0	25%	202.8	621.6
9	32	5	20	2.5	59%	172.7	0.01	55%	234.4	2.3	27%	220.9	628.1
6	32	5	30	2.5	59%	172.7	0.04	63%	269.5	1.4	18%	192.9	635.2
7	28	5	30	2.5	59%	172.7	0.08	67%	288.4	1.1	17%	174.1	635.2
8	24	5	30	2.5	59%	172.7	0.14	71%	308.1	0.9	15%	156.2	637.1

Table 15: Poor configurations for perpendicular layout of stack blocks with container arrival rate of 126 containers/hr and 15 ALVs

N_r	N_b	N_t	N_s	L_q	U_q	$\mathbb{E}[T_q]$ (sec)	L_v	U_v	$\mathbb{E}[T_v]$ (sec)	L_s	U_s	$\mathbb{E}[T_s]$ (sec)	$\mathbb{E}[CT_u]$ (sec)
10	58	5	10	2.5	59%	172.7	0.00	36%	152.3	44.9	81%	1514.5	1839.5
4	120	3	20	2.5	59%	172.7	0.00	41%	177.1	46.3	69%	1719.2	2069.1
9	64	5	10	2.5	59%	172.7	0.00	34%	147.4	78.8	87%	2502.2	2822.3
10	72	4	10	2.5	59%	172.7	0.00	36%	152.3	149.7	92%	4539.5	4864.6
8	72	5	10	2.5	59%	172.7	0.00	33%	142.5	282.8	96%	8352.1	8667.3

Table 16: Percentage expected throughput time difference obtained from optimal parallel vs optimal perpendicular stack layout

V	Locations	λ_a (per hour)	$E[CT_u^*]$ (Parallel)	$E[CT_u^*]$ (Perpendicular)	% Diff.
15	28800	126	597.0	621.6	4%
20	28800	126	595.7	621.1	4%
15	28800	108	545.9	590.1	8%
20	28800	108	545.5	590.0	8%
15	36000	126	624.0	664.7	7%
20	36000	126	621.4	664.7	7%
15	36000	108	571.9	630.2	10%
20	36000	108	571.0	630.1	10%
15	48000	126	664.4	715.5	8%
20	48000	126	657.7	707.3	8%
15	48000	108	609.4	681.8	12%
20	48000	108	609.4	679.6	12%

5.3 Performance Ranks

To rank the performance of both parallel and perpendicular stack layout we use the Tukey test (Hsu [1996]) with 95% confidence interval. The main idea of the Tukey's test is to compute the honestly significant difference between two means using a statistical distribution defined by Student and called the q distribution.

For parallel stack layout, we vary the number of stack blocks, the number of rows, the number of bays, the number of modules in the X and the Y-axis, and number of tiers to obtain 336 different configurations (for three levels of storage locations: 28800, 36000, and 48000). Likewise, for a perpendicular stack layout, we vary the number of stack blocks, the number of rows, the number of bays, and number of tiers to obtain 252 different configurations. For each configuration, we obtain the throughput time performance for 11 different container arrival rates and two levels of vehicles. In sum, we had throughput time measure for 16,632 ($252 \times 3 \times 11 \times 2$) perpendicular stack scenarios and 22,176 ($336 \times 3 \times 11 \times 2$) parallel stack scenarios. Then we perform all-pairwise comparison and obtain

homogeneous subsets of configurations using Tukey’s honest significance test. We denote a parallel and a perpendicular configuration using the notations Pl_Ns_Nr_Nb_Nt and Pr_Ns_Nr_Nb_Nt respectively.

We show the first three homogeneous subsets that ranks the configurations based on average throughput times for 28800, 36000, and 48000 storage locations (see Tables 17-19). For storage location of 28800, we see that the best performing subset (with 16 configurations) has 14 parallel stack layout configurations and 2 perpendicular layout configurations. The second subset has new perpendicular stack layout configurations whose mean performance vary significantly from the layout configurations present in the first group. Likewise, for 36000 and 48000 storage locations, the best subset has only 2-3 perpendicular stack layout configurations that are not significantly different from the other parallel stack layout configurations present in the same group.

Table 17: Top 3 stack configuration groups (for 28800 storage locations) based on Tukey’s range test

Configuration	Subset 1	Subset 2	Subset 3
Pl_28_10_21_5	570.3		
Pl_28_9_23_5	572.7	572.7	
Pl_28_8_26_5	580.9	580.9	580.9
Pl_20_10_29_5	583.6	583.6	583.6
Pl_28_10_26_4	591.1	591.1	591.1
Pl_20_9_32_5	593.5	593.5	593.5
Pl_28_7_30_5	594.6	594.6	594.6
Pl_28_9_29_4	599.0	599.0	599.0
Pr_20_10_29_5	605.0	605.0	605.0
Pl_32_10_18_5	605.7	605.7	605.7
Pl_20_8_36_5	609.2	609.2	609.2
Pr_20_9_32_5	610.7	610.7	610.7
Pl_28_8_33_4	612.8	612.8	612.8
Pl_28_6_35_5	614.1	614.1	614.1
Pl_20_10_36_4	614.9	614.9	614.9
Pl_24_10_24_5	616.4	616.4	616.4
Pr_30_7_28_5		620.1	620.1
Pr_30_6_32_5		620.1	620.1
Pr_30_8_24_5		621.2	621.2
Pr_20_8_36_5			623.8
Pl_28_7_37_4			627.0
Pr_20_10_36_4			629.6

Table 18: Top 3 stack configuration groups (for 36000 storage locations) based on Tukey’s range test

Configuration	Subset 1	Subset 2	Subset 3
Pl_28_10_26_5	596.5		
Pl_28_9_29_5	604.4	604.4	
Pl_28_8_33_5	618.2	618.2	618.2
Pl_20_10_36_5	620.6	620.6	620.6
Pl_28_10_33_4	628.4	628.4	628.4
Pl_28_7_37_5	632.5	632.5	632.5
Pl_28_9_36_4	636.9	636.9	636.9
Pl_20_9_40_5	637.3	637.3	637.3
Pr_20_10_36_5	647.6	647.6	647.6
Pr_30_8_30_5	648.0	648.0	648.0
Pr_30_7_35_5		653.0	653.0
Pr_30_9_27_5		653.6	653.6
Pl_28_8_41_4		658.1	658.1
Pl_28_6_43_5		659.4	659.4
Pl_20_8_45_5		659.4	659.4
Pr_30_6_40_5		659.7	659.7
Pr_30_10_24_5			660.4
Pr_20_9_40_5			662.4
Pl_20_10_45_4			665.5
Pr_30_9_34_4			671.9
Pr_30_8_38_4			672.0
Pr_40_5_36_5			672.3
Pr_40_6_30_5			673.2
Pr_30_10_30_4			673.3

6 Conclusions

This research is a first attempt to develop integrated models for the seaside operations of container terminals with a parallel stack layout by taking into account the stochastic interactions among the quayside, vehicle transport and stackside processes. With the help of extensive numerical experiments (22176 for parallel and 16632 for perpendicular), we are able to show that terminals with parallel stack layout are slightly better (4%-12%) than those with perpendicular stack layout as the best performing layout in the former requires less throughput time for completing one cycle of the seaside operation. Further, we see that even among terminals which have a parallel stack layout, those terminals that have a smaller number of stack modules along the X-axis and more stack modules along the Y-axis show shorter expected unload throughput times. Although we show that the parallel layout are better in practice, other aspects (such as decoupling of loads between

Table 19: Top 3 stack configuration groups (for 48000 storage locations) based on Tukey’s range test

Configuration	Subset 1	Subset 2	Subset 3
Pl_28_10_35_5	644.8		
Pl_28_9_39_5	660.1	660.1	
Pl_28_8_43_5	675.2	675.2	675.2
Pl_28_10_43_4	686.7	686.7	686.7
Pl_20_10_48_5	688.8	688.8	688.8
Pr_30_9_36_5	695.8	695.8	695.8
Pr_30_10_32_5	696.3	696.3	696.3
Pr_30_8_40_5	696.8	696.8	696.8
Pl_28_7_49_5	703.6	703.6	703.6
Pl_28_9_48_4		710.0	710.0
Pr_30_7_46_5		710.1	710.1
Pr_40_6_40_5		716.3	716.3
Pl_20_9_54_5		720.1	720.1
Pr_30_10_40_4		720.8	720.8
Pr_40_7_35_5			722.5
Pr_30_9_45_4			726.9
Pr_40_5_48_5			727.0
Pr_20_10_48_5			733.8
Pr_40_8_30_5			734.0
Pr_30_8_50_4			735.1

sea and landside, safety of the drivers and vehicle congestion) need to be considered while choosing the optimal stack block layout.

We believe that stochastic models of the container handling operations can help in better and faster design of container terminals and can also improve the container handling efficiency of existing terminals.

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A Vehicle Travel Time from Quayside to Stackside

We here consider the case when an ALV travels from quayside to stackside. In this situation, if permissible, the vehicle uses shortcut paths to reach the destination stack block. The selection of the shortcut path depends on the relative position of the index of the QC and the destination stack block. Note that several feasible travel paths exist to reach the destination stack block from the originating QC. We enumerate the possible route combination from quayside to stackside for the vehicle path topology, described in Figure 3. After estimating the sum of travel times for all cases, we determine the average travel time by dividing the sum of total travel time by the number of all possible travel routes from quayside to the stackside, which corresponds to a random storage strategy. Table 20 lists the terms that are used in this paper for denoting the various travel time expressions. In this table, we also include the number of possible feasible routes corresponding to all travel time scenarios for terminal layout shown in Figure 3.

Table 20: Table to show terminology used in this paper for time expression

Scenarios	Cases	Subcases	Terminology for time expressions	Number of possible routes (refer to Figure 3)
Scenario 1	Case I	NA	$T_{s_1c_1}^{qs}$	48
	Case II		$T_{s_1c_2}^{qs}$	144
Scenario 2	Case I	Subcase I	$T_{s_2c_{11}}^{qs}$	24
		Subcase II	$T_{s_2c_{12}}^{qs}$	72
	Case II	Subcase I	$T_{s_2c_{21}}^{qs}$	24
		Subcase II	$T_{s_2c_{22}}^{qs}$	72
Scenario 3	Case I	Subcase I	$T_{s_3c_{11}}^{qs}$	144
		Subcase II		
		<i>Condition 1</i>	$T_{s_3c_{12,1}}^{qs}$	6
		<i>Condition 2</i>	$T_{s_3c_{12,2}}^{qs}$	6
		<i>Condition 3</i>	$T_{s_3c_{12,3}}^{qs}$	36
	Case II	Subcase I	$T_{s_3c_{21}}^{qs}$	144
		Subcase II		
		<i>Condition 1</i>	$T_{s_3c_{22,1}}^{qs}$	6
		<i>Condition 2</i>	$T_{s_3c_{22,2}}^{qs}$	6
<i>Condition 3</i>		$T_{s_3c_{22,3}}^{qs}$	36	

Scenario 1: When the stack blocks lie completely to the left of the first shortcut path, SP_1 .

If $N_{srmx}[k]$ represents the number of stacks lying to the right of the shortcut path k . Then the index i varies as $\{1, \dots, (N_{srmx} - N_{srmx}[1] - 1)\}$. While the other indices vary as $l = \{1, \dots, N_{bs}\}$ and $k = \{1, \dots, N_{qc}\}$.

Case I: In this case, the stack blocks lie in the first stack module along the Y-axis (i.e.

$j = 1$).

For the layout shown in Figure 3, Equation 29 is applicable when ALVs move from any one of the QCs ($QC_1, QC_2, QC_3, QC_4, QC_5$ or QC_6) to the stack block SC_1 . The expression $\left(\frac{D_{ex}}{2} + W_{bl} + W_{bq}\frac{(N_{bq}-1)}{2}\right)$ represents the distance travelled by the ALVs in the transportation path along the quayside. The term W_l , denotes length of shortcut path from which ALVs move to stackside. The expression $(N_{lbs}[k]S + 2(X_e + D_{dl}) + (N_{smx} - N_{srmx}[k] - i)(W_{sb} + 2D_{dl} + D_d))$ denotes the distance to reach the destination stack block from end of shortcut path.

$$\begin{aligned}
T_{s_1c_1}^{qs} = & \sum_{i=1}^{N_{smx}-N_{srmx}[1]-1} \sum_{k=1}^{N_{qc}} \sum_{l=1}^{N_{bs}} \left(\frac{D_{ex}}{2} + W_{bl} + W_{bq}\frac{(N_{bq}-1)}{2} + W_l + N_{lbs}[k]S \right. \\
& + 2(X_e + D_{dl}) + (N_{smx} - N_{srmx}[k] - 1 - i)(W_{sb} + 2D_{dl} + D_d) + (N_{bs} - l)S \\
& \left. + \frac{D_t}{2} + \frac{S}{2} \right) \frac{1}{h_v} \tag{29}
\end{aligned}$$

To explain Equation 29, we consider the movement of an ALV from QC_4 to the l^{th} buffer of SC_1 in the layout shown in Figure 3. For this layout, N_{smx} is 4 and $N_{srmx}[4]$, the number of stack modules to the right of fourth shortcut path, SP_4 along X-axis is 1. We are considering SC_1 as destination stack block which corresponds to $i = 1$ and $j = 1$. Now, we can determine the value of term $(N_{smx} - N_{srmx}[k] - 1 - i)$ as 1 (see Equation 30). Container loaded ALV moves from the QC_4 to the shortcut path SP_4 after travelling $\left(\frac{D_{ex}}{2} + W_{bl} + W_{bq}\frac{(N_{bq}-1)}{2}\right)$ distance units. Now, ALV takes the shortcut path of length W_l units to reach the main guide path. The ALV again travels $(N_{lbs}[4]S + X_e + D_{dl})$ distance units to cross the stack block that is directly connected with the shortcut path SP_4 . Then, the ALV moves towards the left side of main guide path and travels $(W_{sb} + 2D_{dl} + D_d)$ distance units to reach the destination stack block SC_1 . Again, ALV travels $(X_e + D_{dl})$ distance units to reach the destination buffer lane of the stack block SC_1 . Finally, the ALV reaches the specific buffer lane after travelling $(N_{bs} - l)S$ distance units. Here, h_v denotes the ALV travel velocity.

$$\begin{aligned}
T_{s_1c_1}^{QC_4,SC_1} = & \left(\frac{D_{ex}}{2} + W_{bl} + W_{bq}\frac{(N_{bq}-1)}{2} + W_l + N_{lbs}[4]S + 2(X_e + D_{dl}) + 1(W_{sb} \right. \\
& \left. + 2D_{dl} + D_d) + (N_{bs} - l)S + \frac{D_t}{2} + \frac{S}{2} \right) \frac{1}{h_v} \tag{30}
\end{aligned}$$

Case II: In this case, the destination stack blocks lie in a stack module other than the first stack module along the Y-axis.

The index j varies from $j = \{2, \dots, N_{smy}\}$. The travel time expression for this case is given in Equation 31. For the given layout, Equation 31 is applicable when ALVs move from any one of the QC ($QC_1, QC_2, QC_3, QC_4, QC_5$ or QC_6) to the stack block (SC_2, SC_3, SC_4, SC_5 or SC_6).

$$\begin{aligned}
T_{s_1c_2}^{QC_4, SC_1} = & \sum_{i=1}^{N_{smx}-N_{srmx}[1]-1} \sum_{j=2}^{N_{smx}} \sum_{k=1}^{N_{qc}} \sum_{l=1}^{N_{bs}} \left(\frac{D_{ex}}{2} + W_{bl} + W_{bq} \frac{(N_{bq}-1)}{2} + W_l \right. \\
& + (N_{lbs}[k])S + 2(X_e + D_{dl}) + (N_{smx} - N_{srmx}[k] - i)(W_{sb} + 2D_{dl} + D_d) + \\
& \left. (j-1)(2D_t + 2W_{sr} + W_s) + (l-1)S + \frac{D_t}{2} + \frac{S}{2} \right) \frac{1}{h_v} \quad (31)
\end{aligned}$$

For instance, we consider the movement of an ALV from QC_4 to the l^{th} buffer of SC_5 as described in Figure 3 and derive the travel time expression using Equation 31. For the layout, N_{smx} is 4 and $N_{srmx}[4]$, the number of stack modules to the right of fourth shortcut path corresponding to origin QC taken along X-axis is 1. We are considering SC_5 which corresponds to $i = 1$ and $j = 3$. Now, the value of term $(N_{smx} - N_{srmx}[k] - 1 - i)$ is 1 (similar to the Case 1 as shown in Equation 32). The container loaded ALV moves from QC_4 to the shortcut path SP_4 after travelling $\left(\frac{D_{ex}}{2} + W_{bl} + W_{bq} \frac{(N_{bq}-1)}{2}\right)$ distance units. Now, ALV takes the shortcut path of length W_l units to reach the main guide path. The ALV again travels $(N_{lbs}[4])S + X_e + D_{dl}$ units to cross the stack block that is directly connected with shortcut path SP_4 . Further, ALV moves left side of main guide path and travels $2(W_{sb} + 2D_{dl} + D_d)$ distance units in X-axis and then $2(2D_t + 2W_{sr} + W_s)$ distance units in Y-axis to reach the destination stack block SC_5 . Again, the ALV travels $(X_e + D_{dl})$ distance units to reach the buffer lane assigned to the vehicle in stack block SC_1 . Finally, the ALV reaches the destination buffer lane after travelling $(l-1)S$ distance units .

$$\begin{aligned}
T_{s_1c_2}^{QC_4, SC_5} = & \left(\frac{D_{ex}}{2} + W_{bl} + W_{bq} \frac{(N_{bq}-1)}{2} + W_l + (N_{lbs}[4])S + 2(X_e + D_{dl}) + (W_{sb} \right. \\
& \left. + 2D_{dl} + D_d) + 2(2D_t + 2W_{sr} + W_s) + (l-1)S + \frac{D_t}{2} + \frac{S}{2} \right) \frac{1}{h_v} \quad (32)
\end{aligned}$$

Scenario 2: When the stack blocks lie completely to the right of the last shortcut path,

$SP_{N_{qc}}$.

In this case, the index i takes the value from the set $\{(N_{smx} - N_{rsmx}[N_{qc}] + 1), \dots, N_{smx}\}$. There exists several possible paths that a vehicle can take to reach the destination stack block. However, we consider only the shortest path for vehicle movement. An ALV can either follow the main guide path or can go via the shortcut path depending on the least travel distance.

Case I: In this case, the shortcut path is connected with the stack module taken along the X-axis, which also includes the last shortcut path i.e., $k \geq ky[N_{smx} - N_{rsmx}[N_{qc}]]$

Subcase I: In this subcase, the stack blocks lie in a stack module along the Y axis other than the first stack module (i.e. $j = \{2, \dots, N_{smy}\}$).

In this subcase, the ALV can either take a shortcut path to reach the destination stack block or the ALV can go via the main guide path, whichever is shorter. Equations 33 and 34 represent the distance travelled from the originating QC to the assigned stack block via the shortcut path and the main guided path respectively. To develop the travel time expression, we consider the minimum of the two travel distances, $D_{s_2c_{11}}^1$ and $D_{s_2c_{11}}^2$ (see Equation 35). For the layout shown in Figure 3, Equation 35 is applicable when ALVs move from the QC (QC_4 , QC_5 or QC_6) to the stack block (SC_{20} , SC_{21} , SC_{22} , SC_{23} or SC_{24}).

$$D_{s_2c_{11}}^1 = \sum_{i=(N_{smx}-N_{rsmx}[N_{qc}]+1)}^{N_{smx}} \sum_{j=2}^{N_{smy}} \sum_{k=ky[N_{smx}-N_{rsmx}[N_{qc}]]}^{N_{qc}} \sum_{l=1}^{N_{bs}} \left(\frac{D_{ex}}{2} + W_{bl} + W_{bq} \frac{(N_{bq} - 1)}{2} + W_l + N_{lbs}[k]S + 2(X_e + D_{dl}) + (j - 1)(2D_t + 2W_{sr} + W_s) + (i - (N_{smx} - N_{rsmx}[k]))(2D_{dl} + D_d + W_{sb}) + (l - 1)S + \frac{D_t}{2} + \frac{S}{2} \right) \quad (33)$$

$$D_{s_2c_{11}}^2 = \sum_{i=(N_{smx}-N_{rsmx}[N_{qc}]+1)}^{N_{smx}} \sum_{j=2}^{N_{smy}} \sum_{k=ky[N_{smx}-N_{rsmx}[N_{qc}]]}^{N_{qc}} \sum_{l=1}^{N_{bs}} \left(\frac{D_{ex}}{2} + W_{bl} + W_{bq} \frac{(N_{bq} - 1)}{2} + (N_{qc} - k)(D_{ex} + D_{in}) + L_r + W_l + L'_r + D_{dl} + X_e + (l - 1)S + (N_{smx} - i + 1)(2D_{dl} + W_{sb} + D_d) - D_d + (j - 1)(2D_t + 2W_{sr} + W_s) + \frac{D_t}{2} + \frac{S}{2} \right) \quad (34)$$

$$T_{s_2c_{11}}^{qs} = Min \left\{ D_{s_2c_{11}}^1, D_{s_2c_{11}}^2 \right\} \frac{1}{h_v} \quad (35)$$

For instance, we consider the movement of an ALV from QC_5 to the l^{th} buffer of SC_{22} (shown in Figure 3). For the given layout N_{smx} is 4, N_{qc} is 6 and $N_{srmx}[5]$, number of stack modules to the right of fifth shortcut path, SP_5 is 1. We are considering SC_{22} which corresponds to $i = 4$ and $j = 3$. For this case, the ALV takes the shortcut path or the main guide path to reach the destination stack block, whichever is shorter. Equation 36 evaluates the distance travelled by an ALV via the shortcut path. The container loaded ALV moves from the QC_5 to the shortcut path SP_5 after travelling $(\frac{D_{ex}}{2} + W_{bl} + W_{bq} \frac{(N_{bq}-1)}{2})$ distance units. Now, the ALV takes the shortcut path of length W_l distance units to reach the main guide path. The ALV again travels $(S + (X_e + D_{dl}))$ distance units, left to the shortcut path to reach the immediate driving lane. Further, the ALV travels $(2(2D_t + 2W_{sr} + W_s))$ distance units in the Y-axis to reach the third transfer lane that is connected with the stack block SC_{22} . Now, ALV moves along uni-directional transfer lane and reaches the l^{th} buffer of destination stack block after travelling $((2D_{dl} + D_d + W_{sb}) + (X_e + D_{dl}) + (l - 1)S + \frac{D_t}{2} + \frac{S}{2})$ distance units.

$$D_{s_2c_1}^1 = \left(\frac{D_{ex}}{2} + W_{bl} + W_{bq} \frac{(N_{bq}-1)}{2} + W_l + S + 2(X_e + D_{dl}) + 2(2D_t + 2W_{sr} + W_s) \right. \\ \left. + (2D_{dl} + D_d + W_{sb}) + (l - 1)S + \frac{D_t}{2} + \frac{S}{2} \right) \quad (36)$$

Equation 37 evaluates the time taken to reach SC_{22} from the originating QC_5 via the main guide path. The container loaded ALV moves from the QC_5 to reach the main guide path after travelling $(\frac{D_{ex}}{2} + W_{bl} + W_{bq} \frac{(N_{bq}-1)}{2} + (D_{ex} + D_{in}))$ distance units. Now the ALV follows the main guide path and travels $(L_r + W_l + L'_r + (2D_{dl} + W_{sb}))$ distance units to reach the driving lane that lies to the left of the destination stack module along the X-axis (for this particular instance, the driving lane lies left to the 4th stack module taken along X-axis). Now, the ALV moves along the Y-axis using the driving lane and reaches the transfer lane that connects the destination stack block SC_{22} after travelling $2(2D_t + 2W_{sr} + W_s)$ distance units. Finally, the ALV travels $((l - 1)S + \frac{D_t}{2} + \frac{S}{2})$ units to reach the l^{th} buffer of the destination block.

$$D_{s_2c_1}^2 = \left(\frac{D_{ex}}{2} + W_{bl} + W_{bq} \frac{(N_{bq}-1)}{2} + (D_{ex} + D_{in}) + L_r + W_l + L'_r + D_{dl} + X_e + \right. \\ \left. (2D_{dl} + W_{sb}) + 2(2D_t + 2W_{sr} + W_s) + (l - 1)S + \frac{D_t}{2} + \frac{S}{2} \right) \quad (37)$$

Now, Equation 38 considers minimum of $D_{s_2c_{1_1}}^1$ and $D_{s_2c_{1_1}}^2$ and estimates the minimum travel time to reach the destination block SC_{22} from originating QC_5 .

$$T_{s_2c_{1_1}}^{QC_5, SC_{22}} = Min \left\{ D_{s_2c_{1_1}}^1, D_{s_2c_{1_1}}^2 \right\} \frac{1}{h_v} \quad (38)$$

Subcase II: In this subcase, the stacks lie in the first stack module along the Y-axis ($j = 1$).

In this subcase, the ALV cannot go via any shortcut path due to the uni-directional path constraints. So, the ALV reaches the destination block only via the main guide path. The travel time expression for this case is given in Equation 39. For the layout shown in Figure 3, Equation 39 is applicable when an ALV moves from any one of the QCs (QC_4 , QC_5 or QC_6) to the stack block SC_{19} .

$$\begin{aligned} T_{s_2c_{1_2}}^{qs} = & \sum_{i=N_{smx}-N_{srmx}[N_{qc}]+1}^{N_{smx}} \sum_{k=ky[N_{smx}-N_{srmx}[N_{qc}]]}^{N_{qc}} \sum_{l=1}^{N_{bs}} \left(\frac{D_{ex}}{2} + W_{bl} + W_{bq} \frac{(N_{bq}-1)}{2} + \right. \\ & (N_{qc}-k)(D_{ex} + D_{in}) + L_r + W_l + L'_r + D_{dl} + X_e + (N_{lbs}-l)S + (N_{smx}-i) \\ & \left. (2D_{dl} + W_{sb} + D_d) + \frac{D_t}{2} + \frac{S}{2} \right) \frac{1}{h_v} \quad (39) \end{aligned}$$

For instance, we consider the movement of an ALV from QC_5 to the l^{th} buffer of the SC_{19} (shown in Figure 3). Here, N_{smx} is 4, N_{qc} is 6 and $N_{srmx}[5]$, the number of stack modules to the right of the fifth shortcut path corresponding to the originating QC taken along the X-axis, is 1. We are considering SC_{19} , which corresponds to $i = 4$ and $j = 1$.

Equation 40 evaluates the distance travelled by an ALV via the main guide path. The container loaded ALV moves from the QC_5 to the main guide path after travelling $(\frac{D_{ex}}{2} + W_{bl} + W_{bq} \frac{(N_{bq}-1)}{2} + (D_{ex} + D_{in}))$ distance units. Now, the ALV follows the main guide path and travels $(L_r + W_l + L'_r)$ distance units to reach the destination block. Finally, the ALV travels $(D_{dl} + X_e + (N_{lbs}-l)S + \frac{D_t}{2} + \frac{S}{2})$ distance units to reach the l^{th} buffer of destination stack block SC_{19} .

$$\begin{aligned} T_{s_2c_{1_2}}^{QC_5, SC_{19}} = & \left(\frac{D_{ex}}{2} + W_{bl} + W_{bq} \frac{(N_{bq}-1)}{2} + (D_{ex} + D_{in}) + L_r + W_l + L'_r + \right. \\ & \left. D_{dl} + X_e + (N_{lbs}-l)S + \frac{D_t}{2} + \frac{S}{2} \right) \frac{1}{h_v} \quad (40) \end{aligned}$$

Case II: The shortcut path is connected to the stack module taken along the X-axis, which also includes the the first shortcut path i.e., $k < ky[N_{smx} - N_{srmx}[N_{qc}]]$.

Subcase I: In this case, the stack blocks lie in a stack module along the Y-axis other than the first stack module i.e., $j = \{2, \dots, N_{sm_y}\}$.

The ALVs can either follow the main guide path, where the travel time is given in Equation 43 or use a different shortcut path. For example, in the layout shown in Figure 3, ALVs can either follow the main guide path or can go via one of two available shortcut routes to reach any one of the stack blocks (SC_{20} , SC_{21} , SC_{22} , SC_{23} or SC_{24}) from the QC (QC_1 , QC_2 or QC_3). (The shortcut routes SP_1 and SP_4 are the first shortcut paths connected to stack blocks SC_7 and SC_{13} respectively).

We use a variable (n) to denote the stack module taken along X-axis that are directly connected with the shortcut paths. In this paper, we consider a symmetric CT layout and assume that only two stack modules along X-axis (module including SC_7 and the module including SC_{13}) have a direct access to the shortcut paths. Therefore, n takes two values i.e., $n \in \{\frac{N_{sm_x}}{2}, \frac{N_{sm_x}}{2} + 1\}$. Since N_{sm_x} is 4 for the layout shown in Figure 3, n takes the values from $\{2, 3\}$.

We also use the term $ky[n]$ in deriving the travel time expressions. The term $ky[n]$ denotes the index of the first shortcut path connected to n^{th} stack module taken along X-axis. For the layout shown in Figure 3, if we consider $n = 2$ then the value of $ky[2]$ is 1, i.e., SP_1 is the first shortcut path that is connected with the second stack module taken along the X-axis. Similarly, for $n = 3$, the value of $ky[3]$ is 4 i.e., shortcut number four (SP_4) is the first shortcut that is connected with the third stack module taken along the X-axis. We use this term to switch the ALVs from main guide path to the driving lane that lies immediately to the left of the shortcut path. Further, we use another term $kx(i, l)$, which represents the index of the closest shortcut path to the l^{th} buffer of the stack block that lies in the i^{th} th stack module taken along the X-axis.

Equation 41 represents the distance travelled by an ALV to reach the destination stack block via two shortcut paths whereas Equation 42 finds the minimum of these two shortcut travel distances. Further, Equation 44 represents the minimum travel time of all possible cases taken by the ALV to reach the destination stack block. Finally, for the given layout, Equation 44 is applicable when ALVs move from any one of the QCs (QC_1 , QC_2 or QC_3) to the stack block (SC_{20} , SC_{21} , SC_{22} , SC_{23} or SC_{24}).

$$\begin{aligned}
D_{s_2c_{2_1}}^n = & \sum_{i=N_{smx}-N_{srmx}[N_{qc}]+1}^{N_{smx}} \sum_{j=2}^{N_{smy}} \sum_{k=ky[N_{smx}-N_{srmx}[N_{qc}]]-1}^{k=ky[N_{smx}-N_{srmx}[N_{qc}]]-1} \sum_{l=1}^{N_{bs}} \left(\frac{D_{ex}}{2} + W_{bl} + W_{bq} \right. \\
& \frac{(N_{bq} - 1)}{2} + W_l + abs(ky[n] - k)(D_{ex} + D_{in}) + N_{lbs}[ky[n]]S + 2(X_e + \\
& D_{dl}) + (j - 1)(2D_t + 2W_{sr} + W_s) + (i - n)(2D_{dl} + D_d + W_{sb}) + (l - 1)S + \\
& \left. + \frac{D_t}{2} + \frac{S}{2} \right) \tag{41}
\end{aligned}$$

$$D_{s_2c_{2_1}}(1) = Min \left\{ D_{s_2c_{2_1}}^2, D_{s_2c_{2_1}}^3 \right\} \tag{42}$$

$$\begin{aligned}
D_{s_2c_{2_1}}(2) = & \sum_{i=N_{smx}-N_{srmx}[N_{qc}]+1}^{N_{smx}} \sum_{j=2}^{N_{smy}} \sum_{k=ky[N_{smx}-N_{srmx}[N_{qc}]]-1}^{k=ky[N_{smx}-N_{srmx}[N_{qc}]]-1} \sum_{l=1}^{N_{bs}} \left(\frac{D_{ex}}{2} + W_{bl} + W_{bq} \right. \\
& \frac{(N_{bq} - 1)}{2} + (N_{qc} - k)(D_{ex} + D_{in}) + L_r + W_l + L'_r + D_{dl} + X_e + (l - \\
& 1)S + (N_{smx} - i + 1)(2D_{dl} + W_{sb} + D_d) - D_d + (j - 1)(2D_t + 2W_{sr} \\
& \left. + W_s) + \frac{D_t}{2} + \frac{S}{2} \right) \tag{43}
\end{aligned}$$

$$T_{s_2c_{2_1}}^{qs} = Min \left\{ D_{s_2c_{2_1}}(1), D_{s_2c_{2_1}}(2) \right\} \frac{1}{h_v} \tag{44}$$

For instance, we consider the movement of an ALV from QC_2 ($k = 2$) to the l^{th} buffer of SC_{24} . We consider stack block SC_{24} which corresponds to $i = 4$ and $j = 4$. As discussed earlier, there are three possible routes to reach the destination block SC_{24} from QC_2 . The two shortcut paths, SP_1 and SP_4 connects with stack blocks, SC_7 and SC_{13} respectively, whereas the third path uses the main guide path. Here, we use the same variable n (see Equation 41) to estimate the distance between two shortcut paths. The Equations 45 and 46 represent the distance travelled via an ALV corresponding to the shortcut paths, SP_1 and SP_4 respectively.

$$D_{s_2C_{21}}^2 = \left(\frac{D_{ex}}{2} + W_{bl} + W_{bq} \frac{(N_{bq} - 1)}{2} + W_l + (D_{ex} + D_{in}) + N_{lbs}[1]S + 2(X_e + D_{dl}) \right. \\ \left. + 3(2D_t + 2W_{sr} + W_s) + 2(2D_{dl} + D_d + W_{sb}) + (l - 1)S + \frac{D_t}{2} + \frac{S}{2} \right) \quad (45)$$

$$D_{s_2C_{21}}^3 = \left(\frac{D_{ex}}{2} + W_{bl} + W_{bq} \frac{(N_{bq} - 1)}{2} + W_l + 2(D_{ex} + D_{in}) + N_{lbs}[4]S + 2(X_e + D_{dl}) \right. \\ \left. + 3(2D_t + 2W_{sr} + W_s) + (2D_{dl} + D_d + W_{sb}) + (l - 1)S + \frac{D_t}{2} + \frac{S}{2} \right) \quad (46)$$

In Equation 47, we determine the minimum of two distance quantities, $D_{s_2C_{21}}^2$ and $D_{s_2C_{21}}^3$.

$$D_{s_2c_{21}}(1) = Min \left\{ D_{s_2C_{21}}^2, D_{s_2C_{21}}^3 \right\} \quad (47)$$

Now, there exists one more route leading to the destination stack block via the main guide path. The distance which is expressed in Equation 48.

$$D_{s_2c_{21}}(2) = \left(\frac{D_{ex}}{2} + W_{bl} + W_{bq} \frac{(N_{bq} - 1)}{2} + 4(D_{ex} + D_{in}) + L_r + W_l + L'_r + D_{dl} + \right. \\ \left. X_e + (l - 1)S + (2D_{dl} + W_{sb}) + (3)(2D_t + 2W_{sr} + W_s) + \frac{D_t}{2} + \frac{S}{2} \right) \quad (48)$$

After considering all possible routes for this particular instance, Equation 49 estimates minimum the required time to reach the destination block SC_{24} from the originating QC, QC_2 .

$$T_{s_2c_{21}}^{QC_2, SC_{24}} = Min \left\{ D_{s_2c_{21}}(1), D_{s_2c_{21}}(2) \right\} \frac{1}{h_v} \quad (49)$$

Subcase II: In this subcase, the stack blocks lie in the first stack module along the Y-axis ($j = 1$).

For this subcase, the ALVs can reach the destination stack blocks from the QCs only via the main guide path due to uni-directional path constraints. Equation 51 represents the travel time expression for the movement of an ALV from QC_2 to SC_{19} . For the given layout, Equation 51 is applicable when ALVs move from any one of the QCs (QC_1, QC_2

or QC_3) to the stack block (SC_{20} , SC_{21} , SC_{22} , SC_{23} or SC_{24}).

$$\begin{aligned}
T_{s_2c_2}^{qs} = & \sum_{i=N_{smx}-N_{srmx}[N_{qc}]+1}^{N_{smx}} \sum_{k=1}^{ky[N_{smx}-N_{srmx}[N_{qc}]]-1} \sum_{l=1}^{N_{bs}} \left(\frac{D_{ex}}{2} + W_{bl} + W_{bq} \frac{(N_{bq}-1)}{2} + (N_{bq} \right. \\
& -k)(D_{ex} + D_{in}) + L_r + W_l + L'_r + D_{dl} + X_e + (N_{bs} - l)S + (N_{smx} - i) \\
& \left. (2D_{dl} + W_{sb} + D_d) + \frac{D_t}{2} + \frac{S}{2} \right) \quad (50)
\end{aligned}$$

For instance, we consider the movement of an ALV from QC_2 ($k = 2$) to the l^{th} buffer of SC_{19} in the layout (shown in Figure 3). Here, N_{smx} is 4, N_{qc} is 6 and $N_{srmx}[5]$, the number of stack modules to the right of the fifth shortcut path SP_5 , is 1. We consider SC_{19} , which correspond to $i = 4$ and $j = 1$.

Equation 40 evaluates the distance travelled by an ALV via the main guide path. Container loaded ALV moves from the QC_2 to the main guide path after travelling $(\frac{D_{ex}}{2} + W_{bl} + W_{bq} \frac{(N_{bq}-1)}{2} + 4(D_{ex} + D_{in}))$ distance units. Now the ALV follows the main guide path and travels $(L_r + W_l + L'_r)$ distance units to reach the destination block. Finally, the ALV travels $(D_{dl} + X_e + (N_{bs} - l)S + \frac{D_t}{2} + \frac{S}{2})$ distance units to reach the l^{th} buffer of the destination stack block SC_{19} .

$$\begin{aligned}
T_{s_2c_2}^{QC_2, SC_{19}} = & \left(\frac{D_{ex}}{2} + W_{bl} + W_{bq} \frac{(N_{bq}-1)}{2} + 4(D_{ex} + D_{in}) + L_r + W_l + L'_r + D_{dl} + X_e \right. \\
& \left. + (N_{bs} - l)S + \frac{D_t}{2} + \frac{S}{2} \right) \quad (51)
\end{aligned}$$

Scenario 3: In this scenario, the destination stack blocks lie between the first shortcut and the last shortcut path.

Case I: The destination stack block lies on the same stack module taken along X-axis that also includes the first shortcut path i.e., $i = N_{smx} - N_{srmx}[N_{srmx}[1]]$

Subcase I: The stack blocks lie in a stack module along the Y-axis (other than the first Y stack module i.e., $j = \{2, \dots, N_{smy}\}$).

For the layout, Equation 52 is applicable when ALVs move from any one of the QCs (QC_1 , QC_2 , QC_3 , QC_4 , QC_5 or QC_6) to the stack block (SC_8 , SC_9 , SC_{10} , SC_{11} or SC_{12}). In this case, all ALVs are routed through the driving lane that lies to the left of the SC_7 .

$$\begin{aligned}
T_{s_3c_{1_1}}^{qs} &= \sum_{j=2}^{N_{smy}} \sum_{k=1}^{N_{qc}} \sum_{l=1}^{N_{bs}} \left(\frac{D_{ex}}{2} + W_{bl} + W_{bq} \frac{(N_{bq} - 1)}{2} + W_l + N_{lbs}[k]S + 2(X_e + D_{dl}) \right. \\
&\quad \left. + 2(X_e + D_{dl}) + (N_{smx} - N_{srmx}[k] - i)(W_{sb} + 2D_{dl} + D_d) + (j - 1) \right. \\
&\quad \left. (2D_t + 2W_{sr} + W_s) + (l - 1)S + \frac{D_t}{2} + \frac{S}{2} \right) \frac{1}{h_v} \tag{52}
\end{aligned}$$

Subcase II: In this subcase, the stack blocks lie in the first stack module along the Y-axis ($j = 1$).

In this subcase, time expressions differ depending on the location of the buffer lane relative to the shortcut path. For a given layout as shown in Figure 3, Equations 53 to 55 are applicable when ALVs move from the QC ($QC_1, QC_2, QC_3, QC_4, QC_5$ or QC_6) to the stack block SC_7 depending on the relative position of the buffer lanes and the shortcut path.

Condition 1: The shortcut path k is connected with the stack module along the X-axis (which is also connected with the first shortcut path) and the buffer lane at the destination stack block lies right to the shortcut path k .

$$\begin{aligned}
T_{s_3c_{1_2,1}}^{qs} &= \sum_{k=1}^{ky[N_{smx} - N_{srmx}[N_{qc}]] - 1} \sum_{l=N_{lbs}(k)}^{N_{bs}} \left(\frac{D_{ex}}{2} + W_{bl} + W_{bq} \frac{(N_{bq} - 1)}{2} + W_l + (kx(i, l) - k) \right. \\
&\quad \left. (D_{ex} + D_{in}) + N_{lbs}[kx(i, l) - l]S + \frac{D_t}{2} + \frac{S}{2} \right) \frac{1}{h_v} \tag{53}
\end{aligned}$$

Condition 2: The shortcut path k is connected with the stack module along the X-axis (which is also connected with the first shortcut path) and the buffer lane at the destination stack block lies left to the shortcut path k .

$$\begin{aligned}
T_{s_3c_{1_2,2}}^{qs} &= \sum_{k=1}^{ky[N_{smx} - N_{srmx}[N_{qc}]] - 1} \sum_{l=1}^{N_{lbs}(k)} \left(\frac{D_{ex}}{2} + W_{bl} + W_{bq} \frac{(N_{bq} - 1)}{2} + W_l + (N_{lbs}[k] - l)S \right. \\
&\quad \left. + \frac{D_t}{2} + \frac{S}{2} \right) \frac{1}{h_v} \tag{54}
\end{aligned}$$

Condition 3: The shortcut path k is connected with the stack module along the X-axis (which is also connected with the last shortcut path) and the buffer lane at the destination

stack block lies left to the shortcut path k .

$$\begin{aligned}
T_{s_3c_{12,3}}^{qs} &= \sum_{k=ky[N_{smx}-N_{srmx}[N_{qc}]]}^{N_{qc}} \sum_{l=1}^{N_{bs}} \left(\frac{D_{ex}}{2} + W_{bl} + W_{bq} \frac{(N_{bq}-1)}{2} + W_l + N_{lbs}[k]S + 2X_e \right. \\
&\quad \left. + 2D_{dl} + (N_{bs}-l)S + \frac{D_t}{2} + \frac{S}{2} \right) \frac{1}{h_v} \tag{55}
\end{aligned}$$

Case II: The destination stack block lies in the same stack module taken along X-axis that is connected with the last shortcut path i.e. $i = N_{smx} - N_{srmx}[N_{qc}]$.

Subcase I: The stack blocks lie in a stack module along the Y-axis (other than the first module i.e., $j = \{2, \dots, N_{smy}\}$).

Similar to the Case II in Scenario 2, there exists multiple routes to reach the destination stack blocks from all QCs. The ALVs can either follow the main guide path (where the travel time is expressed by Equation 58) or use one of the multiple shortcut paths. For example, ALVs can either follow the main guide path or can go via one of two available shortcut routes to reach the stack block from the originating QC in the layout shown in Figure 3. SP_1 and SP_4 are the first shortcut paths connected with the stack blocks, SP_7 and SP_{13} respectively. As described earlier, we consider a variable n that represents the number of stack blocks in the first stack module (along the Y-axis) directly connected with the shortcut path.

Equation 56 represents the distance travelled by ALVs to reach the destination stack block via all possible shortcut paths and Equation 57 finds the minimum of all distances along the possible shortcut paths. Further, Equation 59 represents the minimum travel time along all possible shortcut paths taken by an ALV to reach the destination stack block. Finally, for the given shown in Figure 3, Equation 59 is applicable when ALVs move from any one of the QCs ($QC_1, QC_2, QC_3, QC_4, QC_5$ or QC_6) to stack block ($SC_{14}, SC_{15}, SC_{16}, SC_{17}$ or SC_{18}).

$$\begin{aligned}
D_{s_3c_{21}}^n &= \sum_{j=2}^{N_{smy}} \sum_{k=ky[N_{smx}-N_{srmx}[N_{qc}]]}^{N_{qc}} \sum_{l=1}^{N_{bs}} \left(\frac{D_{ex}}{2} + W_{bl} + W_{bq} \frac{(N_{bq}-1)}{2} + W_l + abs(ky[n] \right. \\
&\quad \left. -k)(D_{ex} + D_{in}) + N_{lbs}[ky[n]]S + 2(X_e + D_{dl}) + (j-1)(2D_t + 2W_{sr} + W_s) \right. \\
&\quad \left. + (i-n)(2D_1 + D_d + W_{sb}) + (l-1)S + \frac{D_t}{2} + \frac{S}{2} \right) \tag{56}
\end{aligned}$$

$$D_{s_3c_2_1}(1) = \text{Min} \left\{ D_{s_2c_2_1}^1, D_{s_2c_2_1}^2 \right\} \quad (57)$$

$$\begin{aligned} D_{s_3c_2_1}(2) = & \sum_{j=2}^{N_{smx}} \sum_{k=ky[N_{smx}-N_{srmx}[N_{qc}]]}^{N_{qc}} \sum_{l=1}^{N_{bs}} \left(\frac{D_{ex}}{2} + W_{bl} + W_{bq} \frac{(N_{bq}-1)}{2} + (N_{qc}-k) \right. \\ & (D_{ex} + D_{in}) + L_r + W_l + L'_r + D_{dl} + X_e + (l-1)S + (N_{smx}-i+1) \\ & \left. (2D_{dl} + W_{sb} + D_d) - D_d + (j-1)(2D_t + 2W_{sr} + W_s) + \frac{D_t}{2} + \frac{S}{2} \right) \quad (58) \end{aligned}$$

$$T_{s_3c_2_1}^{qs} = \text{Min} \left\{ D_{s_2c_2_1}(1), D_{s_2c_2_1}(2) \right\} \frac{1}{h_v} \quad (59)$$

Subcase II: In this subcase, the stack blocks lie in the first stack module along the Y-axis ($j = 1$).

This subcase has a different travel time expression depending on the location of the buffer lane relative to the shortcut path. For the given layout, Equation 58 is applicable when ALVs move from any one of QCs ($QC_1, QC_2, QC_3, QC_4, QC_5$ or QC_6) to the stack block SC_{13} depending on the relative position of the buffer lanes and the shortcut path.

Condition 1: The buffer lane lies to the right of the last shortcut path.

$$\begin{aligned} T_{s_3c_2_2,1}^{qs} = & \sum_{k=1}^{N_{qc}} \sum_{l=N_{lbs}[N_{qc}]}^{N_{bs}} \left(\frac{D_{ex}}{2} + W_{bl} + W_{bq} \frac{(N_{bq}-1)}{2} + W_l + (N_{qc}-k)(D_{ex} + D_{in}) \right. \\ & + L_r + W_l + D_{dl} + X_e + (N_{bs}-1)S + (N_{smx}-i)(2D_{dl} + W_{sb} + D_d) \\ & \left. + \frac{D_t}{2} + \frac{S}{2} \right) \frac{1}{h_v} \quad (60) \end{aligned}$$

Condition 2: The buffers lane lies left to the originating shortcut path.

$$\begin{aligned} T_{s_3c_2_2,2}^{qs} = & \sum_{k=kx[N_{smx}-N_{srmx}[N_{qc}]]}^{N_{qc}} \sum_{l=1}^{N_{lbs}[k]} \left(\frac{D_{ex}}{2} + W_{bl} + W_{bq} \frac{(N_{bq}-1)}{2} + W_l + (N_{lbs}[k]-l)S \right. \\ & \left. + \frac{D_t}{2} + \frac{S}{2} \right) \frac{1}{h_v} \quad (61) \end{aligned}$$

Condition 3: The buffer lanes lies right to the originating shortcut path but left to the

last shortcut path.

$$T_{s_3c_{2,3}}^{qs} = \sum_{k=1}^{N_{qc}} \sum_{l=1}^{N_{bs}} \left(\frac{D_{ex}}{2} + W_{bl} + W_{bq} \frac{(N_{bq} - 1)}{2} + W_l + (kx(i, l) - k)(D_{ex} + D_{in}) + (N_{lbs}[kx(i, l)] - l + 1)S + \frac{D_t}{2} + \frac{S}{2} \right) \frac{1}{h_v} \quad (62)$$

To obtain T^{qs} , we need to take the average of travel time over possible routes from the QCs to all stack buffers positions (Equation 63).

$$T^{qs} = \frac{1}{(N_{smx} \times N_{smy} \times N_{bs} \times N_{qc})} \left(T_{s_1c_1}^{qs} + T_{s_1c_2}^{qs} + T_{s_2c_{1_1}}^{qs} + T_{s_2c_{1_2}}^{qs} + T_{s_2c_{2_1}}^{qs} + T_{s_2c_{2_2}}^{qs} + T_{s_3c_{1_1}}^{qs} + T_{s_3c_{1_2,1}}^{qs} + T_{s_3c_{1_2,2}}^{qs} + T_{s_3c_{1_2,3}}^{qs} + T_{s_3c_{2_1}}^{qs} + T_{s_3c_{2_2,1}}^{qs} + T_{s_3c_{2_2,2}}^{qs} + T_{s_3c_{2_2,3}}^{qs} \right) \quad (63)$$

B Flow chart for unloading process

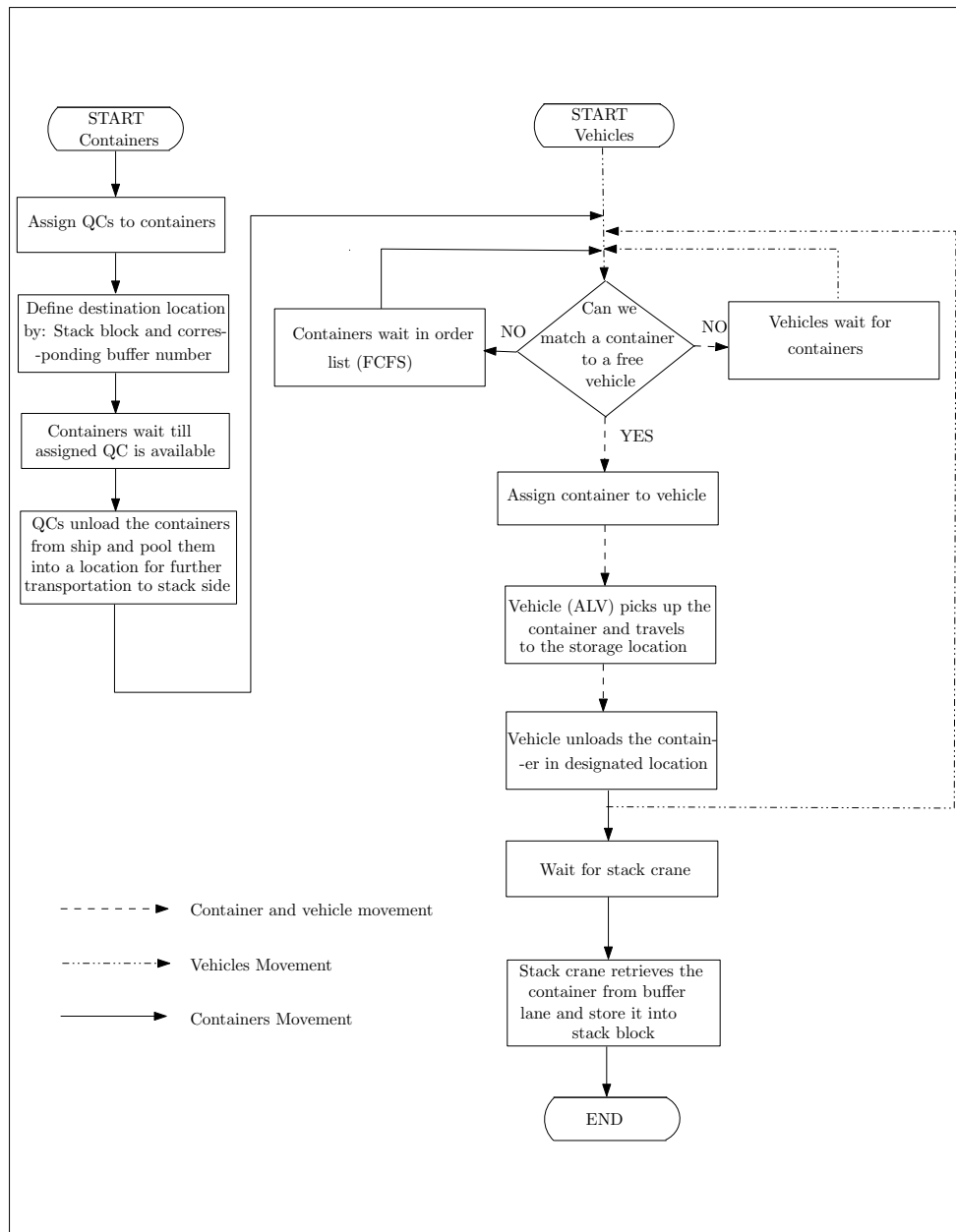


Figure 6: Flowchart of container flow in unloading process at a CT

OR Spectrum

Optimal Stack Layout in a Sea Container Terminal with Automated Lifting Vehicles

--Manuscript Draft--

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Abstract:	<p>Container terminal performance is largely determined by its design decisions, which include the number and type of quay cranes (QCs), stack cranes (SCs), transport vehicles, vehicle travel path, and stack layout. The terminal design process is complex because it is affected by factors such as topological constraints, stochastic interactions among the quayside, vehicle transport and stackside operations. Further, the orientation of the stack layout (parallel or perpendicular to the quayside) plays an important role in the throughput time performance of the terminals. Previous studies in this area typically use deterministic optimization or probabilistic travel time models to analyze the effect of stack layout on terminal throughput times, and ignore the stochastic interactions among the resources. It is unclear if stochastic interactions have an impact on the optimal stack layout. In this research, we capture the stochasticity with an integrated queuing network modeling approach to analyze the performance of container terminals with parallel stack layout using automated lifting vehicles (ALVs). Using this model, we investigate 1008 parallel stack layout configurations in terms of throughput times and determine the optimal stack layout configuration. We also find that, assuming an identical width of the internal transport area, container terminals with parallel stack layout perform better (from 4% - 12% in terms of container throughput times) than terminals with a perpendicular stack layout.</p>

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