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Authors

Mangold, C
Neogi, S
Donadio, D

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Optimal thickness of silicon membranes to achieve maximum thermoelectric efficiency: a first principles study

Claudia Mangold,[1] Sanghamitra Neogi,[2,1] and Davide Donadio[3,1,*]

[1] *Max Planck Institut für Polymerforschung, Ackermannweg 10, D-55128 Mainz, Germany*
[2] *Department of Aerospace Engineering Sciences, University of Colorado Boulder, Boulder, Colorado 80309, USA*
[3] *Department of Chemistry, University of California Davis, One Shields Ave., Davis, CA, 95616*

Silicon nanostructures with reduced dimensionality, such as nanowires, membranes and thin films, are promising thermoelectric materials, as they exhibit considerably reduced thermal conductivity. Here we utilize density functional theory and Boltzmann transport equation to compute the electronic properties of ultra-thin crystalline silicon membranes with thickness between 1 and 12 nm. We predict that an optimal thickness of $\sim$ 7 nm maximizes the thermoelectric figure of merit of membranes with native oxide surface layers. Further thinning of the membranes, although attainable in experiments, reduces the electrical conductivity and worsens the thermoelectric efficiency.

Small and flexible thermoelectric (TE) devices that do not involve moving components are increasingly favored for applications in microelectronics, sensing, nanometrology and low-power energy scavenging. Currently the best TE materials for room temperature applications are heavy metal chalcogenides, e.g. Bi_2Te_3 and PbTe [1, 2], and it is desirable to replace them with less expensive, non toxic alternatives. To achieve a high figure of merit, $ZT = TS^2\sigma/(\kappa_e + \kappa_{ph})$, a material should have a high electronic power factor $S^2\sigma$ (S is the Seeback coefficient and σ the electronic conductivity),and a low thermal conductivity (κ), to which both electrons (κ_e) and phonons (κ_{ph}) contribute. Silicon is Earth-abundant and environmentally friendly, easy to integrate in nowadays technology, but in its bulk form it has a very low ZT (0.01 at T =300 K), especially due to its high thermal conductivity.

Dimensionality reduction to nanowires [3, 4] and nanostructuring, as e.g. in nanomeshes [5], SiGe superlattices [6] and nano-grained SiGe [7], has shown potential to achieve technologically viable TE performances in silicon at room temperature, thanks to a large reduction of κ_{ph}. However, there is a trade-off between phononic and electronic transport coefficients: in fact, the presence of pores, grain boundaries and alloying negatively affects structural stability and charge transport, leading to a reduction of σ. Conversely, dimensionality reduction may enhance Seebeck coefficient and electron mobility, due to quantum confinement [8–12].

Crystalline silicon thin films (silicon on insulator, SOI) [13, 14] and suspended membranes [15] exhibit reduced thermal conductivity, up to 40 times lower than the bulk at room temperature [16–18], thus potentially enabling their use for TE applications. While the phononic properties of these systems have been investigated in detail [17–21], their electronic transport coefficients still need to be characterized. It is necessary to unravel the interplay among the charge transport properties of silicon membranes as a function of thickness and doping, assessing the optimal criteria, for which ZT is maximized.

Here we consider suspended ultra-thin silicon membranes with thickness up to 12 nm, for which very low κ was measured [17, 18], and we compute their electronic transport coefficients, σ, κ_e and S by first principles, using Boltzmann transport equation (BTE) and density functional theory (DFT). σ, κ_e and S are combined with the values of κ_{ph} formerly obtained by classical molecular dynamics (MD) [18], to get ZT as a function of carrier concentrations. We find that, due to a trade-off among the transport coefficients, ZT peaks at 0.2 at room temperature for an optimal membrane thickness of about 7 nm, which is within the range of feasibility of fabrication techniques [15]. Our calculations suggest that the presence of surface oxide layers, which leads to a drastic reduction of κ [18], does not hamper the electronic power factor significantly.

To address the relation between membrane thickness and charge transport we compute S, σ, κ_e and ZT of crystalline Si membranes exposing the hydrogen passivated [001] surface with (2×1) reconstruction [22] (Fig. 1a). We consider five models of Si membranes 0.8, 1.1, 3.3, 5.4 and 10.9 nm thick. When exposed to air under normal conditions silicon membranes form a $\sim$ 1 nm thick layer of native oxide at the surfaces,[23]. To comply with the size limitations imposed by DFT calculations, we model

* ddonadio@ucdavis.edu

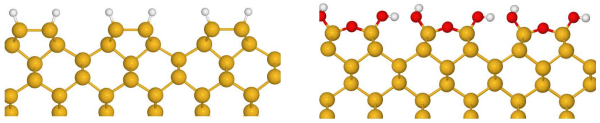

FIG. 1. Side view of the surface of hydrogen-passivated (left) and oxidized (right) Si membranes

the presence of native oxide by saturating the dangling bonds of an as-cleaved [001] surface with bridging oxygen atoms and hydroxyl groups, as shown in Figure 1(b). These simplified models do not have dangling bonds or other defects that produce states in the middle of the band gap, and reproduce the electronic properties of realistic silicon membranes, especially in the proximity of the Fermi level [24]. We consider three models of surface oxidized membranes with thickness of 3.9, 6.4 and 11.9 nm.

Electronic structure calculation are performed by DFT, using the generalized gradient approximation (GGA) functional by Perdew, Burke and Ernzerhof (PBE) [25], as implemented in the plane-waves code QUANTUM ESPRESSO [26]. Charge transport coefficients, S, σ and κ_e, are evaluated within the framework of semi-classical BTE [27] as implemented in BoltzTraP [28]. Computational details are provided in the supporting information (SI). The Fermi integrals that determine the transport coefficients (Eq. S1) depend on the relaxation time $\tau(\mathbf{k})$, which is computationally expensive to compute by first principles for systems so large as the ones considered here. We adopt the relaxation time approximation (RTA), assuming that the electron relaxation time τ is independent on ϵ and $\mathbf{k}$ and depends only on the concentration of carriers. In RTA S is independent of τ. The relaxation time remains as a prefactor to σ and κ_e. Since confinement and reduced dimensionality were predicted to enhance mobilities, at least for specific channels and surface orientations [8, 12, 29], we consider two sets of relaxation times: namely, τ fitted on the electron (hole) mobility of bulk Silicon [30, 31], and to four times enhanced mobilities, as computed for silicon nanowires [9].

Electronic transport coefficients combine with the lattice thermal conductivity, $\kappa_{\rm ph}$, to compute the thermoelectric figure of merit, ZT. $\kappa_{\rm ph}$ for membranes both with (2×1) reconstructed surfaces and with native oxide surface layers were computed by equilibrium MD simulations, and are in excellent agreement with Raman thermometry measure-

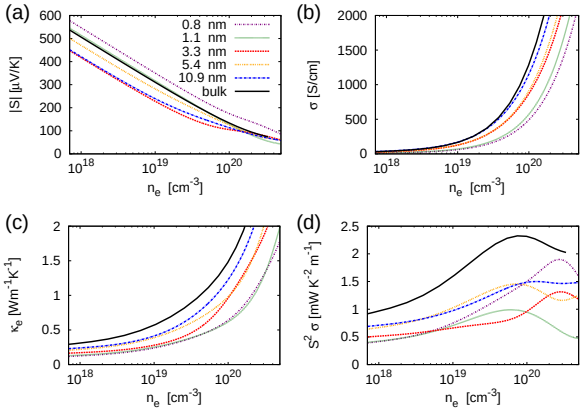

FIG. 2. (a) Seebeck coefficient, (b) electronic conductivity, (c) electronic contribution to the thermal conductivity, and (d) power factor, as a function of the carrier density, n_e, of hydrogen passivated Si membranes with thickness 0.8, 1.1, 3.3, 5.4 and 10.9 nm, compared to bulk Si at 300 K.

ments [18, 21]. The MD values of $\kappa_{\rm ph}$ reported in Table S1 in SI, are rescaled by the ratio between experimental $\kappa_{\rm ph}$ (160 Wm^{-1}K^{-1}) [32] and the one obtained by MD ($\kappa_{\rm ph} \sim 200$ Wm^{-1}K^{-1}[33]). $\kappa_{\rm ph}$ are in the range between 60 and 96 Wm^{-1}K^{-1}for hydrogen passivated membranes, and between 4 and 19 Wm^{-1}K^{-1}for surface oxidized ones.

Figure 2 shows the transport coefficients S, σ, κ_e, and the power factor, $S^2\sigma$ of five hydrogen passivated membranes with different thickness, as a function of the carrier concentration, n_e, compared to the corresponding values for bulk silicon. Here we report only the case of n-doping, as p-doping gives

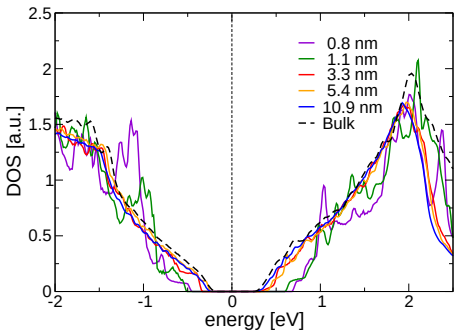

FIG. 3. Electronic density of states near the Fermi level of bulk silicon and crystalline membranes with thickness 0.8, 1.1, 3.3, 5.4 and 10.9 nm. The curves are aligned to the intrinsic Fermi level, and are rescaled by the number of electrons in the supercell to facilitate comparison.

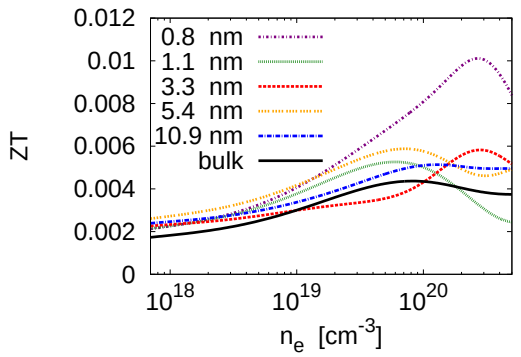

FIG. 4. Thermoelectric figure of merit, ZT, of n-type doped Si membranes with thickness 0.8, 1.1, 3.3, 5.4 and 10.9 nm, and of bulk silicon at 300 K.

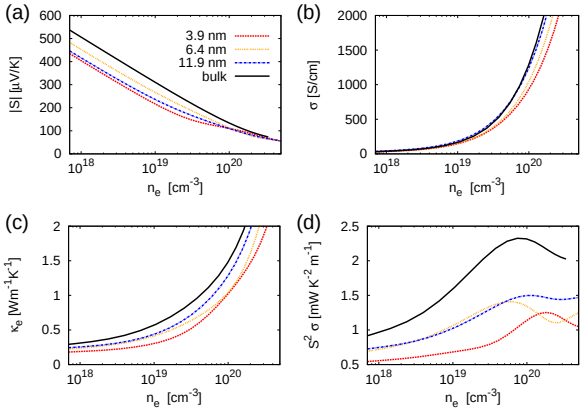

FIG. 5. (a) Seebeck coefficient, (b) electronic conductivity, (c) electronic contribution to the thermal conductivity, and (d) power factor, as a function of the carrier density, n_e, of oxidized Si membranes with thickness 3.9, 6.4 and 11.9 nm, compared to bulk Si at 300 K.

similar results. Confinement produces an enhancement of S (Fig. 2a) in the thinnest 0.8 and 1.1 nm thick membranes. The thicker membranes have slightly lower $|S|$ than bulk silicon. This behavior stems from the details of the band structures (Figures S1, S2) and the electronic density of states (DOS) (Fig. 3): 0.8 and 1.1 nm-thick membranes exhibit much larger energy gap and sharp peaks due to confinement[8], whereas the DOS of 3.3 nm and thicker membranes display slightly increased energy gaps but similar features as bulk silicon. The energy gap computed from Kohn-Sham states is systematically underestimated [34], but it does not affect directly the calculation of transport coefficients as a function of carrier density.

σ is systematically reduced by thinning the membranes (Fig. 2b), because of the increasing importance of surface scattering and of the reduced density of available electronic states in the conduction band. A similar effect occurs for κ_e (Fig. 2c), which is also reduced in membranes, and decreases as a function of thickness. The combination of S and σ yields a power factor that never exceeds the one of bulk silicon (Fig. 2d), and approaches it only for the thinnest membrane at very high carrier concentration. The peak power factor of the 10.9 nm membrane is about 2/3 of the bulk one. Using $\kappa_{\rm ph}$ from Table S1, we have computed ZT at 300 K (Figure 4). Since $\kappa_{\rm ph}$ is only mildly reduced in crystalline membranes with H-passivated reconstructed surfaces, ZT is of the same order of magnitude as that of bulk Si, which peaks at ~ 0.004. Nevertheless, all the membranes exhibit higher ZT than bulk Si, with a peak at 0.01 for the strongly confined 0.8 nm one.

These results suggest that the power factor of membranes is neither improved, nor seriously hampered by reducing their thickness to the nanoscale. In turn, they highlight the necessity of reducing $\kappa_{\rm ph}$ by more than one order of magnitude, to achieve viable TE efficiency. Native oxide surface layers lead to such reduction of $\kappa_{\rm ph}$ [18]. Hence we probe whether surface oxidation alters charge transport in silicon membranes. S, σ, κ_e and the power factor of oxidized silicon membranes, 3.9, 6.4 and 11.9 nm thick, are shown in Figure 5. We observe no substantial difference between the transport coefficients of H-passivated and of oxidized membranes, which exhibit the same trends with respect to thickness and carriers concentration. We note that κ_e grows beyond 1 $\rm Wm^{-1}K^{-1}$ for $n_e \geq 10^{20}$ $\rm cm^{-3}$, and becomes comparable to $\kappa_{\rm ph}$, thus contributing to limit ZT at high doping. The peak power factor (Fig. 5) is higher for thicker membranes, but it is reduced to 1.5 $\rm mWK^{-2}m^{-1}$ with respect to 2.3 $\rm mWK^{-2}m^{-1}$ computed for bulk silicon. Enhanced mobility due to confinement enhances $S^2\sigma$, whereas surface roughness, which is not considered in our calculations, may hamper charge carrier mobilities [24, 35] and smoothen the features of the DOS that enhance S in confinement [36], thus counteracting the positive effects on $\kappa_{\rm ph}$.

In the conservative hypothesis that electron lifetimes are the same as in bulk, the largely reduced $\kappa_{\rm ph}$ yields ZT up to ~ 0.07, while in the best case scenario in which τ is enhanced by confinement, we predict a ZT as high as 0.2 (Figure 6), 50 times larger than the reference bulk value of 0.004 (Fig-

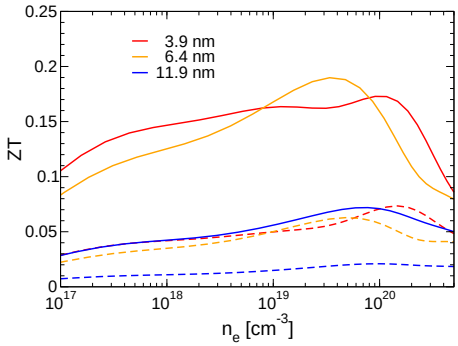

FIG. 6. Thermoelectric figure of merit, ZT, of 3.9, 6.4 and 11.9 nm thick Si membranes with oxidized surfaces at 300 K as a function of carrier concentration n_e. ZT is computed using relaxation times fitted from bulk silicon mobilities (dashed lines) and assuming enhanced mobility due to confinement (solid lines).

ure 4). Remarkably, the highest ZT is achieved for 6.4 nm thick membranes, while reducing thickness further does not lead to improvements in the thermoelectric performance. The 11.9 nm thick membrane approaches $ZT \sim 0.1$, which makes this system viable for applications in the microwatt power range, such as autonomous sensors. For example, each leg of a TE device made of 11.9 nm thick, 5 μm wide, 1 μm long membranes, with a temperature difference of 10 K between its hot and cold side yields a power output up to 0.1 μW at maximum efficiency [37]. A major advantage of ultra thin silicon membranes is their flexibility, which makes their use possible as TE sensors, e.g. for biomedical applications [38].

Since previous works indicated the possibility that the S may be enhanced by the formation of impurity bands in heavily doped membranes [10, 11], we have also considered 5.4 nm thick membranes with explicit phosphorous boron substitutional defects corresponding to carrier concentrations of 1.5 and 3 10^{20} cm^{-3}. These calculations show that in the range of concentrations considered, S is not enhanced with respect to that computed using the electronic structure of intrinsic membranes (Figures S5, S6). This result rules out the impurity band effect proposed in [10], but it is still possible that large S is boosted by phonon drag [39].

In conclusion, our calculations show that silicon membranes covered with native oxide layers exhibit improved ZT up to 0.2 at room temperature, with an optimal thickness of $6-7$ nm. Even though these systems can only generate power in the microwatt range, several applications involving autonomously powered sensors may be envisaged.

Supplementary material contains a description of the computational methods, lattice thermal conductivity, analysis of electronic band structures, energy dependent electrical conductivity, and Seebeck coefficients of doped membranes.

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