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# Optimal Topologies for Cascaded Sub-Multilevel Converters

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**Abstract**

The general function of a multilevel converter is to synthesize a desired output voltage from several levels of dc voltages as inputs. In order to increase the steps in the output voltage, a new topology is recommended in [1], which benefits from a series connection of sub-multilevel converters. In the procedure described in this reference, despite all the advantages, it is not possible to produce all the steps (odd and even) in the output. In addition, for producing an output voltage with a constant number of steps, there are different configurations with a different number of components. In this paper, the optimal structures for this topology are investigated for various objectives such as minimum number of switches and dc voltage sources and minimum standing voltage on the switches for producing the maximum output voltage steps. Two new algorithms for determining the dc voltage sources magnitudes have been proposed. Finally, in order to verify the theoretical issues, simulation and experimental results for a 49-level converter with a maximum output voltage of 200V are presented.

**Key Words:** Bidirectional switch, Cascaded multilevel converter, Lagrange multiplier, Multilevel converter, Sub-multilevel converter

## I. INTRODUCTION

The concept of utilizing multiple small voltage levels to perform power conversion was presented by an MIT researcher over thirty years ago [2], [3]. The advantages of this multilevel approach include good power quality, good electro-magnetic compatibility, low switching losses and high voltage capability [4].

The first multilevel converter can be attributed to Baker and Bannister, who patented the cascaded H-bridge in 1975. In 1980, Baker patented a diode-clamped topology which is still the most widely used. This topology utilizes a bank of series capacitors to split the dc bus voltage [3], [5]. In 1992, Meynard and Foch patented the flying-capacitor architecture. Instead of a series of connected capacitors, this topology uses floating capacitors to clamp the voltage levels [6]. In the same year, Osagawara and his colleagues presented a new approach. They considered a standard current source inverter but increased the number of current levels instead of voltage levels. In this design, the semiconductors must block the entire voltage, but share the load current [7]. From 1992 till now, several combinatorial designs have also emerged [8], [9], by means of cascading the fundamental topologies [10], [11]; they are called hybrid topologies [12]. These designs can create higher power quality for a given number of semiconductor devices than the fundamental topologies alone due to a multiplying effect of the number of levels. Mixed-level hybrid

multilevel cells [13] belong to this family of converters. In this kind of converter, the H-bridge cells of the cascaded leg are substituted with diode-clamped or flying-capacitors. To reduce the number of separate dc sources for high-voltage-high-power applications new configurations have also been presented [14], [15]. Some soft switched multilevel converters are presented in the literature [16], [17] that consider several different implementations. The aim of soft-switch converters is to reduce the switching losses and increasing the efficiency of multilevel converters. Recently, several multilevel converter topologies have been developed [18]–[20].

The cascaded H-bridge converter is a very modular solution based on a widely commercialized product. This has a good effect on the reliability and maintenance of the system since the cells have high availability, intrinsic reliability and a relatively low cost. Unfortunately, these converters do have some disadvantages. One particular disadvantage is the greater number of power semiconductor switches needed. Although, lower voltage rated switches can be utilized in a cascaded multilevel converter, each switch requires a related gate driver and protection circuits. This may cause the overall system to be more expensive and complex.

An attempt has been made in [1] to introduce a new topology for cascaded multilevel converters. This topology consists of series connected sub-multilevel converter blocks. It is necessary to mention that the hybrid and mixed-level hybrid multilevel converters are called sub-multilevel converters. However, these are combinations of two of the basic multilevel topologies or slight variations of them. In other words, the hybrid multilevel converters are composed of
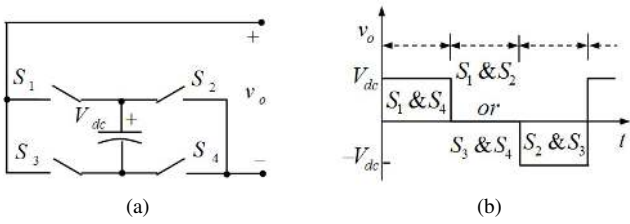
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Fig. 1.   (a) Basic unit presented in [1] (b) Typical output waveform of $v_o$.

several series-connected cells that present different dc voltage levels, modulation strategies, topologies, and/or semiconductor technologies operating in synergism. Based on these principles, the concept of hybrid multilevel converters can be generalized for different arrangements of dc voltage levels and distinct topologies for multilevel cells, increasing significantly the flexibility and complexity of their design. The topology presented in [1] is a new kind of cascaded sub-multilevel converter. In this topology, the modulation strategies and the structures of the different cells and the required switches are the same. By the presented algorithm in [1], it is not possible to create all the steps (odd and even) at the output voltage. In addition, for creating an output voltage with a constant number of steps, there are different structures with a different number of components. Thus, in order to reduce the cost of the converter, it is necessary to introduce an optimal structure with the minimum number of components. In this paper, in order to generate all the steps (odd and even) at the output voltage, two new procedures for calculating the magnitudes of the required dc voltage sources are proposed. In addition, this paper proposes an optimal structure for this type of multilevel converter with a high number of steps associated with a low number of power switches and dc voltage sources. This results in a reduction in cost for the converter. Finally, this paper includes a design example of a multilevel converter.

## II. PRESENTED TOPOLOGY IN [1]

The basic unit for the multilevel converter presented in [1], is illustrated in Fig. 1(a). This consists of a dc voltage source (with a voltage equal to $V_{dc}$) with four unidirectional switches. There are several arrangement that can be used to create such a unidirectional switch. For example, one insulated-gate bipolar transistor (IGBT) with one anti-parallel diode can be used. The output waveform of $v_o$ is shown in Fig. 1(b). It is noted that three levels can be achieved for $v_o$.

The basic unit shown in Fig. 1(a) can be extended as shown in Fig. 2 (a). The basic units in series can increase the possible values of $v_o$. If $n$ dc voltage sources are used in the extended unit as shown in Fig. 2 (a), then the number of output voltage steps ($N_{step}$) and switches ($N_{switch}$) are given by the following equations, respectively:

$$N_{step} = n(n+1) + 1 \qquad (1)$$
$$N_{switch} = 2(n+1). \qquad (2)$$

The presented extended unit requires bidirectional switches with the ability to block voltage and conducting current in both directions. There are several arrangements that can
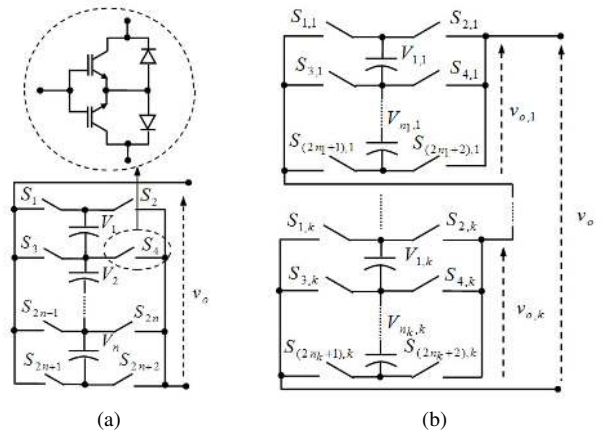


Fig. 2.   (a) Extended basic unit (b) $k$ basic units connected in series [1].

be used to create such a bidirectional switch [21]. In this paper, the common emitter configuration has been used. This configuration consists of two diodes and two IGBTs as shown in Fig. 2(a). The advantage of this configuration is that each bidirectional switch requires a gate driver circuit.

It is important to note that only two switches for each extended unit turn on in the different modes of converter operation. The extended basic units in series can increase the possible values of $v_o$. Fig. 2(b) shows $k$ basic units in series where the structure of the first unit, second unit, ..., and $k$th unit have $n_1, n_2, \cdots, n_k$ capacitors, respectively. In this case, the number of output voltage steps and switches are given by the following equations, respectively:

$$N_{step} = \prod_{i=1}^{k} [n_i(n_i + 1) + 1] \qquad (3)$$

$$N_{switch} = \sum_{i=1}^{k} [2(n_i + 1)]. \qquad (4)$$

The output voltage of the converter can be calculated as follows:

$$v_o(t) = \sum_{j=1}^{k} v_{o,j} \qquad (5)$$

and the peak value of the output voltage is calculated as follows:

$$V_{o,\max} = \sum_{j=1}^{k} \sum_{i=1}^{n_j} V_{i,j}. \qquad (6)$$

Although this topology requires multiple dc sources, in some systems they may be available through renewable energy sources such as photovoltaic panels or fuel cells or with energy storage devices such as capacitors or batteries. When an ac voltage is already available, multiple dc sources can be generated using isolated transformers and rectifiers (Fig. 3). In Fig. 3, by choosing proper values for the capacitors, the desired values for the capacitors voltages are obtained. For example, by choosing $C_{1,1} = 2C_{2,1} = 4C_{3,1} = \cdots$, we have $V_{1,1} = \frac{1}{2}V_{2,1} = \frac{1}{4}V_{3,1} = \cdots$.

It is necessary to point out that it is possible to have an equal value for $v_o$ over the different states of the switches.
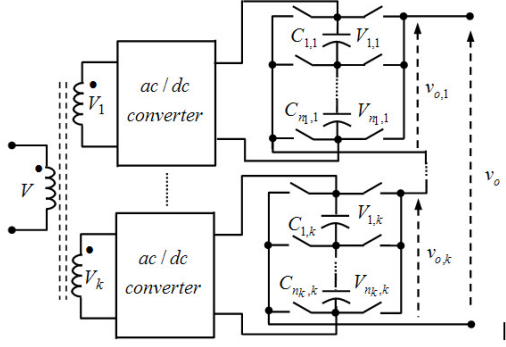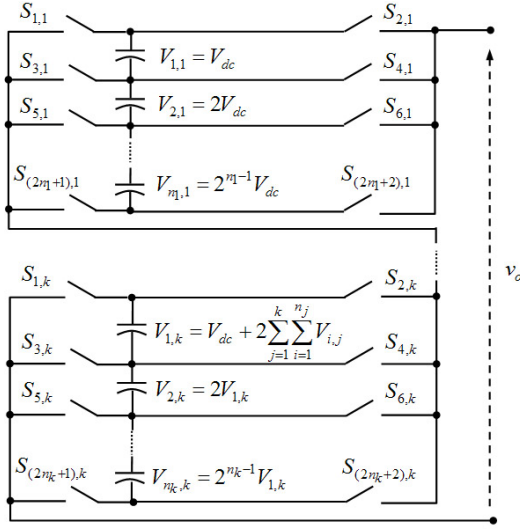
Fig. 3.   One of different methods for producing multiple dc sources.



Fig. 4.   Values of dc voltage sources for unequal values for $v_o$ recommended in [1].

In order to have unequal values for $v_o$ an algorithm has been presented for the determination of the values of the dc voltage sources in [1]. The values of the dc voltage sources have been indicated in Fig. 4. This algorithm can not produce all the steps (odd and even) at the output.

## III. PROPOSED ALGORITHIMS FOR THE DETERMINATION OF MAGNITUDES OF DC VOLTAGE SOURCES

As mentioned previously, to determine the values of the dc voltage sources, an algorithm was presented in [1] which utilized a lower number of dc voltage sources and power switches. But if the number of dc voltage sources in each stage precedes 2, all the steps (odd and even) will not be producible at the output. To demonstrate this limitation of the method presented in [1], consider the converter shown in Fig. 5. This figure shows a converter with two stages and each of the stages has three dc voltage sources based on the algorithm presented in [1]. Considering (3), this is a 169-level converter. It is clear that the first and second stages of this converter cannot produce $\pm 5pu$ or $\pm 10pu$ at the output voltage, respectively. Therefore, these steps and their combinations can not appear in the output
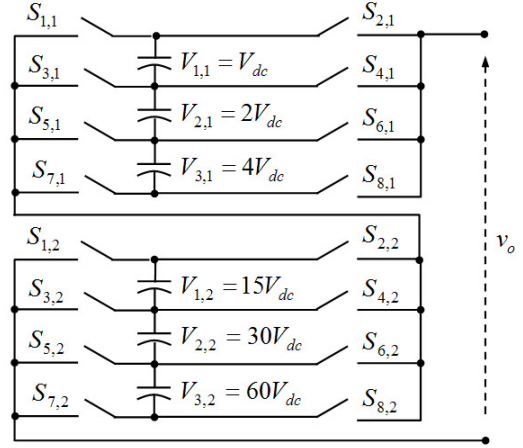


Fig. 5.   169-level converter based on [1].

voltage. In other words, the converter shown in Fig. 5 can not produce the following steps at the output voltage:

$$\pm 5pu; \pm 10pu; \pm 20pu; \pm 25pu; \pm 35pu; \pm 40pu;$$
$$\pm 50pu; \pm 55pu; \pm 65pu; \pm 68pu; \pm 69pu; \pm 70pu;$$
$$\pm 71pu; \pm 72pu; \pm 73pu; \pm 74pu; \pm 75pu; \pm 76pu;$$
$$\pm 77pu; \pm 78pu; \pm 79pu; \pm 80pu; \pm 81pu; \pm 82pu;$$
$$\pm 85pu; \pm 95pu; \pm 100pu; \pm 110pu;$$

To overcome this problem two new algorithms are proposed as follows.

### A. First Proposed Algorithm

In this algorithm it is proposed that the values for all of the dc voltage sources for generating odd and even steps can be calculated using the following relationships:
**First stage:**

$$V_{1,1} = V_{dc} \tag{7}$$
$$V_{j,1} = 2V_{dc} \qquad for \quad j = 2,3,\cdots,n_1 \tag{8}$$

**Second stage:**

$$V_{1,2} = V_{dc} + 2\sum_{j=1}^{n1} V_{j,1} = (4n_1 - 1)V_{dc} \tag{9}$$
$$V_{j,2} = 2(4n_1 - 1)V_{dc} \qquad for \quad j = 2,3,\cdots,n_2 \tag{10}$$

**$m$th stage:**

$$V_{1,m} = V_{dc} + 2\left(\sum_{i=1}^{m-1}\sum_{j=1}^{n_i} V_{j,i}\right) \tag{11}$$
$$V_{j,m} = 2V_{1,m} \qquad for \quad j = 2,3,\cdots,n_m. \tag{12}$$

One of the advantages of this algorithm when compare to the algorithm recommended in [1] is the ability to produce all of the steps at the output voltage. A reduction in the variety of the values of the dc voltage sources is another advantage of this algorithm. The disadvantage of this algorithm is that two or more switching states produce the same output voltage. These states are called redundant states. Obviously this kind

of redundancy is strictly related to the hardware architecture of the converter and the values of the dc voltage sources. In the proposed algorithm, the number of output voltage steps is obtained as follows:

$$N_{step} = \prod_{i=1}^{k}(4n_i - 1). \qquad (13)$$

### B. Second Proposed Algorithm

For a greater reduction in the variety of the values of the dc voltage sources, another new algorithm is proposed as follows:

**First stage:**

$$V_{j,1} = V_{dc} \qquad for \quad j = 1, 2, 3, \cdots, n_1 \qquad (14)$$

**Second stage:**

$$V_{j,2} = V_{dc} + 2\sum_{i=1}^{n_1} V_{i,1} = (2n_1 + 1)V_{dc}$$
$$for \quad j = 1, 2, \cdots, n_2 \quad (15)$$

**$m$th stage:**

$$V_{j,m} = V_{dc} + 2\left(\sum_{i=1}^{m-1}\sum_{l=1}^{n_i} V_{j,l}\right) \quad for \; j = 1, 2, \cdots, n_m. \; (16)$$

This algorithm produces redundant states. In this algorithm, the number of output voltage steps is given as follows:

$$N_{step} = \prod_{i=1}^{k}(2n_i + 1). \qquad (17)$$

Considering (13) and (17), it is clear that the first proposed algorithm can generate a larger number of steps. In other words, the number of redundant states in the first algorithm is less than with the second algorithm. In contrast, in the second algorithm, the variety of the values of the dc voltage sources is less than with the first algorithm.

## IV. OPTIMAL STRUCTURES BASED ON THE TOPOLOGY RECOMMENDED IN [1]

For a constant number of dc voltage sources and their possible arrangements in different stages, it is possible to obtain a different number of steps at the output voltage utilizing a different number of power switches. For a constant number of dc voltage sources all of the possible configurations are summarized in Table I. As shown in this Table, for more than three dc voltage sources, some configurations are created which produce a different number of steps at the output while utilizing the same number of dc voltage sources and power switches. For example with four dc voltage sources and 12 power switches, if there are three dc voltage sources in the first stage and one in the second stage, the number of steps at the output will be 39. While using two dc voltage sources in each stage and utilizing the same number of power switches the output steps will be equal to 49. By utilizing more dc voltage sources, the repetition of such states will grow.

As shown in Table I, there is a great variety of configurations for a constant number of dc voltage sources. Therefore, we must be able to choose the optimal structure for a special

state because this ability leads to a reduction in the size, weight and cost of the converter. Considering the great variety of existing configurations, we propose some of the optimal structures in the next sections.

TABLE I
DIFFERENT CONFIGURATIONS

| No. of sources | Possibility configurations | | | | | | | | No. of switches | No. of steps |
|---|---|---|---|---|---|---|---|---|---|---|
| | $n_1$ | $n_2$ | $n_3$ | $n_4$ | $n_5$ | $n_6$ | $\cdots$ | $n_{k,j}$ | | |
| 1 | 1 | | | | | | | | 4 | 3 |
| 2 | 1 | 1 | | | | | | | 8 | 9 |
| | 2 | | | | | | | | 6 | 7 |
| 3 | 1 | 1 | 1 | | | | | | 12 | 27 |
| | 2 | 1 | | | | | | | 10 | 21 |
| | 3 | | | | | | | | 8 | 13 |
| 4 | 1 | 1 | 1 | 1 | | | | | 16 | 81 |
| | 2 | 1 | 1 | | | | | | 14 | 63 |
| | 2 | 2 | | | | | | | 12 | 49 |
| | 3 | 1 | | | | | | | 12 | 39 |
| | 4 | | | | | | | | 10 | 21 |
| 5 | 1 | 1 | 1 | 1 | 1 | | | | 20 | 243 |
| | 2 | 1 | 1 | 1 | | | | | 18 | 189 |
| | 2 | 2 | 1 | | | | | | 16 | 147 |
| | 3 | 1 | 1 | | | | | | 16 | 117 |
| | 3 | 2 | | | | | | | 14 | 91 |
| | 4 | 1 | | | | | | | 14 | 63 |
| | 5 | | | | | | | | 12 | 31 |
| 5 | 1 | 1 | 1 | 1 | 1 | | | | 20 | 243 |
| | 2 | 1 | 1 | 1 | | | | | 18 | 189 |
| | 2 | 2 | 1 | | | | | | 16 | 147 |
| | 3 | 1 | 1 | | | | | | 16 | 117 |
| | 3 | 2 | | | | | | | 14 | 91 |
| | 4 | 1 | | | | | | | 14 | 63 |
| | 5 | | | | | | | | 12 | 31 |
| 6 | 1 | 1 | 1 | 1 | 1 | 1 | | | 24 | 729 |
| | 2 | 1 | 1 | 1 | 1 | | | | 22 | 567 |
| | 2 | 2 | 1 | 1 | | | | | 20 | 324 |
| | 2 | 2 | 2 | | | | | | 18 | 343 |
| | 3 | 1 | 1 | 1 | | | | | 20 | 351 |
| | 3 | 2 | 1 | | | | | | 18 | 273 |
| | 3 | 3 | | | | | | | 16 | 269 |
| | 4 | 1 | 1 | | | | | | 18 | 189 |
| | 4 | 2 | | | | | | | 16 | 147 |
| | 5 | 1 | | | | | | | 16 | 93 |
| | 6 | | | | | | | | 14 | 43 |
| $\vdots$ | $\vdots$ | $\vdots$ | $\vdots$ | $\vdots$ | $\vdots$ | $\vdots$ | | | $\vdots$ | $\vdots$ |

### A. Optimal Structure for the Minimum Number of Switches with a Constant Number of dc Voltage Sources

The question concerning the proposed structure is that if the number of dc voltage sources ($N_{capacitor}$) is constant, which topology can provide a minimum number of switches ($N_{switch}$).

Suppose the converter consists of a series of $k$ stages each with $n_i$ dc voltage sources ($i = 1, 2, \cdots, k$). Thus:

$$N_{capacitor} = n_1 + n_2 + \cdots + n_k = cte. \qquad (18)$$

Considering (4), the number of switches is given by the following equation:

$$N_{switch} = [2(n_1 + 1)] + [2(n_2 + 1)] + \cdots + [2(n_k + 1)]. (19)$$

The minimum number of switches occurs when using only one stage (Fig. 2(a)). This is because each of the stage two switches are common between two series dc voltage sources. It is obvious that by this topology the minimum number of voltage steps can be produced.

### B. Optimal Structure for a Minimum Number of Switches with a Constant Number of Voltage Steps

The objective of a multilevel converter is to obtain the maximum step number with a minimum of switches. The question concerning the proposed structure is that if the number of voltage steps ($N_{step}$) is constant, which topology can provide a minimum number of switches.

Suppose a converter consists of a series of $k$ stages each with $n_i$ ($i = 1, 2, \cdots, k$) dc voltage sources as shown in Fig. 4. The number of switches is given by (19). Considering (3), the number of output steps is given as follows:

$$N_{step} = \sum_{j=1}^{k} [n_j(n_j + 1) + 1] = cte. \tag{20}$$

Using the method of the lagrange multipliers, such problems are solved. For this method, the cost function is defined as follows:

$$f = N_{switch} + \lambda \cdot g. \tag{21}$$

In the above equation, $\lambda$ is the lagrange multiplier and the function $g$ is as follows:

$$g = N_{step} - cte. = 0. \tag{22}$$

According to the method of the lagrange multipliers, the minimum number of switches can be calculated by solving the following equations:

$$\frac{\partial f}{\partial n_j} = \frac{\partial N_{switch}}{\partial n_j} + \lambda \frac{\partial g}{\partial n_j} = 0 \quad for\ j = 1, 2, \cdots, k \tag{23}$$

$$\frac{\partial f}{\partial \lambda} = g = 0. \tag{24}$$

Equations (23) and (24) can be rewritten as follows:

$$2 + \lambda(2n_1 + 1) \times [n_2(n_2 + 1) + 1] \times [n_3(n_3 + 1) + 1] \times$$
$$\cdots \times [n_k(n_k + 1) + 1] = 0$$
$$2 + \lambda[n_1(n_1 + 1) + 1] \times (2n_2 + 1) \times [n_3(n_3 + 1) + 1] \times$$
$$\cdots \times [n_k(n_k + 1) + 1] = 0$$
$$2 + \lambda[n_1(n_1 + 1) + 1] \times [n_2(n_2 + 1) + 1] \times (2n_3 + 1) \times$$
$$\cdots \times [n_k(n_k + 1) + 1] = 0 \tag{25}$$
$$\vdots$$
$$2 + \lambda[n_1(n_1 + 1) + 1] \times [n_2(n_2 + 1) + 1] \times$$
$$\cdots \times (2n_k + 1) = 0$$
$$[n_1(n_1 + 1) + 1] \times [n_2(n_2 + 1) + 1] \times$$
$$\cdots \times [n_k(n_k + 1) + 1] - cte. = 0.$$

The optimal values of $\lambda, n_1, n_2, \cdots, n_k$ are determined by solving the above equations. In order to solve the above equations set, the following changes are applied to the variables:

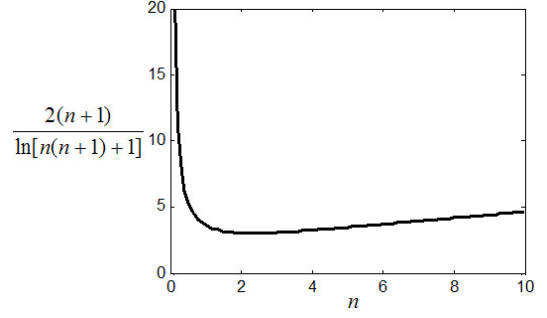$$n_j(n_j + 1) + 1 = S_j \quad for \quad j = 1, 2, \cdots, k. \tag{26}$$



Fig. 6.    Variation of $2(n + 1)/\ln[n(n + 1) + 1]$ versus $n$.

Now (25) can be rewritten as follows:

$$2 + \lambda \times \left(\sqrt{4S_1 - 3}\right) \times S_2 \times S_3 \times S_4 \times \cdots \times S_k = 0$$
$$2 + \lambda \times S_1 \times \left(\sqrt{4S_2 - 3}\right) \times S_3 \times S_4 \times \cdots \times S_k = 0$$
$$\vdots \tag{27}$$
$$2 + \lambda \times S_1 \times S_2 \times S_3 \times S_4 \times \cdots \times S_{k-1} \times \left(\sqrt{4S_k - 3}\right) = 0$$
$$S_1 \times S_2 \times S_3 \times S_4 \times \cdots \times S_k - cte. = 0.$$

Notice that $n_j$ ($j = 1, 2, \cdots, k$) is an integer and thus $S_j$ is an integer too. In (27), if $n_j$ is substituted by an integer between zero and infinity, the answer-set for $S_j$ will be:

$$S_j = \{1, 3, 7, 13, 21, 31, \cdots\}. \tag{28}$$

Considering (27), the answer-set for $S_j$ is obtained as follows:

$$S_1 = S_2 = S_3 = \cdots = S_k = S. \tag{29}$$

From (26) and (29) it is obvious that:

$$n_1 = n_2 = n_3 = \cdots = n_k = n. \tag{30}$$

The above equation denotes that in order to use the minimum number of switches for producing the maximum number of voltage steps, the number of switches must be the same in all stages. Substituting (30) into (19) and (20) results in:

$$N_{switch} = 2k(n + 1) \tag{31}$$
$$N_{step} = [n(n + 1) + 1]^k. \tag{32}$$

Equation (32) can be written as follows:

$$k = \frac{\ln N_{step}}{\ln[n(n + 1) + 1]}. \tag{33}$$

Therefore the minimum number of switches will be:

$$N_{switch} = \frac{2(n + 1)}{\ln[n(n + 1) + 1]} \ln N_{step}. \tag{34}$$

Since $N_{step}$ is constant, $N_{switch}$ will be minimized when $2(n + 1)/\ln[n(n + 1) + 1]$ tends to the minimum. Fig. 6 shows the variation of $2(n + 1)/\ln[n(n + 1) + 1]$ versus $n$. It is clear that the minimum number of switches is obtained for $n = 2$. Therefore, a structure consisting of a series of extended basic units with two dc voltage sources can provide the maximum step voltages for $v_o$. Fig. 7 shows the corresponding structure.

It is necessary to point out that the number of components and the number of series units is integers. Therefore, if an integer number is not obtained, the nearest integer number is certainly the proposed solution.
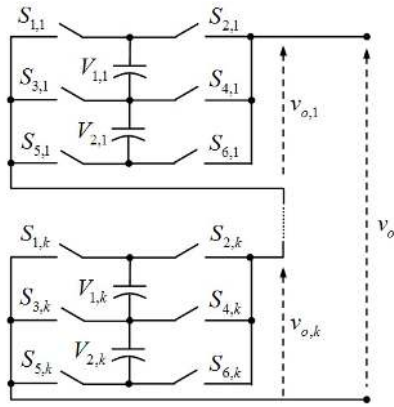
Fig. 7.   Optimal structure for minimum number of switches with constant number of voltage steps.
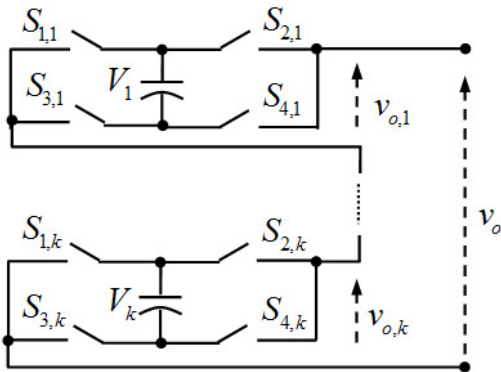


Fig. 8.   Optimal structure for minimum number of dc voltage sources with constant number of voltage steps.

### C. Optimal Structure for the Minimum Number of dc Voltage Sources with a Constant Number of Voltage Steps

The next question is that if $N_{step}$ is the number of voltage steps considered for voltage $v_o$, which topology with a minimum number of dc voltage sources can satisfy this need.

Suppose the converter consists of a series of $k$ stages each with $n_i$ $(i = 1, 2, \cdots, k)$ dc voltage sources. The number of output voltage steps is given by (20) and the number of dc voltage sources is given as follows:

$$N_{capacitor} = n_1 + n_2 + \cdots + n_k. \tag{35}$$

Using the method of the lagrange multiplier the optimal answer is obtained by solving the following equation:

$$\sqrt{4S_j - 3} = S_j \qquad for \quad j = 1, 2, \cdots, k. \tag{36}$$

Considering (36), it is clear that:

$$S_j = 3 \qquad for \quad j = 1, 2, \cdots, k. \tag{37}$$

Considering (26) and (37), we have:

$$n_1 = n_2 = n_3 = \cdots = n_k = 1. \tag{38}$$

In other words, as illustrated in Fig. 8, the minimum number of dc voltage sources may be obtained for one dc voltage source in each stage.
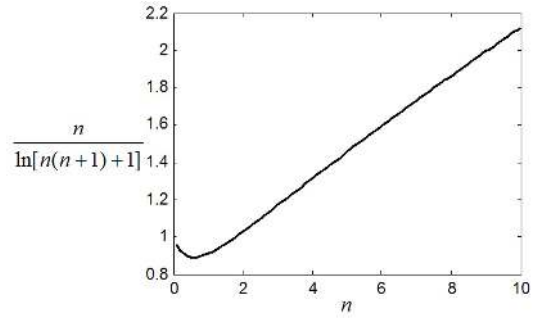


Fig. 9.   Variation of $n/\ln[n(n + 1) + 1]$ versus $n$.

The second method for proving the above conclusion is as follows. It can be proven that the minimum number of dc voltage sources may be obtained for an equal number of dc voltage sources in each stage. With reference to Fig. 4, the number of the dc voltage sources is given by:

$$N_{capacitor} = n \times k. \tag{39}$$

Considering (33), (39) can be written as follows:

$$N_{capacitor} = \frac{n}{\ln[n(n + 1) + 1]} \ln N_{step}. \tag{40}$$

Since $N_{step}$ is constant, $N_{capacitor}$ will be minimized when $n/\ln[n(n + 1) + 1]$ tends to minimum. Fig. 9 shows the corresponding figure, where $n = 1$ gives the minimum number of dc voltage sources to realize $N_{step}$ values for the voltage.

### D. Optimal Structure for the Minimum Standing Voltage of Switches with Constant Number of Voltage Steps

The voltage and current ratings of the switches in a multi-level converter play important roles in the cost and realization of the multilevel converter. In all topologies, the currents of all the switches are equal to the rated current of the load. However, this is, not true for the voltage. The question is that if $N_{step}$ voltages are considered for $v_o$, which topology uses the switches with the minimum voltage. Suppose that the peak voltage of the switches is represented by:

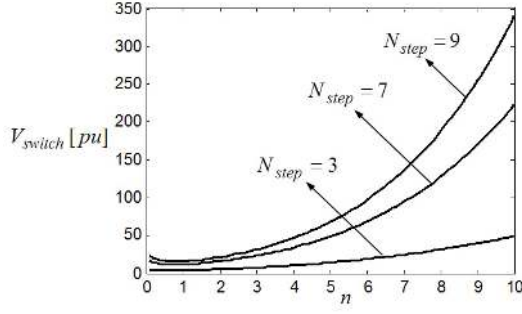$$V_{switch} = \sum_{j=1}^{k} V_{stage,j}. \tag{41}$$

In the above equation, $V_{stage,j}$ represents the peak voltage of the switches in stage $j$. Therefore, (41) can be considered as a criterion for the comparison of different topologies from the maximum voltage on the switches [20], [22]. A lower criterion indicates that a smaller voltage is applied at the terminal of the switches in the topology, which is considered an advantage. With reference to Fig. 4, the following equations can be obtained:

The maximum standing voltage on $S_{1,1}$, $(V_{S1,1})$, is as follows:

$$V_{S1,1} = V_{1,1} + V_{2,1} + V_{3,1} + \cdots + V_{n,1}. \tag{42}$$

Equation (42) can be simplified as:

$$V_{S1,1} = (2^n - 1)V_{dc}. \tag{43}$$

Fig. 10.   Variation of $V_{switch}$ versus $n$.


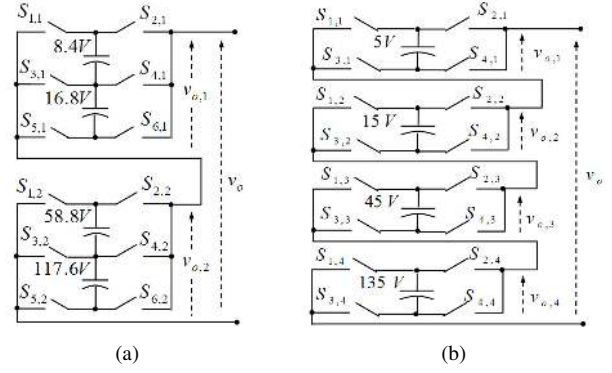
(a)                                    (b)

Fig. 11.   Optimal structures; (a) considering the minimum used switches;
(b) considering the minimum used dc voltage sources and minimum
standing voltage of switches.

The maximum standing voltage on $S_{3,1}$, $(V_{S3,1})$, is as follows:

$$V_{S3,1} = V_{2,1} + V_{3,1} + \cdots + V_{n,1} = V_{S1,1} - (2^1 - 1)V_{dc}. \quad (44)$$

The maximum standing voltage on $S_{2n-1,1}$, $(V_{S(2n-1),1})$ is calculated as follows:

$$V_{S(2n-1),1} = V_{n,1} = V_{S1,1} - (2^{n-1} - 1)V_{dc}. \quad (45)$$

Finally, the maximum standing voltage on $S_{2n+1,1}$, $(V_{S(2n+1),1})$, is obtained as follows:

$$V_{S(2n+1),1} = V_{1,1} + V_{2,1} + V_{3,1} + \cdots + V_{n,1} = V_{S1,1}. \quad (46)$$

Thus, the maximum standing voltage on the switches in the first stage is calculated as follows:

$$V_{stage,1} = 2(V_{S1,1} + V_{S3,1} + \cdots + V_{S(2n-1),1} + V_{S(2n+1),1})$$
$$= n2^{n+1}V_{dc}. \quad (47)$$

Considering (41), the maximum standing voltage on the switches can be obtained as:

$$V_{switch} = (n2^{n+1}) \times (V_{1,1} + V_{1,2} + V_{1,3} + \cdots + V_{1,k}). \quad (48)$$

The above equation can be rewritten as:

$$V_{switch} = (n2^{n+1}) \times (1 + x + x^2 + \cdots + x^{k-1})V_{dc} \quad (49)$$

where $x$ is calculated as follows:

$$x = 2^{n+1} - 1. \quad (50)$$

Equation (49) can be simplified as:

$$V_{switch} = (n2^{n+1}) \times \left( \frac{x^k - 1}{x - 1} \right) V_{dc}. \quad (51)$$

Considering (33) and (50), the maximum standing voltage on the switches will be:

$$V_{switch} = (n2^n) \frac{(2^{n+1} - 1)^{\left( \frac{\ln N_{step}}{\ln[n(n+1)+1]} \right)} - 1}{2^n - 1} V_{dc}. \quad (52)$$

The variation of $V_{switch}$ is shown in Fig. 10. As illustrated in Fig. 10, the $V_{switch}$ is minimized for $n = 1$. Therefore, the optimal structure from the minimum voltage of the switch point of view consists of series units with one dc voltage source (Fig. 8).

## V. DESIGN OF A MULTILEVEL CONVERTER BASED ON THE RECOMMENDATIONS IN [1]

The problem is to design a typical 200V single-phase multilevel converter with minimum of 48 voltage steps. It is clear that more voltage steps will provide a better design. The optimal structures for the topology recommended in [1] were investigated for various objectives. Note that the on-state voltage drops of the switches have been neglected. Based on Section IV, Fig. 11(a) shows the optimal structure for the minimum number of switches. With reference to Fig. 11(a), the number of switches and dc voltage sources are $N_{switch} = 12$ and $N_{capacitor} = 4$, respectively. In this design, the number of voltage steps is 49. The optimal structure based on the minimum number of dc voltage sources and the minimum standing voltage of the switches has been shown in Fig. 11(b). The number of switches and dc voltage sources are 16 and 4, respectively. In this structure, the number of voltage steps is 81.

It is important to note that the optimal structures have been obtained based on bidirectional switches. The structure shown in Fig. 11(b) can be constructed with unidirectional switches. So, from this point of view, the converters shown in Figs. 11(a) and 11(b) require 24 and 16 IGBTs, respectively. Therefore, the required number of IGBTs in the converter shown in Fig. 11(b) is less than the converter in Fig. 11 (a). It is necessary to note that in both of the converters the number of diodes is equal to the number of IGBTs. Multilevel single-dc-bus units can be constructed with unidirectional switches. Therefore, the topology shown in Fig. 11(b) not only needs the minimum number of dc voltage sources and the minimum standing voltage of switches but also it needs the minimum number of IGBTs and diodes. Each bidirectional switch used needs one gate driver circuit. So, from this point of view, the topologies shown in Figs. 11(a) and 11(b) require 12 and 16 gate driver circuits, respectively.

The standing voltages of the switches in Figs. 11(a) and 11(b) are 1075.2V and 800V, respectively. It is necessary to point out that the structure proposed in Fig. 11(a) provides 49 voltage steps using 12 switches and a standing voltage of 1075.2V, whereas the structure given in Fig. 11(a) produces 81 voltage steps using 16 switches and a standing voltage of 800V.
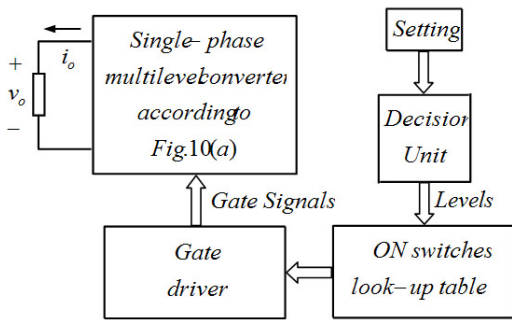
Fig. 12.    Control block diagram.



Fig. 13.    Output voltage.



Fig. 14.    Output current.

## VI. SIMULATION RESULTS

To show the performance of the proposed multilevel converters, the multilevel converter shown in Fig. 11(a) is simulated. PSCAD/EMTDC software has been used for this simulation. In the simulation, the switches are assumed ideal. There are several modulation strategies for multilevel converters [23]–[27]. In this paper, the fundamental frequency switching technique has been used. The benefit of the fundamental frequency switching method is its low switching frequency compared to other control methods [25]. Table II shows the ON switches look-up table for the multilevel converter shown in Fig. 11(a). Note that there are different switching patterns for producing the zero level in each unit, and that only one of them is shown in Table II. Fig. 12 shows a control block diagram of the converter. The main idea in the control strategy is to deliver to the load a voltage that minimizes the error with respect to the reference voltage. It is important to note that the calculation of the optimal switching angles for different goals such as the elimination of selected harmonics and minimizing the total harmonic distortion (THD) is not the objective of this paper.

TABLE II
ON SWITCHES LOOK-UP TABLE FOR MULTILEVEL
CONVERTER SHOWN IN FIG. 11(A)

| $v_o[pu]$ $(8.4V = 1pu)$ | | -24 | $\cdots$ | -1 | 0 | 1 | $\cdots$ | 24 |
|---|---|---|---|---|---|---|---|---|
| Switches state | $S_{1,1}$ | on | $\cdots$ | on | on | off | $\cdots$ | off |
| | $S_{2,1}$ | off | $\cdots$ | off | on | on | $\cdots$ | on |
| | $S_{3,1}$ | off | $\cdots$ | off | off | on | $\cdots$ | off |
| | $S_{4,1}$ | off | $\cdots$ | on | off | off | $\cdots$ | off |
| | $S_{5,1}$ | off | $\cdots$ | off | off | off | $\cdots$ | on |
| | $S_{6,1}$ | on | $\cdots$ | off | off | off | $\cdots$ | off |
| | $S_{1,2}$ | on | $\cdots$ | off | off | off | $\cdots$ | off |
| | $S_{2,2}$ | off | $\cdots$ | off | off | off | $\cdots$ | on |
| | $S_{3,2}$ | off | $\cdots$ | off | off | off | $\cdots$ | off |
| | $S_{4,2}$ | off | $\cdots$ | off | off | off | $\cdots$ | off |
| | $S_{5,2}$ | off | $\cdots$ | on | on | on | $\cdots$ | on |
| | $S_{6,2}$ | on | $\cdots$ | on | on | on | $\cdots$ | off |

The first study is for investigating the waveforms of the output and the standing voltage on the switches. For this reason, the converter has been adjusted to produce a 50Hz, 29-level staircase waveform. A test has been made on the R-L load ($R = 100\Omega$ and $L = 55mH$). Figs. 13 and 14
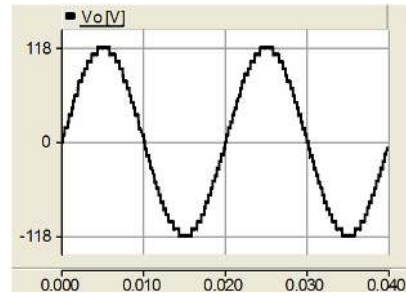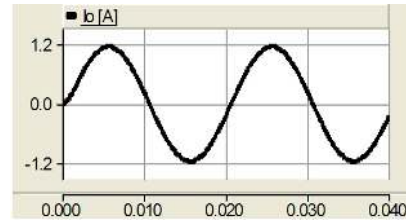
show the simulation results for the output voltage and current, respectively. The output voltage is a staircase waveform. The amplitudes of the steps are 8.4V. Therefore, the amplitude of the output voltage is 117.6V. The amplitude of the output current is 1.16A. The Fourier series expansion of the (stepped) output voltages waveform of the multilevel converter, as shown in Fig. 13, is made up from a fundamental frequency sine wave and an infinite number of odd harmonics. As can be seen from the waveforms, the output current is almost sinusoidal. Since the load of the converters is almost a low pass filter (R-L), the output currents contain less high order harmonics than the output voltages. For this example, the THDs of the output voltage and current based on the simulation are 1.92% and 0.57%, respectively. To generate a desired output with the best quality waveform, the number of the voltage steps should be increased.

Fig. 15 shows the output voltage of the different units. Each unit generates a quasi-square waveform with positive, zero and negative values. The overall output voltage of the converter is the sum of the outputs of units.

Fig. 16 shows the standing voltage of the switches in the left side of the multilevel converter. As this figure shows, the switches have the ability to block voltage with both positive and negative polarities. Zero values show the ON state of the switches. With reference to Fig. 16, the maximum standing voltage of the switches $S_{1,1}$, $S_{3,1}$, $S_{5,1}$, $S_{1,2}$, $S_{3,2}$ and $S_{5,2}$ are 25.2V, 16.8V, 25.2V, 176.4V, 117.6V and 176.4V, respectively. Therefore, the peak voltage of the switches on the left side of this converter is 537.6V. The peak voltage of the switches on the right side of the converter has the same value. Therefore, the peak voltage of the switches in this converter is 1075.2V. This result has good agreement with the given theoretical analysis.

## VII. EXPERIMENTAL RESULTS

To examine the performance of the proposed multilevel converter in the generation of different voltage waveforms, a
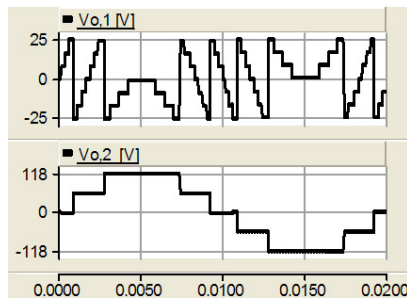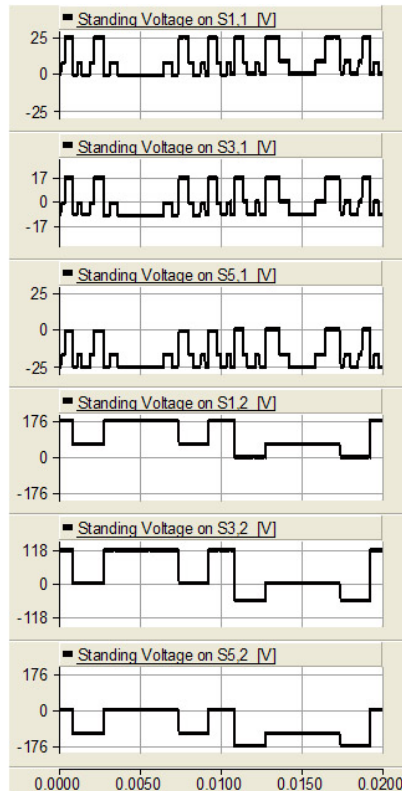
Fig. 15.   Outputs for different units.


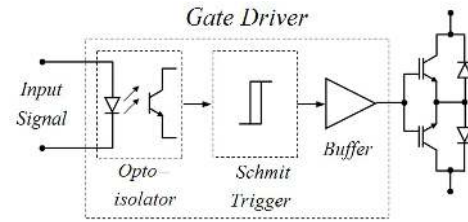Fig. 16.   Standing voltage for different switches.


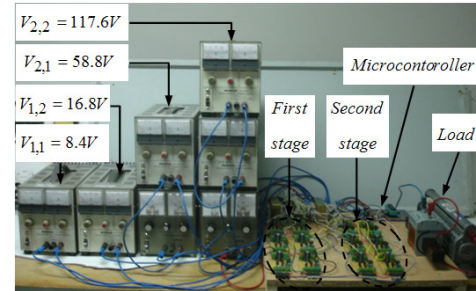Fig. 17.   Gate driver circuit of bi-directional switch.


Fig. 18.   Experimental set-up of the 49-level converter.

in series. It is important to note that designing the required dc voltage sources by different available methods such as isolated transformers and rectifiers (as shown in Fig. 3) is not the objective of this paper.

The ON switches look-up table shown in Table II has been used in the implemented multilevel converter. The states of the ON/OFF switches in different output levels are saved in the memory of the microcontroller. The main idea of the control strategy is to deliver a voltage to the load that minimizes the error with respect to the desired reference voltage. Considering the amplitude of the instantaneous desired reference voltage, the microcontroller sends the commands for the ON/OFF states switches based on Table II to the gate driver circuits of the switches. The 89C52 microcontroller by ATMEL Company has been used to generate the switching patterns. Fig. 18 shows the hardware of the implemented set-up.

The first experimental study is for showing the capability of the proposed multilevel converter in the generation of different voltage waveforms. It is assumed that the three time intervals and the related equations of the output voltage waveforms, which should be generated by the proposed multilevel converter, are as follows:

$$v_o(t) = \begin{cases} 120\cos(100\pi t) & 0 \leq t < 20ms \\ 80\sin(100\pi t) & 20 \leq< 40ms \\ 170\sin(100\pi t) + 60\sin(300\pi t) & 40 \leq< 60ms \end{cases}$$

Fig. 19 shows the experimental and simulation output voltage waveforms. As can be seen, the results verify the ability of proposed converter in the generation of the desired voltage waveforms. The experimental results show good agreement with simulation results.

The second study was for investigating the waveform of the output current and an evaluation of the efficiency of the converter. For this reason, the converter has been adjusted to produce a 50Hz, 29-level staircase waveform. A test has been made on the R-L load ($R = 100\Omega$ and $L = 55mH$). Fig. 20 shows the experimental output current. The experimental

single-phase 49-level multilevel converter prototype is implemented based on the proposed topology shown in Fig. 11(a).

The proposed multilevel converter requires bidirectional switches with the ability to block voltage and conduct current in both directions. As mentioned previously, common emitter anti-parallel IGBTs with a diode pair arrangement have been used in this paper. The IGBTs of the prototype are BUP306D with internal anti-parallel diodes. Fig. 17 shows the isolator and driver circuit of each bidirectional switch. These circuits consist of an opto-isolator, a schmit trigger and a buffer. Each bidirectional switch in the converter requires an isolated driver circuit. The isolation can be provided using either pulse transformers or opto-isolators. Opto-isolators can work in a wide range of input signal pulse widths, but a separate isolated power supply is required for each switching device.

The converter is fed by independent dc voltage sources with a variable output voltage to adjust the applied input voltages to the converter. For synthesizing dc voltage sources with high magnitudes, multiple small dc voltage sources have been used
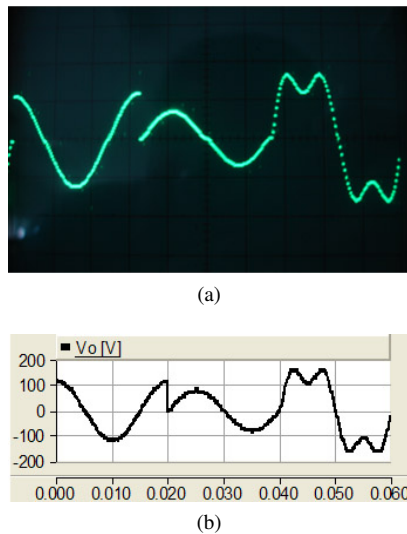
(a)



(b)

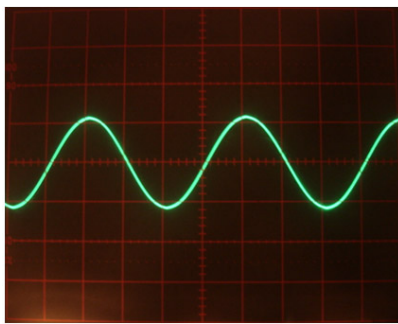Fig. 19.  Output voltage; (a) experimental result (by 100:1 probe); (b) Simulation result.



Fig. 20.  Experimental output current (by 1:1 probe).

results correspond very well with the simulation results seen in Fig. 14.

For calculating the efficiency of the converter ($\eta$) based on measurements, it is necessary to measure the total input ($P_{in,total}$) and output ($P_o$) powers. Then, the efficiency can be easily calculated by the following equation:

$$\eta = \frac{P_o}{P_{in,total}}. \qquad (53)$$

The total input power is the sum of the output power of the dc voltage sources. Table III summarizes the values of the different powers and the efficiency of the converter. The efficiency of the converter depends on the applied control method. As mentioned previously, the fundamental frequency control method has been used in this paper. As a result, the converter has high efficiency.

TABLE III
VALUES OF DIFFERENT POWERS AND EFFICIENCY OF THE CONVERTER

| Input powers to the converter | | | | Output power | Efficiency |
|---|---|---|---|---|---|
| By 8.4V source | By 16.8V source | By 58.8V source | By 117.6V source | | |
| 1.8W | 3.9W | 18.7W | 38.2W | 67.8W | %92.33 |

## VIII. CONCLUSIONS

In this paper, two new algorithms for the determination of the magnitudes of dc voltage sources have been proposed for the topology recommended in [1]. These algorithms can provide all steps (odd and even). It was shown that the structure consisting of units with two dc voltage sources is the best case to keep the minimum number of switches for a certain number of voltage steps. In addition, it was proven that the topology, consisting of units with one dc voltage source, is the optimal structure for minimizing the standing voltage on the switches, and that it minimizes the number of dc voltage sources.

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