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Area, Performance and Testability

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Area, Performance and Testability

Catherine H. Gebotys
and
Mohamed I. Elmasry

University of Waterloo

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To

Robert Joseph and Kathleen Vanessa Gebotys

and

Elizabeth, Carmen, Samir, Nadia and Hassan Elmasry

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PREFACE

Although research in architectural synthesis has been conducted for over ten years it has had very little impact on industry. This in our view is due to the inability of current architectural synthesizers to provide area-delay competitive (or "optimal") architectures, that will support interfaces to analog, asynchronous, and other complex processes. They also fail to incorporate testability. The OASIC (optimal architectural synthesis with interface constraints) architectural synthesizer and the CATREE (computer aided trees) synthesizer demonstrate how these problems can be solved.

Traditionally architectural synthesis is viewed as NP hard and therefore most research has involved heuristics. OASIC demonstrates by using an IP approach (using polyhedral analysis), that most input algorithms can be synthesized very fast into globally optimal architectures. Since a mathematical model is used, complex interface constraints can easily be incorporated and solved.

Research in test incorporation has in general been separate from synthesis research. This is due to the fact that traditional test research has been at the gate or lower level of design representation. Nevertheless as technologies scale down, and complexity of design scales up, the push for reducing testing times is increased. On way to deal with this is to incorporate test strategies early in the design process. The second half of this text examines an approach for integrating architectural synthesis with test incorporation. Research showed that test must be considered during synthesis to provide good architectural solutions which minimize

area delay cost functions.

Though originally developed separately, OASIC and CATREE can be integrated so that OASIC simultaneously schedules and allocates the architecture and CATREE performs binding (and reallocating) of the architecture for testability.

Part I introduces the motivation and current open problems with high level CAD. Part II provides the necessary background material on architectural synthesis and integer programming. This part includes a definition of problems in both areas and a brief review of previous approaches to solving these problems. Part III outlines the OASIC methodology, models, the solution techniques used, and some synthesized results. Part IV outlines the CATREE methodology, the algorithms and data structures used and some synthesized results. Part V provides a brief discussion and concluding remarks concerning how we will interface with CAD tools of the future.

The book can be used at the senior undergraduate and graduate levels in courses dealing with computer architectures, computer organization, VLSI design, computer-aided design, VLSI digital signal processing, testing, or integer programming. It will be also of value to resesarchers dealing with these topics.

C.H. Gebotys
M.I. Elmasry
Waterloo, Ontario, Canada