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Optimization of LDMOS Transistor in Power Amplifiers for Communication Systems

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This thesis is dedicated to beloved parents, wife, and other family members

Abstract

The emergence of new communication standards has put a key challenge for semiconductor industry to develop *RF* devices that can handle high power and high data rates simultaneously. The *RF* devices play a key role in the design of power amplifiers (PAs), which is considered as a heart of base-station. From economical point of view, a single wideband *RF* power module is more desirable rather than multiple narrowband PAs especially for multi-band and multi-mode operation. Therefore, device modeling has now become much more crucial for such applications. In order to reduce the device design cycle time, the researchers also heavily rely on computer aided design (CAD) tools. With improvement in CAD technology the model extraction has become more accurate and device physical structure optimization can be carried out with less number of iterations.

LDMOS devices have been dominating in the communication field since last decade and are still widely used for PA design and development. This thesis deals with the optimization of *RF*- LDMOS transistor and its evaluation in different PA classes, such as linear, switching, wideband and multi-band applications. For accurate evaluation of *RF*-LDMOS transistor parameters, some techniques are also developed in technology CAD (TCAD) using large signal time domain computational load-pull (CLP) methods.

Initially the *RF*-LDMOS is studied in TCAD for the improved *RF* performance. The physical intrinsic structure of *RF*-LDMOS is provided by Infenion Technologies AG. A reduced surface field (RESURF) of low-doped drain (LDD) region is considered in detail because it plays an important role in *RF*-LDMOS devices to obtain high breakdown voltage (BV_{DS}). But on the other hand, it also reduces the *RF* performance due to high on-resistance (R_{on}). The excess interface state charges at the RESURF region are introduced to reduce the R_{on}, which not only increases the *dc* drain current, but also improve the *RF* performance in terms of power, gain and efficiency. The important achievement is the enhancement in operating frequency up to 4 GHz. In LDD region, the effect of excess interface charges at the RESURF is also compared with dual implanted-layer of p-type and n-type. The comparison revealed that the former provides 43 % reduction in R_{on} with BV_{DS} of 70 V, while the later provides 26 % reduction in R_{on} together with BV_{DS} of 64 - 68 V.

In the second part of my research work, computational load pull (CLP) simulation technique is used in TCAD to extract the impedances of *RF*-LDMOS at different frequencies under large signal operation. Flexible matching is an issue in the design of broadband or multi-band PAs. Optimum impedance of *RF*-LDMOS is extracted at operating frequencies of 1, 2 and 2.5 GHz in class AB PA. After this, CLP simulation technique is further developed in TCAD to study the non-linear behavior of *RF* devices. Through modified CLP technique, non-linear effects inside the transistor structure are studied by conventional two-tone *RF* signals in time domain. This is helpful to detect and understand the phenomena, which can be resolved to improve the device performance. The third order inter-modulation distortion (IMD_3) of *RF*- LDMOS was observed at different power levels. The IMD_3 of −22 dBc is obtained at 1-dB compression point ($P_{1\text{-}dB}$), while at 10 dB back off the value increases to −36 dBc. These results were also verified experimentally by fabricating a linear PA. Similarly, CLP technique is developed further for the analysis of *RF* devices in high efficiency operation by investigating the odd harmonic effects for the design of class-F PA. *RF*-LDMOS can provide a power added efficiency (PAE) of 81.2 % in class-F PA at 1 GHz in TCAD simulations. The results are verified by design and fabrication of class-F PA using large signal model of the similar device in ADS. In fabrication, a PAE of 76 % is achieved.

Keywords: *RF*-LDMOS, power amplifiers, technology CAD, load-pull, non-linear analysis, and switching analysis

Preface

This thesis presents research work performed during my PhD studies from May, 2005 to September, 2010 at Semiconductor Materials Group in the Division of Material Science at the Department of Physics, Chemistry and Biology (IFM), Linköping University, Linköping. Some partial work is done in collaboration with Division of Electronic Devices, Department of Electrical Engineering (ISY), Linköping University, Sweden and Microwave Group of National Engineering and Scientific Commission (NESCOM), Islamabad, Pakistan.

This thesis is mainly composed of two parts. First part covers introduction, *RF*-LDMOS transistor design and its optimization in TCAD and PA characterization. The main motivation behind this work is accurate large signal characterization of *RF*-transistors using Computational Load Pull (CLP) techniques in TCAD and its validation with experimental data.

The second part of the thesis presents our research results which are append in form of published and submitted papers.

Publications included in this Thesis

The following papers are included in this thesis:

1. **Influence of Interface State Charges at the RESURF Region of LDMOS Transistors**

   A. Kashif, T. Johansson, C. Svensson, T. Arnborg, S. Azam and Q. Wahab

   Journal of Solid State Electronics, Vol. 52, no. 7, p 1099-1105, 2008

2. **Reduction in on-resistance of LDMOS transistor for improved RF performance**

   A. Kashif, C. Svensson, and Q. Wahab

   Electro-Chemical Society (ECS) Transations, Vol. 23, no. 1, p 413-420, 2009

3. **Flexible Power Amplifiers Designing from Device to Circuit Level by Computational Load-Pull Simulation Technique in TCAD**

   A. Kashif, Sher Azam, C. Svensson, and Q. Wahab

   Electro-Chemical Society (ECS) Transations, Vol. 14, issue 1, p 233-239, 2008

4. **A TCAD approach for non-linear evaluation of microwave power transistor and its experimental verification by LDMOS**

   Ahsan Ullah Kashif, Christer Svensson, Khizar Hayat, Sher Azam, Nauman Akhter, Muhammad Imran, Qamar-ul Wahab

   Journal of Computational Electronics: Vol. 9, Issue 2, p 79-86, 2010

5. **Switching Behavior of Microwave Power Transistor Studied in TCAD for Switching Class Power Amplifiers and Experimental Verification by LDMOS based Class-F Power Amplifier**

   A. Kashif, S. Azam, K. Hayat, M. Imran, C. Svensson and Q. Wahab

   Submitted to journal publication

6. **A TCAD Approach to Design a Broadband Power Amplifier**

   A. Kashif, C. Svensson, S. Azam, K. Hayat, M. Imran and Q. Wahab

   Submitted to journal publication

Other Publications

The following papers are related with this research work but not included in this thesis:

1. **A New Powerful Envelop Model of Si LD-MOSFET for Device and System Level Simulations for Power Amplifiers**

   T. Arnborg, T. Johansson, A. Kashif, and Q. Wahab

   Proc. of the GigaHertz 2005, Swedish National Symposium Uppsala, Sweden, November 7-8, p 139, 2005

2. **High Power LDMOS Transistor for RF-Amplifiers**

   A. Kashif, C. Svensson and Q. Wahab

   Proc. of IEEE 5th Int. Bhurban Conference on Applied Sciences Technology (IBCAST), Islamabad, Pakistan; January 8-11, p 1-4, 2007

3. **Enhancement in RF Performance of LDMOS Transistor Utilizing Large Signal TCAD Physical Simulation**

   A. Kashif, T. Johansson, C. Svensson , T. Arnborg and Q. Wahab

   Proc. of the conference on RF Measurement Technology (RFMTC-07), Gälve, Sweden September 11-12, 2007

4. **A New Large Signal TCAD Method for Non-Linear Analysis of Microwave Transistor**

   A. Kashif, C. Svensson, S. Azam and Q. Wahab

   Proc. of IEEE International Semiconductor device symposium (ISDRS-07), College Park, MD, USA, 12- 14 December, 2007

5. **Optimization of RF LDMOS transistors by TCAD simulations**

   A. Kashif, T. Johansson, C. Svensson , T. Arnborg and Q. Wahab

   Proc. of the GigaHertz 2008 Conference, Chalmers University, Göteborg, Sweden, p. 85, 5-6 March, 2008

6. **Evaluation of RF-LDMOS for Power Amplifier designing through Optimal Matching in TCAD**

   A. Kashif, C. Svensson, K. Hayat, S. Azam, M. Imran, and Q. Wahab

   Accepted for the Proc. of IEEE 8th Int. Bhurban Conference on Applied Sciences Technology (IBCAST), will be held in January 10-13, 2011, Islamabad, Pakistan

7. Design of 20 Watt High Efficiency Power Amplifier for L Band RADAR , Based on Si-LDMOS

A. Kashif, K. Hayat, S. Azam , N. Akhter, M. Imran, and Q. Wahab

Accepted for the Proc. of IEEE 8th Int. Bhurban Conference on Applied Sciences Technology (IBCAST), will be held in January 10-13, 2011, Islamabad, Pakistan

8. Design & Implementation of 50 W Two-Stage UHF Power Amplifiers Using GaN HEMT

K. Hayat, M.Imran, N.Akhtar, A. Kashif and S.Azam

Accepted for the Proc. of IEEE 8th Int. Bhurban Conference on Applied Sciences Technology (IBCAST), will be held in January 10-13, 2011, Islamabad, Pakistan

9. Broad Band Pre-Amplifier using GaN HEMT on Silicon for Radars & Communication Systems

S. Azam, K. Hayt, A. Kashif, M. Imran and Q. Wahab

Accepted for the Proc. of IEEE 8th Int. Bhurban Conference on Applied Sciences Technology (IBCAST), will be held in January 10-13, 2011, Islamabad, Pakistan

(The listed below publications are belongs to my MS project work related with TCAD approach for the design of RF limiters)

10. Simulations of 4H-SiC PIN and Schottky Diodes for Microwave Limiters

Ahsan- Ullah. Kashif

MS Thesis, Linköping University, 2005, *LiTH-IFM- 05/1441-SE*

11. 4H-SiC PIN and Schottky Diodes for RF Circuits

A. Kashif, R. Jonsson, M. Backström and Q. Wahab

Proc. of RVK 2005 conf, Linköping, Sweden, June 12-14, 2005

12. Limiter Characterization

Toney Nilsson, Rolf Jonsson, A. Kashif, and M. Backström

Tech. report FOI Memo 1072, 2004-12-02, Swedish Defense Research Agency, FOI, Sensor Technology, P.O. Box 1165, SE-581 11 Linköping, Sweden

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Ahsan -Ullah Kashif

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Chapter 1

Introduction

1.1 History of RF- Devices

In *RF* communication system, the power amplifier (PA) is considered a vital component. Its functionality is directly related with the performance of the *RF*-devices. The emerging communication standards demand for high performance *RF*-devices.

Historically, vacuum tubes were used to amplify the signal. First three terminal (triode) vacuum tube was reported by Lee De Forest in 1906 [1]. While the basic principle of first solid state semiconductor device was a surface field effect transistor (FET), patented by Julius Edgar Lilienfeld in 22nd October 1925 [2]. Later on, Dr. Oscar Heil described the possibility of above theoretical FET transistor (British patent in 1935) in a realistic way by controlling the resistance in semiconducting material with an electric field [3]. Bipolar junction transistor (BJT) is considered as first working transistor reported by John Bardeen, Walter Brattain and Walter Shockley at Bell Labs in California in 1947 [1]. Though the theory of the FET transistor was older (~ 20 years) than the BJT, because at that time good semiconductors and its fabrication process was not mature enough to fabricate FET devices. First bipolar transistor was made on germanium, but soon silicon replaced the germanium in 1960 due to ease in fabrication process, by the passivation of SiO_2 layers [4]. Meanwhile the Jack Kilby and Robert Noyce proposed the idea of integrated circuits “integration of multiple devices on a single chip” by photolithography to implement multiple layers with specific properties in 1958. Just two year later (in 1960), D. Kahng and M. M Atalla developed the first working metal oxide semiconductor FET (MOSFET) based on

Shockley's theories [5]. Even after the development of first MOSFET, the commercial MOS devices took one more decade to resolve the fabrication problems.

In the beginning, germanium based BJTs were used in communication systems upto 1 GHz applications [4]. Later on, Si based BJTs enhanced the operation upto 3 GHz. Meanwhile for improved performance, III-V compound semiconductors, GaAs, AlP, InP, InSb, AlGaAs, GaAsP etc., were studied to design the *RF* devices (BJTs, MESFET, HBTs etc.). In 1951, Shockley patented the basic principle of hetro-junction bipolar transistor (HBT) [6]. In 1970's, first GaAs based BJT was developed for high frequency *RF* applications to counter the Si -BJTs limitations. But it had two major problems to cater with. 1) Noise factor due to low mobility of holes in the p-type base of BJTs, and 2) high cost. In 1980, GaAs based metal semiconductor FET (MESFET) devices were developed based on the principle of Schottky diode. It achieved some commercial success as low-noise and medium power transistor and operated upto 12 GHz, but was still costly. Today such devices are operating upto 50 GHz [7].

Before1980, the wireless communication system was mostly used only for broadcasting radio, TV and radars communication both for commercial and military applications rather than point –to- point communication. In 1990, the cellular communication system brought a new start up of technologies in wireless communication system by introducing transfer of data and voice conversation together at high operating frequencies. Hence, we can say that cellular communication systems enhanced the production and development of the solid state devices rapidly to meet the low cost goals with higher performance.

In 1996, laterally diffused metal oxide field effect (LDMOS) transistor replaced the silicon BJTs [8] due to advantageous properties such as, low inter-modulation, higher gain and reduced thermal effect [9]. In LDMOS devices, its substrate provides large area contact to dissipate heat exclusively compare to other devices and this also resulting only two terminals (gate and drain) left on top, suitable to reduce the effect of source inductance enabling the transmission lines easier. This is the reason that LDMOS devices have a dominant role in the communication field (low frequency applications upto 4 GHz). They are used in *RF* amplifier for more than a decade in various systems e.g. HF, UHF and VHF, cellular and WiMAX base stations [10] – [16].

In recent years, wideband gap (WBG) semiconductors, SiC and GaN, are promising semiconductors for future *RF* applications due to their physical properties like high breakdown electric field, and thermal conductivity etc. [17]-[22]. Such properties of WBG semiconductors are helpful to reduce the size of devices and beneficial for portable military applications, where the reduced size is also important along with high performance. Though GaN devices provide 10 times higher power density as compare to Si-LDMOS devices, but cost factor is not comparable. Secondly, high power density is not beneficial until the package of the device can manage the thermal management properly. Hence GaN devices are mainly focused in the communication market at those frequencies which are not handled by Si-LDMOS devices. Nowadays, GaN devices are grown on Si wafers to reduce the cost for commercial aspect, but there is a compromise on thermal conductivity. Table -1.1 [23] shows comparison among physical properties of the different semiconductors. It shows that future *RF* devices can be designed on III- V semiconductors, such as GaAs and GaN, but these devices are not comparable with LDMOS devices below 4 GHz, due to low fabrication cost.

Table- 1.1 ***Comparison among physical properties of semiconductors for RF applications***

Physical properties	**SiGe**	**Si**	**GaAs**	**InP**	**4H-SiC**	**GaN**
Band Gap (eV)	0.84- 1.1	1.1	1.42	1.35	3.26	3.28
Mobility (cm^2/ Vs)	1400-4315	1400	8500	5400	900	2000
Critical Electric Field (MV/cm)	0.3	0.3	0.4	0.5	3.0	5.0
Electron thermal velocity (10^7 cm/s)	2.4	2.3	4.4	3.9	1.9	2.1
Thermal conductivity (W/cm.K)	0.8-1.3	1.5	0.5	0.7	3.7	1.3
Transistor Type	BJTs HBTs MOSFET	BJTs MOSFET HBTs	MESFETs HEMT HBTs	MESFETs HEMTs HBTs	MESFETs HEMTs	MESFETs HEMTs
Cost per mass fabrication	High	low	high	v. high	v. high	v. high

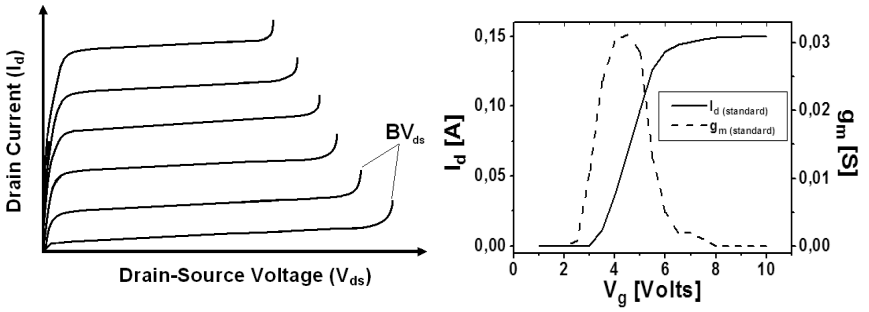
1.2 Figure of Merit for RF Transistor Design

Figure of merit (FoM) is a straightforward way to study the performance of a transistor. It provides the performance comparison of different devices from different manufacturers having same technology. It is also helpful to compare the technologies based on different semiconductors (e.g. Si, GaAs and GaN etc) as well as devices (e.g. MOSFET, LDMOS, MESFET, HEMTs and HBT etc.). FoM is derived by *dc*, small-signal and large signal analysis to analyze the device accordingly to the *RF* applications.

DC analysis is taken by input (gate) and output (drain) current-voltage (I-V) characteristics as shown in Fig. 1, *dc* analysis provides the drain -source breakdown voltage (BV_{DS}), on-resistance (R_{on}), knee voltage (V_k) and transconductance (g_m). The BV_{DS} is shown by circle in Fig. 1.1(a), while R_{on} is calculated from the slop of the linear part of the drain current-voltage (I-V) characteristics (Fig. 1.1(a)). The knee voltage (V_k) of the FET transistor is an important factor to improve the drain efficiency of the device together with $R_{on.}$ Because small V_k provides large swing of *RF* voltage at the given drain bias.

The transconductance (g_m) of MOSFET in a saturation region is defined by following equation [24];

$$g_m = \frac{\partial I_{D(sat)}}{\partial V_G} = \frac{Z.C_{ox.}\mu_n}{L}(V_G - V_T) \qquad (1.1)$$



(a) **(b)**

Fig. 1.1 I-V characteristics of LDMOS transistor at (a) Output (drain) b) input (gate).

Where C_{ox} is the gate capacitance, μ_n is the channel mobility and Z, L represents the width and length of the gate respectively. Fig. 1.1(b) shows the g_m curve of an LDMOS transistor which is defined by above equation $(\partial I_D/\partial V_G)$. (Note: In LDMOS devices, g_m curve is reduced in the compression region due to low doped drain (LDD) region [25].)

In *RF* – transistor design, the frequency of operation is a key feature which depends on transition frequency (f_T) and maximum oscillation frequency (f_{max}), extracted through small- signal analysis. The f_T provides how rapidly a transistor can transfer charge in its channel from gate to drain. Therefore the value of f_T depends on gate –source capacitance (C_{gs}) and transconductance (g_m) written as following;

$$f_T = \frac{g_m}{2.\pi.C_{gs}} \qquad (1.2)$$

And f_{max} is defined by unilateral gain (U) of the transistor [26]:

$$U = \left(\frac{f_{max}}{f} \right)^2 \qquad (1.3)$$

$$f_{max} = \frac{f_T}{2} \sqrt{\frac{R_{out}}{R_{in}}} \qquad (1.4)$$

In principle f_{max} gives the intrinsic switching speed which depends on high output and input resistance (R_{in}). The R_{out} can be approximated by the slop of the drain current in saturation region of the transistor from *dc* I-V characteristics, while R_{in} is calculated from the real part of the input Y-parameter (Y_{11}).

The most important FoM in *RF*- transistor design is its accurate large-signal analysis for optimal bias point selection, which can affect the performance of PAs. Therefore, PA designers mainly focus on large signal analysis of the *RF* -transistor and try to extract an accurate equivalent circuit model. Load -pull (LP) measurement is common to extract the parameters of

the transistor for PA design in terms of *RF*-output power (P_{out}), power gain (G), drain efficiency (η_d), power added efficiency (PAE) and the distortion behaviors etc. [7].

1.3 Future trends of RF-Technology

RF-technology has a major share in wireless communication market. Today, various commercial communication standards are in use. For future aspect, there is a need to operate several *RF* applications with signal solution having low cost, smaller in size and high market potential. Therefore, the demand of *RF*- devices are continuously increasing from the last decade and it will remain in future as well.

Nowadays, PA designers face new challenges due to rapid enhancement in the cellular communication technology, for example need to fabricate good *RF* devices with higher power levels and operate at higher frequencies but with low cost as well. Thus the future trend demands an accurate characterization of *RF* devices both at circuit and device level to enhance the system performance at an optimal condition in a reduced time. There is also a need to couple the *RF* characterization both at circuit and device level in order to utilize the active device adequately.

Technology computer aided design (TCAD) is a versatile tool to design the semiconductor devices prior to fabrication and its optimization [27]-[28]. TCAD software is based on physical models to describe the active device in terms of the carrier transport equations together with geometrical limitations. Physical models need larger computational resources compare to the equivalent circuit models due to a huge set of the transport equations, but provides a valuable insight view of the device and characteristics to be closely related to the device structure [29]. Today computers having faster clock speed and large capability of data storage in memory tracks. So, it is possible for device designers to study the device's operation before fabrication in a reduced time. This may also reduce the number of iterations required for an optimized design, hence saving the cost. Therefore, currently PA designers are focusing on TCAD approaches for the large signal analysis of *RF*-transistor as an alternate method and its capability has already been demonstrated on different devices for different communication systems [29-31].

In this research work, our emphasis is to establish new TCAD methods that could be useful for the characterization of physical structure of *RF*-power transistor in PAs design.

1.4 About Thesis

This research work is composed of two parts. First part covers *RF*-LDMOS transistor design, to enhance the *RF* performance in terms of *RF* power and operating frequency [***Paper-I***]. The optimization of *RF*-LDMOS is studied in two different techniques; i) surface doping technique and ii) excess interface charges technique at the RESURF (reduce surface field) of low doped drain (LDD) region in order to compare the most important trade - off R_{on} and $BV_{DS,}$ which is also important factor for achieving good *RF* performance [***Paper-II***].

The second part of the thesis is about large signal characterization of *RF*-transistors using computational load-pull (CLP) techniques in TCAD for design and development of PAs. Large signal time domain CLP technique is a useful method to extract the large signal parameters as well as to identify the performance-killing phenomenon to predict the transistor's performance in a real circuit context [31]. Through CLP technique, both input and output impedances can be tuned at various frequencies which are helpful in the design and development of broadband / flexible PAs [***Paper-III & VI***]. The CLP simulation technique is further developed in TCAD to study the non-linear behavior of *RF* devices. Through modified CLP technique, non-linear effects inside the transistor structure are studied by conventional two-tone *RF* signals in time domain. This is helpful to detect and understand the phenomena, which can be resolved to improve the device performance [***Paper-IV***]. The demand of transferring the high data rate increases in present and future communication systems. Therefore, CLP technique is extended to study the switching behavior of *RF*- transistor for high efficiency PAs e.g. class F mode [***Paper-V***]. All these techniques are useful for PAs and to characterize the *RF*- transistor with large signal operation adequately, which is helpful to reduce the design time of cycle important for rapid enhancement from industry point of view.

1.5 *References*

[1] Frank Ellinger, *Radio Frequency Integrated circuits and Technologies*, Springer, 2007

[2] US patent 1745175 Lilienfeld "Method and apparatus for controlling electric current" *first filing in Canada,* 1925

[3] GB patent 439457 Oskar Heil: "Improvements in or relating to electrical amplifiers and other control arrangements and devices" *first filed in Germany,* 1934

[4] H. F. Cooke, "Microwave Transistors: Theory and Design," *Proceedings of the IEEE*, v 59, n 8, p 1163-81, 1971

[5] D. Kahng, and M. M. Atalla, "Silicon dioxide field surface devices," *Device Research Conf. IEEE*, Pittsburgh, 1960

[6] U.S. patent 2569347 W. Shockely, 1951

[7] Peter Aaen, Jaime Pl´a and John Wood, "Modeling and characterization of RF and microwave Power FETs", *Cambridge University Press 2007*, ISBN-13 978-0-521-87066-5

[8] A. Wood, C. Dragon, and W. Burger, "High performance silicon LDMOS technology for 2 GHz RF power amplifier applications" *Int. Electron Devices Meeting.(IEDM) Tech. Dig. (Cat. No.96CH35961)*, p 87-90, 1996

[9] J. J. Bouny, "Advantages of LDMOS in high power linear amplification," *Microwave Engineering Europe*, p 37–40, 1996

[10] A. Wood, "Silicon LDMOS technology for a new generation of cellular and PCN RF power amplifier applications" *Conf. Proc. of Microwave and Communications Technologies*, p 334-9, 1997

[11] *330 W LDMOS power transistor for L-band radar applications*, Microwave Journal, Euro-Global Edition, v 51, n 8, p 58 - 9, 2008

[12] G. Vacca, " Power amplifiers for microwaves and RF applications with LDMOS transistors" *Microwave Journal*, v 49, n 6, p 98-102, 2006

[13] S. De Meyer, and H. Beaulaton, " A 210 W LDMOS RF power transistor for 2.2 GHz cellular applications with enabling features for LTE base stations" , *Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits*, p 4, 2008

[14] G. Formicone, F. Boueri, J. Burger, W. Cheng, Y. Kim, and J. Titizian, "Analysis of bias effects on VSWR ruggedness in RF LDMOS for avionics applications" *European Microwave Integrated Circuit Conference (EuMIC)*, p 28-31, 2008

[15] *LDMOS RFICs simplify WiMAX base station design*, Microwave Journal, Euro-Global Edition, v 50, n 11, p 32- 34, 2007

[16] G. Ma, Chen Qiang, O. Tornblad, Wei Tao, C.Ahrens, and R. Gerlach, "High frequency power LDMOS technologies for base station applications status, potential, and benchmarking" *Int. Electron Devices Meeting 2005 (IEEE Cat. No.05CH37703C)*, p 4, 2005

[17] Chu Rongming, Shen Likun, N. Fichtenbaum, D. Brown, Chen Zhen, S. Keller, S.P. DenBaars, and U.K. Mishra, "V-gate GaN HEMTs for X-band power applications" *IEEE Electron Device Letters*, v 29, n 9, p 974-6, 2008

[18] R. Szweda, "HEMT materials and devices" *III-Vs Review*, v 16, n 3, p 36-39, 2003

[19] A. Agarwal, J. Haley, H. Bartlow, B. McCalpin, C. Capell, and John W. Palmour, "2100 W at 425 MHz with SiC RF power BJTs" *Device Research Conference – DRC Conf. Dig.*, p 189-190, 2005

[20] C. Brylinski, "Silicon carbide for microwave power applications" *Diamond and Related Materials*, v 6, n 10, p 1405-13, 1997

[21] F. Temcamani, P. Pouvil, O. Noblanc, C. Brylinski, P. Bannelier, B. Darges, and J.P. Prigent, "Silicon carbide MESFETs performances and application in broadcast power amplifiers" *IEEE Int. Microwave Symp. (MTT-S) Dig. (Cat. No.01CH37157)*, v 2, p 641-4, 2001

[22] F. Temcamani, P. Pouvil, O. Noblanc, C. Brylinski, B. Darges, F. Villard, and J. P. Prigent, "Silicon Carbide amplifiers for communication applications" *30th Conf. Proc. of European Microwave Conference 2000*, v 3, p 144-6, 2000

[23] http://www.ioffe.rssi.ru/SVA/NSM/Semicond/

[24] Ben G. Streetman, and S. Banerjee, *Solid State Electronic Devices*, Pearson Education Inc., ISBN 81-7808-691-3

[25] F. Rotella, G. Ma, Z. Yu, and R. W. Duttton, "Modeling, analysis and design of RF LDMOS devices using harmonic balance device simulation," *IEEE Trans. Microwave Theory and Tech.*, v 48, n 6, p 991-99, 2000

[26] G. D. Vendelin, A. M. Pavio, and U. L. Rohde, *Microwave Circuit Design*. New York, NY: John Wiley & Sons, 1990

[27] *Sentaurus Workbench Visualization*, version X-2005.10, Synopsys, Inc.

[28] *Atlas User's Manual, Device Simulation Software*, vol. I and II, Silvaco International, 2000

[29] C.M. Snowden, "Nonlinear modelling of power FETs and HBTs" *Proc. of 3rd Int. Workshop on Integrated Nonlinear Microwave and Millimeter wave Circuits (Cat. No.94TH8020)*, p 11-25, 1994

[30] G. H. Loechelt and P. A. Blakey, "A computational load-pull system for evaluating RF and microwave power amplifier technologies," *IEEE MTT-S Int. Microwave Symp. Dig.*, p 465–468, 2000

[31] R. Jonsson, Q. Wahab, S. Rudner, and C. Svensson, "Computational load pull simulations of SiC microwave power transistors," *J. Solid State Electronics*, v 4, p 1921-5, 2003

Chapter 2

Technology Computer Aided Design (TCAD)

TCAD is a branch of the electronic device and circuit design automation to model the semiconductor device performance before fabrication. The concept of TCAD was first introduced for the physics-oriented challenges of bipolar transistor in the beginning of 1970s for process control issues through the modeling approaches in one- and two-dimensional solutions [1]. The TCAD standards initiated by S. G. Duvall in 1988 [2]. Now TCAD tools are playing key roles in the development of new type of semiconductor technology. It provides technology development in especially, for deep sub-micrometer devices to see insight during device operation, what is comparable to the measurement of device after fabrication. In this way, the optimization of device is much easier with less financial and manpower resources required by the no. of experiments. Moreover it is also helpful to speed-up the technology for integration [3]. Now TCAD is considered a versatile tool for the development of semiconductor technology and provides realistic process steps for the fabrication, such as, diffusion, ion implantation, etching, metallization as well as explores the electrical properties based on semiconductor physics models.

The aim of TCAD simulation is to obtain an accurate prediction of device performance with respect to physical parameters, such as the thickness and doping concentrations of different layers and regions, and stress distribution in the device geometry [4-5]. A designed device, e.g. FET, is represented in TCAD device simulator as a “virtual” device whose physical properties are defined by grid or mesh. The simulations in 2-dimensions with defined boundary conditions are performed to analyze the basic behavior of the device carefully from intrinsic to final stage including parasitic effects before fabrication. The hydro-thermal model in TCAD can

also be used to obtain self heating effect due to current flow in the device while the transient analysis provides the small and large signal analysis.

2.1 Device Simulation

TCAD modeling is an art to study the electrical behavior of virtual designed devices by critical analysis and detailed understanding based on computer simulations with device engineering, process development and circuit design. Device simulation helps to realize the behavior in an obvious way and also show the physical limitations at process and manufacturing level. When the device structure is designed in TCAD, either in 2-D structure editor (MDRAW in Synopsys) or process simulator, the device simulator (e.g. DESSIS is in Senturus TCAD) solves the Poisson equations by coupled systems of partial differential equations (PDEs) under selected boundary conditions.

The grid file provides the description of the various regions regarding material type, doping concentrations and the location of electrical contact to the device simulator for the analysis (*dc*, AC analysis, Noise, transient and large signal cyclic analysis) on the basis of device physics in cylindrical geometries, drift diffusion, thermodynamics, full band Monte Carlo, mobility models [6]. In device simulation, the mesh of the device is a part of the design to create the nodes at different regions for electrical measurement. The dense mesh is always required at regions of high current density and electric field for obtaining accurate results close to experiment. In case of LDMOS the channel and low doped drift region need comparatively dense grid than other regions. A typical design flow of the device simulator is shown in Fig. 2.1.

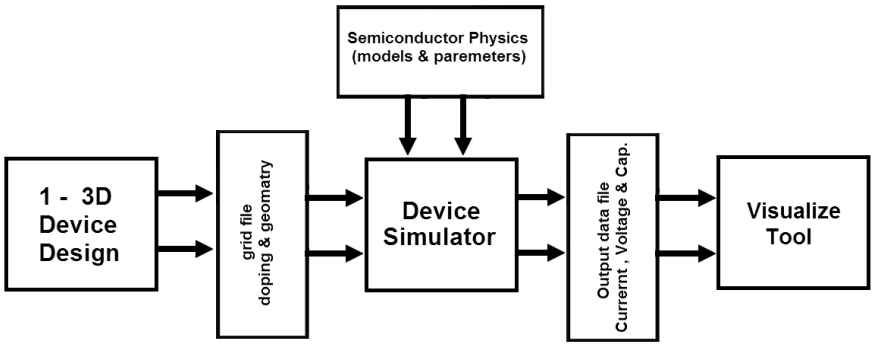


***Fig. 2.1** Design flow for device simulation*

A mixed device and circuit level simulation in TCAD provides a suitable solution to study the performance in a real circuit perspective. In this way the circuit stresses on the transistor can be studied in detail and also helpful to adjust the critical issues like packaging and related device parasitic.

2.2 TCAD Advantages over other CAD Tools

TCAD simulations have a significant role to reduce the design time for the technology development. To develop the devices and circuits precisely, its friendly graphical user interface (GUI) provides a reasonable information and understanding to device designers, semiconductor researchers and process engineers. This is the main reason; nowadays TCAD tool has a dominant place in semiconductor industry for technology development. Its main advantages are;

- Provides information about the wafer state such as topography, dopant profile and current density for the optimal device development which is not clear in other CAD tool (mostly defining the layout only).
- On the basis of wafer state a desired device can be processed satisfactorily with the help of process simulator and also ensures the design reliability. Thus, the time and cost in technology development reduces with practical approach.
- TCAD provides a simplified method to describe the circuit behavior based on complex device equations into an analytical form [7].
- Mixed mode TCAD simulate the device with spice circuit models for better reliability, because the effects of electro-migration, ESD (electro-static discharge), hot carrier, oxide breakdown and latch-up phenomena which is not possible to study in other CAD tool.
- With the help of TCAD, the circuit designers can investigate the feasibility and impact of process modification to increase the performance of the technology.

2.3 TCAD Applications in Different Areas

The prediction of future trends and the direction of technology is always a hard proposal, because in technology development the rate of change devices depends on the high performance in compact size. But it is not easy to control the device scaling issues properly according to technology road-map defined by Moore's law. Sometimes theoretical approach provides a

pre-defined concept about the device design but the fabrication has its own limitations and may need more time for proper implementation (e.g. the concept of FET device came in 1925, but its practical implementation was done in 1958). Now the use of TCAD tool provides a better approach for both device design and its fabrication that, what is the next technology or transistor demand and how it will be processed in a better way, such as its yield and reliability etc. Some examples about the role of TCAD in different areas are;

- Nowadays, MOS technology having dimensions about 45 nm is in production while 32 nm or below are in process. TCAD provides a detailed statistics of dopant distributions with conventional methods under different growth conditions, and also provide the alternate doping methods and technologies for junction formations to overcome the problems of process such as shallow junctions, controlling thresholds, and compound problem of gate stack scaling such as spacer. Now simulations are focused on nano-device scale modelling e.g. 10 nm devices [8].
- As semiconductor devices are approaching at atomic scales, therefore devices can also have dimensions comparable to many biological microstructures. TCAD has potential to give an overview to solve the challenges in modeling of electronics with the domains of biotechnology. Recently, biosensors in molecular identification and quantification applications were studied in TCAD [9]-[10].
- In recent years, the use of wireless communication increases gradually in different areas such as broadcasting, local area networks, cellular telephone systems, ultra-wideband and low cost low power radios, wide area wireless data services and portable military applications etc. All these applications directly or indirectly depend on the functionality of the *RFICs (*such as transreceiver, power amplifiers) to operate with multi-bands and multi-standards as well as need compact solution. For *RFICs*, the designers struggle to improve the functionality of *RF*-transistors with different ways such as designing of *RF* devices with new semiconductors SiGe, SiC, GaN, AlGaN, and ZnO or by implementing the new architectures such as envelope tracking, and envelope elimination restoration. TCAD tool provide a reasonable platform to study the performance of *RF*- transistor in both way by material [11-13] as well as architectures with the help of some computational techniques at device level [14]-[17].

TCAD uses finite element method or matrices to solve the semiconductors physics equations together with virtual device structure. It takes a lot of computational resources and time as compare to other CAD tools. To overcome this drawback, the computational techniques are also developed to characterize the *RF*-device properly prior to fabrication at device level as mentioned in paper-I, III, IV, V, and VI. Through computational technique in TCAD, it is possible to predict the device performance adequately for PA design. Thus, it provides an initial ground work and can be able to study the performance killing factors of the transistor with parasitic effects. The detailed discussion about how TCAD approach is beneficial in PA design for *RF* –characterization is discussed in ***Chapter 4*.**

2.4 References

[1] http://en.wikipedia.org/wiki/Technology_CAD

[2] S. G. Duvall, "An interchange format for process and device simulation," *IEEE Trans. on CAD*, v CAD-7, p 741-54, 1988

[3] Robert W. Dutton and A. J. Strojwas, "Perspectives on technology and technology-driven CAD", *IEEE trans. on CAD of integrated circuit and systems*, v 19, n 12, p 1544-60, 2000

[4] Sentaurus TCAD Workbench ver. X-2005.10. Copyright (C) 1994-2005 Synopsys

[5] Athena User's manual, 2D Process Simulation Software, *Silvaco International*, Feb.2000. [http://www.engr.sjsu.edu/~dparent/Silvaco/athena.pdf]

[6] Dessis Manual of Sentaurus TCAD Workbench

[7] G. Chin, W. Dietrich. Jr. D. Boning, A. Wong, N. Neureuther, R.W. Dutton," Linking TCAD to EDA – benefits and issues" , *IEEE proc. Design Automation Conference*, p 573-78, 1991

[8] http://www-tcad.stanford.edu/index.html

[9] Arjang Hassibi, Yang Liu, and Robert W. Dutton, "Progress in Biosensor and Bioelectronics Simulations: new applications for TCAD," *IEEE proc. of SISPAD*, p 1 - 4, 2008

[10] Liu Yang, K. Lilja, C. Heitzinger, and Robert W. Dutton, "Overcoming the screening –induced performance limits of nanowire biosensors: a simulation study on the electro-diffusion flow", *IEEE Int. Elec. Dev. Meet. (IEDM) Tech. Dig.*, p 4, 2008

[11] W. Liu, C.M. Zetterling, M. Ostling , "Thermal-issues for design of high power SiC MESFETs", *Proc. of IEEE CPMT Conference on High Density Microsystem Design and Packaging and Component Failure Analysis (HDP '04)*, p 331-5, 2004

[12] Peng Cheng, Curtis M. Grens, Aravind Appaswamy, Partha S. Chakraborty, John D. Cressler, "Modeling mixed-mode DC and RF stress in SiGe HBT power amplifiers", *Proc. of IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, p 133-36, 2008

[13] S.K. Jones, S.P. Marsh, W.A. Phillips, "TCAD evaluation of AlGaN/GaN device performance for high power applications", *Workshop on High Performance Electron Devices for Microwave and Optoelectronic Applications, EDMO*, p 65-70, 1999

[14] R. Jonsson, Q. wahab, S. Runder, and C. Svensson "Computational load-pull simulation of SiC microwave power transistor" , Journal of Solid State Electronics, v 47, p 1921 - 6, 2003

[15] O. Bengtsson, L. Vestling, J. Olsson, "A computational load-pull method for TCAD optimization of RF-power transistors in bias-modulation applications", *Proc. of European Microwave Integrated Circuit Conference (EuMIC)*, p 222-5, 2008

[16] O. Bengtsson, L. Vestling, "A method for device intermodulation analysis from 2D, TCAD simulations using a time-domain waveform approach", *Proc.of the 36th European Microwave Conference* , p 3 , 2006

[17] Sher Azam, C. Svensson, Q. Wahab, “Pulse input Class-C power amplifier response of SiC MESFET using physical transistor structure in TCAD” *Journal Solid-State Electronics*, v 52, n 5, p 740- 44, 2008

Chapter 3

Power Amplifiers (PAs)

High performance power amplifiers (PAs) are always demanding in wireless communication systems with superior linearity and high efficiency, both for narrow and broadband applications. In PA design, the power performance is directly depending on the *RF* power-transistor behavior, which is the key component [1]. Therefore, proper selection of the active transistor is very important, this means, device should have low on-resistance, high output current, higher drain-source breakdown voltage, low harmonics behavior together with desired operating frequency and bandwidth. For optimal PA design, the best approach is to study the real behavior of *RF*-transistor from device to circuit level. Usually, *RF*-designers built an equivalent circuit model of the active transistor, based on small and large signal. For example high gain and low noise amplifiers can easily be designed on the basis of small signal S-parameters because are utilized in the receiver where the available signal level is low. The large signal analysis is performed in power amplifiers because it is used in transmitters where high RF power is desired. It is therefore, challenging to predict an accurate large signal model due to several variables with respect to input *RF* signal [2].

The main goal of small and large signal analysis is similar; to obtain proper impedances both at the input and output ports of device under test (DUT). The difference is only in the impedances measurement techniques. Current–Voltage (I-V) characteristics are sufficient in case of small signal analysis because the signal level is small and close to quiescent or bias points, while in the case of large signal analysis, techniques, such as passive or active load-pull and two ports large signal S-parameters characterization etc are required [3].

3.1 PA Design Considerations

RF-transistors play a key role in PA design; therefore are especially designed to deliver the desired *RF* output power, high gain and efficiency. For this purpose, optimization of various manufacturing process and package parameters has vital role. Normally, high *RF* output power is achieved by parallel placing of many transistors (or gate fingers) on a single chip/die and in a package which is often a gold plate heat sink to remove the generated heat from chip.

RF - LDMOS transistor is used in this research work, widely utilized in the following telecommunication bands (e.g. GSM, GSM- PCS, and WLAN 802.11b applications) as shown in Fig. 3.1.

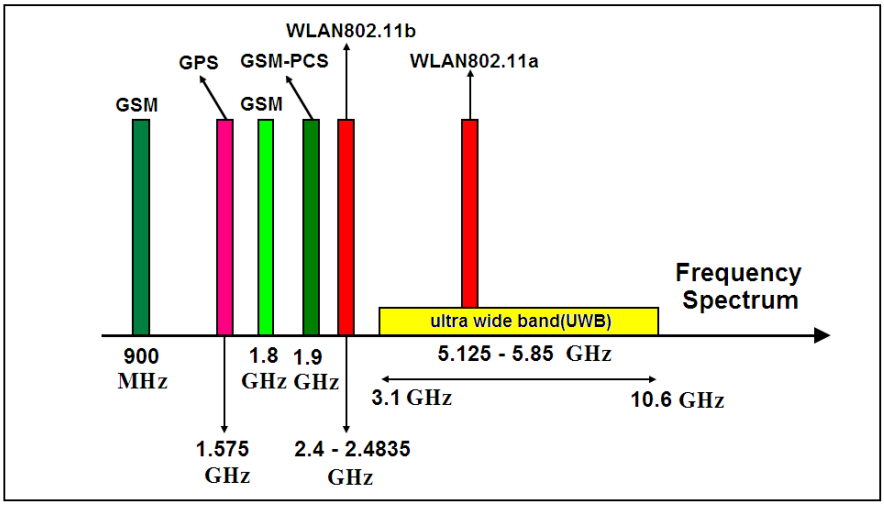


***Fig. 3.1** Frequency spectrums with communication bands [4]*

A single stage amplifier setup is shown in Fig. 3.2 in which amplifier configuration with transistor is represented by a box at the centre. The input (IMN) and output matching networks (OMN) are parts of the amplifier to reduce unwanted reflections. P_{in} is input *RF* power to the amplifier while P_L is the *RF* power to the load. Γ_{in} and Γ_{out} are the reflection coefficients at the input and output. Similarly Γ_S and Γ_L are the source and load reflection coefficients respectively [5]. *dc* biasing network is used to bias the transistor of an amplifier for a specific performance and class of operation.

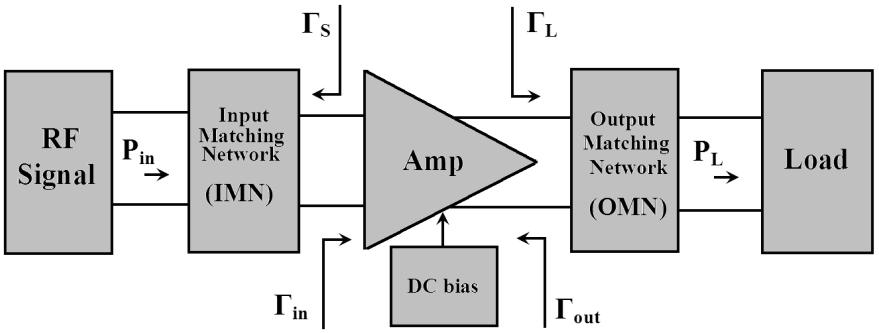


***Fig. 3.2** A single stage amplifier set-up [5]*

Usually 28 V *d*c supply is used for the base station PAs. (Note: High power rating of LDMOS transistors will be available soon for the base-station applications with 50V *dc* power supply upto 1 kW handling power claimed by both NXP and FreeScale [6] - [7]). In normal telecommunication system, IMN and OMN are equal to the characteristics impedances (normally 50 Ω). The following characteristics are important in PA design;

3.1.1 Output Power

RF- transistor is the most important part, because high output power is always important to transmit the signal to a long distance. In this way, the number of mobile telephone base stations is reduced in numbers, and this is one example since mobile telephone is one of the biggest market in wireless communication system. This is the reason; why designers are forced to use the low cost transistor in PA design with higher *RF* output power. LDMOS devices provide power in the transmitter for GSM base station in the range 320 – 640 W [8].

a) Output Power at 1-dB compression point

Compression point 1-dB is referred to the point in output power curve of an amplifier when the power gain of the amplifier is reduced by 1-dB. This point is often used to define the output power performance of an amplifier. The gain is constant in the linear region where the input signal is small to medium. The saturated power at which the power gain is 1 dB less from small signal regime is called 1-dB compression point [9], this point is illustrated in Fig. 3.3 [**Paper –VI**].

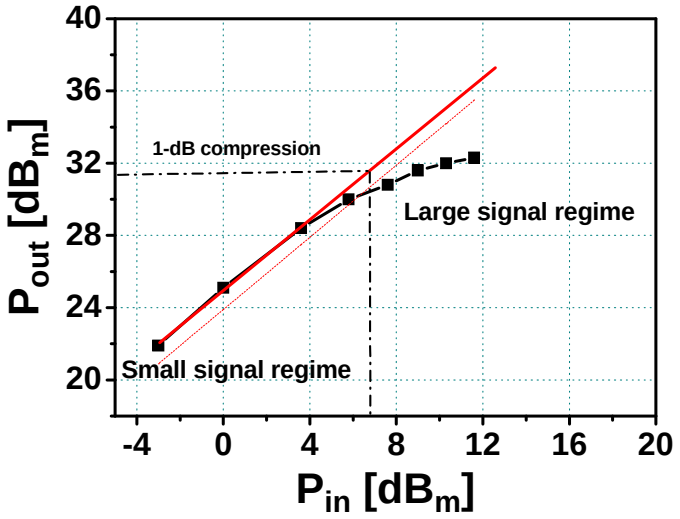


***Fig. 3.3** Power sweep to study the 1- dB compression point of PA*

3.1.2 Power Gain (G)

There are various definitions of the power gain such as transducer power gain, unilateral power gain and operating power gain etc. These definitions are used to understand the critical phenomena of an amplifier functions. Usually the ***Power gain or Operating power gain (G)*** is mostly considered in the designing of power amplifier, which defines the ratio of the power delivered to the load and the power supplied to the amplifier.

$$G = \frac{\text{power deliverd to the load}}{\text{power supplied to the amplifer}} = \frac{P_L}{P_{in}} \qquad (3.1)$$

For optimal performance of PAs, constant gain is important with large input signal span. 18-20 dB of power gain at 2 GHz as reported for a modern 100 W Si- LDMOS [10].

3.1.3 Efficiency

The ability to convert the *dc* power into *RF* output power is called the efficiency of the transistor or amplifier. There are two main definitions widely used in PA design; drain efficiency (η_D) and power added efficiency (PAE).

Drain Efficiency (η_D) is defined by the ratio of the *RF* output power to *dc* input power [11]

$$\eta_{\mathrm{D}} = \frac{P_{RF(out)}}{P_{DC}} \qquad (3.2)$$

Where $P_{DC} = V_{dc} * I_{dc}$

Power Added Efficiency (PAE) is a useful term to define the efficiency with net boost given to a signal that passes through an amplifying stage. This is an important parameter in PA design system where *dc* power is limited or overall heat dissipation is of prime concern [9]. PAE is defined by:

$$PAE = \frac{P_{RF(out)} - P_{in}}{P_{DC}} \qquad (3.3)$$

PAE and η_{D} is almost same. From eq. (3.2) and (3.3), the efficiency is directly affected from biasing of the transistor. Theoretically, the efficiency increases with reduced conduction angle (Θ). For example, class A can have a maximum efficiency upto 50 % (Θ is 360^0), while class AB (Θ is above 180^0) and C (Θ is 0^0) has theoretical values upto 78.5 and 100 % respectively [11].

3.1.4 Linearity

Linearity is an important parameter in PA design; especially in case of new standards in communication systems. Since by definition, transistor is a non-linear device, therefore non-linear behavior is not possible to remove completely. Thus, an amplifier works linearly upto a certain level of input signal. After this PA operation goes in a compression region and generates harmonic signals. An additional filter circuit is required to dump such harmonic signals, but closely spaced signals are not easy to filter out directly and may cause distortion, referred as, intermodulation distortion (IMD).

The compression point shown in Fig. 3.3 gives a rough assistance about the maximum available linear *RF* output power. For more precision normally a multi-tone input signals are applied to study the non-linear behavior or IMD products relative to considering the reference point, typically measured by two-tone test. Two closely tones f_1 and f_2 with narrow

frequency spacing are simultaneously applied. Due to PA nonlinearity, IMD side bands will appear at the output signal as illustrated in Fig. 3.4.

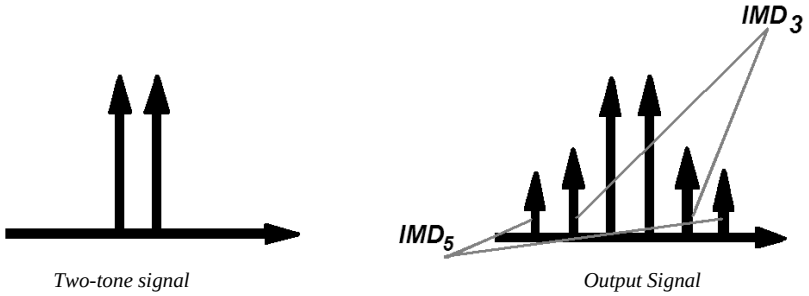


***Fig 3.4** Two-tone power spectrums with IMD_3 and IMD_5 [16]*

In practice, more side bands often appear at the both sides (e.g. 2nd, 3rd, 5th, 7th and so on), but normally the designers consider 2nd and 3rd IMDs only, because it lies inside the bandwidth of the channel and not easy to remove or filtered [8], [12]. Fig. 3.5 shows 3rd order intercept point based on an idealized two - tone measurement.

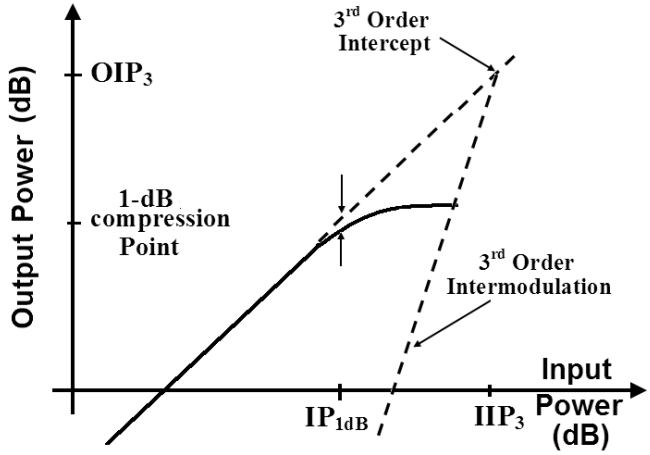


***Fig. 3.5** Illustration of two-tone test results, 3rd order input/ output intercepts point (IIP_3/ OIP_3) together with IMD product [16]*

The designers are trying to suppress IMD levels upto -70 dBc to meet high demand of multi–carrier mobile telephones by increasing the linearity.

This is a main reason, linearity received intense attention. To my knowledge, the maximum reported value of IMD in LDMOS is around -57 to -60 dBc for WCDMA carrier signal, $\pm$ 10MHz offset frequency at 2.14 GHz [14].

3.1.5 Stability

The amplifier can become unstable due to the combination of the different load and source impedances. The cause of instability is the gain to drain coupling, and layout of the amplifier. To avoid the expansion of inherent device feedback capacitances, the designer embedded 50 Ω value for source and load to stabilize the transistor operation. Otherwise there is possibility that the PA can start oscillating [11].

The stability is usually defined into two types; unconditional and conditional. If $|\Gamma_{in}|$ and $|\Gamma_{out}| < 1$ for all passive source and load, then the circuit will be ***Unconditionally Stable,*** while if $|\Gamma_{in}|$ and $|\Gamma_{out}| > 1$ for a certain range of passive source and load is called ***Conditionally Stable*** [15]**.**

The stability is also defined by the stability factor (K), for example if

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta^2|}{2|S_{12}.S_{21}|} \succ 1 \qquad (3.4)$$

If $|\Delta| \prec 1$ the amplifier will be unconditionally stable, (Where $\Delta = S_{11}S_{22} - S_{12}S_{21}$).

3.2 PA Classification

PAs are mainly divided into two parts; linear PAs (e.g. class-A, B and AB) and non-linear or switching PAs (class-C, D, E and F so on). This section described briefly about general classification of PAs along with their merits and demerits.

3.2.1 Linear PAs (Class A, B and AB)

Class- A PA operates for a certain desirable (high) linearity at the expense of efficiency across the full input and output range. To achieve the full period, Q-point is adjusted at mid of the maximum drain current (I_d).

In class-A, peak-to–peak sinusoidal voltage is around $2V_{DD}$. The maximum drain efficiency (η_D) will become 50 %. In practical design, it will be less than 40 % [16].

Class-A provides linearity at the expense of efficiency and relatively large device stress. Normally, it is used in low–level applications or as early stage of a cascade design.

In ***class-B***, the bias point (Q-point) is adjusted to the output of active device at every half cycle (50 %) to enhance the efficiency. The drain current (i_d) is sinusoidal for the first half cycle and zero for the other half cycle. Output power is approximately same as class-A PA operation while *dc* power will be $2V_{DD}^2 / \Pi R$. Hence the efficiency is around $\pi/4$ = 78.5 %. In practice, it is not possible to achieve the exact conduction angle (Θ) of 180^0. Therefore, class-B is considered as theoretical and its concept is useful for the classifications. However, some example exits in class-B PA operation in form of push–pull amplifiers, which is normally used for audio applications.

The dissipated power is higher in class-A to limit the efficiency, while the class-B is not feasible. Therefore, ***class-AB*** PAs represents a reasonable solution to compromise between class-A and B in terms of linearity and efficiency. In that case, the transistor is normally biased close to threshold voltage. Today class-AB PAs are famous, and in use for linear PA applications in the telecommunication technology. LDMOS devices are most favorable up to 3.5 GHz, and mainly used in this class.

3.2.2 Switching PAs (Class C - F)

Switching PAs are attractive due to high efficiency as well as reducing the operational cost. In switching PAs, the efficiency is critical instead of linearity, such as in case of class-C, D E, F or F^{-1} [3]. The idea of the switching PA was first proposed by Ewing, G. in 1964 [17].

Class- C**:** In this class, *RF* transistor is switched on for less than half cycle ($\Theta < 180^0$), it means amplifier operates as a switch. A tank circuit is

used at the output to create a sinusoid signal. If Θ assumes at zero, then the current drawn from the device is assumed to be a piece of the input signal and the output voltage is a sinusoid with a peak voltage to V_{DD}. At this condition, η_D will be 100 % and the actual power delivered to the load will be proportional to Θ defined by following relation;

$$P_{RF} \propto \frac{\theta - \sin\theta}{1 - \cos\theta} \qquad (3.5)$$

The true class-C is not suitable for transreceivers, because if the η_D is 100 % then the peak output power, power handling capability and gain approaches to zero [11],[16]. These entire factors forced to use this class for less than 100% efficiency in piratical applications (not in an ideal condition).

Class-D: utilizes the output power for a half of the period as turned "on" and remaining half as turned "off" (as switching mode). It works similar to push-pull class-B with two transistors; the only difference is that the transistors work in switching mode rather than linear amplifications. During operation, if one transistor goes to zero voltage than other is forced to a voltage of $2V_{DD,}$ as a result transistors act like a switch and have η_D of 100% theoretically. It is also known as digital amplifier and most favorable with square wave signals.

The power handling capability is around 1/π (0. 32) much better than all above classes). Thus good η_d can be achieved with less stress on devices. The only drawback is non-zero saturation voltage has static dissipation in switching behavior, this is the reason it will perform well below cut-off frequency (f_T) [11].

Class- E: To obtain the ideal high efficiency (100%), the idea of class E amplifier was first presented by N. Sokal [18]. In such class, high efficiency is obtained along with delivering a good output power which has an advantage over class-C PA operation. Class-E deals with finite input and output transition times by proper load. As discussed in class D, the static dissipation will degrades the efficiency; therefore proper harmonic loading is required to force a zero switching for non-zero interval of time. Hence it exhibits a trade-off between efficiency (η) and output harmonics.

Another disadvantage of class-E is large peak voltage that the switch can sustain in the "off" state (~ 3.56 V_{DD}) [18]-[19]. The maximum output power will be taken as following:

$$P_{RF} = \frac{2}{1+\frac{\pi^2}{4}}\left(\frac{V_{DD}^2}{R}\right) \approx 0.577\left(\frac{V_{DD}^2}{R}\right) \qquad (3.6)$$

The power handling capability is quite low ~ 0.098. Due to high switching stress, it is not implemented gracefully with trend of low power technologies (for example in CMOS technology). However, Class E has an excellent performance with discrete components [11].

Class-F or F^{-1}: The basis of these modes consists of loading the active device output with appropriate terminations at fundamental and harmonic frequencies to improve efficiency (similar to class-E). But, when the drain voltage waveform adds odd harmonics to build the shape of the square wave, than the drain current waveform will add even harmonics to build the shape towards half sine wave. In this way, no power is generated at the harmonics because there is either no voltage or no current present before at a given harmonic. Therefore, ideal efficiency (100%) can be achieved together with desired (high) output power by proper controls of the harmonic loads. Alternately, in case of class- F^{-1}, the drain voltage can be used for a half sine wave by adding the even harmonics while drain current creates a square wave [20]-[21].

In class-F, total peak-to-peak voltage is seen to be twice, so the fundamental component will be equal to $(4/\pi).2.V_{DD}$. Therefore, the output power delivered will be [11]:

$$P_{RF} = \frac{\left(\left(4/\pi\right)V_{DD}\right)^2}{2R} \qquad (3.9)$$

Since, class F or F^{-1} has no power dissipation in switching behavior; therefore, they are capable of maximum efficiency and also superior to class-E due to twice of power handling capability.

At the end, a summary about the state-of-art PA classifications based on Si- LDMOS device is illustrated in Table- 3.1.

***Table 3.1** State-of- art in different classes of PAs based on LDMOS devices*

Class	Freq. (GHz)	Pout (dBm)	G (dB)	PAE/η_D (%)	Ref. (Year)
A	3.5	34.2	12.9	21.1/---	[26] (2008)
AB	2.69	36	12.6	39 /44	[27] (2010)
C	0.88	30.3	28.7	64 / ---	[28] (2004)
D	1.8	47.0	--	--- / 63	[29] (2005)
D	2.5	60.3	15.5	59.7/--	[51] (2010)
D^{-1}	1.0	43.0	15.1	---/ 71	[23] (2006)
E	1.0	39.1	14.8	73.6 / 76.1	[22] (2006)
E	2.14	39.8	13.8	--- / 65.2	[24] (2007)
E	3.7	---	8.3	74 / 87	[52] (2009)
F	0.5	49.0	--	--- / 76.6	[20] (2005)
F	2.1	35.9	24.0	77 / ---	[30] (2008)
F^{-1}	1.0	41.2	16.0	71.9 / 73.7	[25] (2006)

There are some other high efficiency classes also exits such as G, H and S etc. Such classes use different techniques to increase the efficiency. For example, G and H use resonators and multi power-supply voltage to reduce the power. While class-S uses a similar switching technique like class D, and E.

All above PA classes directly depends on the performance of power transistor and design considerations. Each classification of PAs is limited by the physical limitations of the active devices. For example in FET devices, there are four fundamental effects forced to deviate the ideal performance of PAs; on – resistance, maximum channel current, avalanche breakdown and drain to source breakdown voltage.

3.3 Large Signal Characterization in PA Design

To obtain the optimal performance in PA operations, the large signal impedance matching is an important factor to deliver the maximum power to the load. The well-known established technique for the large signal characterization is called “Load-pull”. It performed under different signal excitations, power levels and frequencies both in on-wafer or in-fixture set-

up [31]-[32]. The method also has flexibility in measurement to characterize the transistor at different sizes and frequencies for an accurate modeling of the transistor.

3.3.1 Load-Pull (LP)

Specific impedance terminations are important at the edges of device under test (DUT) to obtain desired PA design considerations, such as output power, gain, linearity and efficiency etc. Typical load pull measurements are plotted as contours of equal performance as function of input and output impedance termination superimposed on a smith chat [33]. The load-pull contours are in use for the design of solid state power amplifiers to extract the optimum impedance values [44]. The basic diagram of the load- pull test setup is illustrated in Fig. 3.6. The desired signal is generated by source, while *dc* supply is used to bias the DUT.

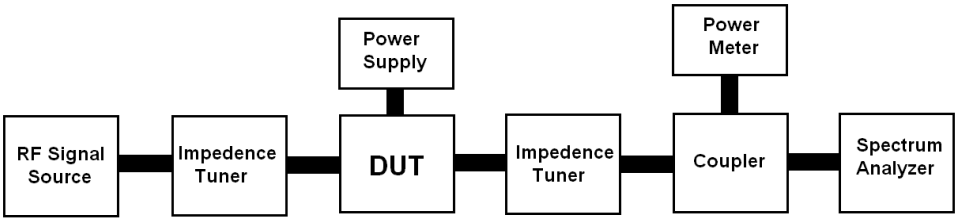


***Fig. 3.6** Basic load-pull test setup for the large signal RF characterization*

Source and load impedances are obtainable by impedance tuners. A power meter demonstrates the delivered power to the load. (A simple way of power measurement, modern sensors provides upto 114 dB dynamic range for CW signals, while for modulated signal it has 50 dB dynamic range [33]). The spectrum analyzer characteristics show the behavior of *RF* signal [44]. Different signal excitations are applied through *RF* signal source to create the contours of impedance smith chart for an optimal PA design. In load-pull, mechanical impedance tuners are used which consist of slab termination lines loaded by one or more sliding stubs. These mechanical stub tuners have limited range of impedances due to losses in the tuner reflection co-efficient. Nowadays, modern load-pull systems are classified into two main types; ***Passive and Active load-pull.***

In ***Passive load-pull***, highly precise electromechanical or PIN diode based tuners are in use for approaching the accurate matching. The PIN diode based tuners provides much better repeatability as compare to electromechanical tuners, but also have limited number of impedance states. Such type of system is capable to measure the *RF* device upto 100 - 200 W with 1 Ω impedance upto frequency range around 2 GHz. For higher frequencies like 40 GHz, we have to reduce the power rating upto 20 W [33]. The major disadvantage of the passive load-pull is that it can't handle those power devices which have optimum impedance values below than 1 Ω.

Active load-pull is a famous method of large signal characterization due to fast speed as compare to conventional load pull and has possibility to reach the reflection co-efficient > 1, and also compensate the losses of the system in matching the interface of the DUT. The load impedance is synthesized by sampling the output signal, modifying its phase and amplitude. In such case, the load impedance is completely synthesized according to following relation [35]:

$$Z_L = 50\frac{1+\Gamma}{1-\Gamma} \qquad (3.11)$$

Fig. 3.7 illustrates the block diagrams of the active load- pull system. An amplifier together with a phase shifter and attenuator is used as active impedance tuner which is coupled through a coupler as shown in Fig.3.7. In this way, by changing the phase and amplitude of the injected signal, the impedance can be seen from the DUT. A special care is required to assure that the PA doesn't contribute a significant amount of distortion. In modern active load pull setup, IQ modulators are used to make changes in phase and amplitude [36] - [37].

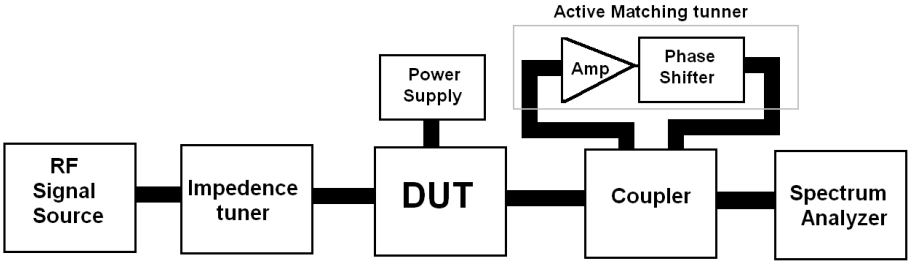


***Fig. 3.7** Basic Schematic of the active load-pull setup*

The major drawback in active load-pull system is the stability of the amplifier, which may contribute in distortion while in case of the passive system, the rapid frequency variations of passive tuners, may affect the distortion. Secondly impedance present at the edge of smith chart and even beyond in case of active load-pull [38].

To handle the multi-carrier signals today, the demand of higher efficiency and highly linear power amplifiers are increasing. For this, the harmonic studies become important, and create the demand of **harmonic load-pull system** [39]–[40]. A common approach is simply adding the harmonic impedances control. The basic schematic of the harmonic load pull set-up is shown in Fig. 3.8 [8].

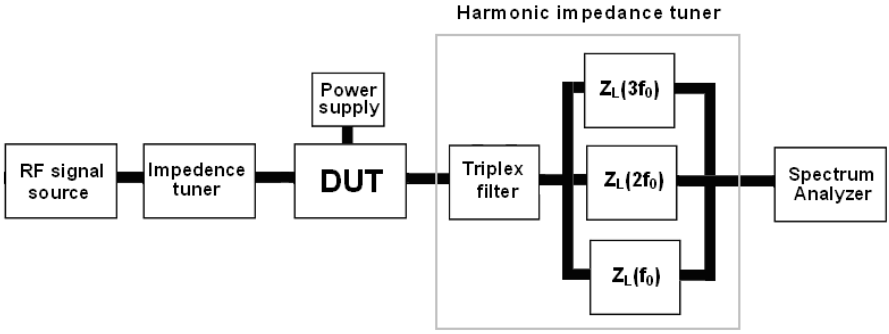


***Fig. 3.8** Basic schematic of the harmonic load-pull setup [8]*

A tri-plexer filter is required between the DUT and output impedance tuner; allowing the remaining two ports to be used for second and third harmonic tuning [8].

A major drawback is an additional loss of tri-plexer filter is added in such system, which will reduce the impedance range that can be realized at harmonic frequencies. Another approach is also famous by using the harmonic rejection tuner between the DUT and the fundamental tuner. But its disadvantage is varied in phase only not magnitude at the resulting harmonic frequencies [41]. Both passive and active load-pull systems have limited ability to deal the harmonics.

All type of load-pull set-ups has a basic goal to characterize the *RF* devices with accurate large signal analysis for a specified *RF* application. But it seems that they have different limitations and even sometimes it is

noticed that the device measurement results are not the same at different set-ups. It might be due to the limitation in calibration errors like tuner calibration errors, system component error, instrument imprecision, and repeatability of the impedance positions etc.

One way of improvement is to introduce the calibration methods of the set-up, which run in a reduced time and shows actual impedance error by measuring the background impedance of the system in different positions through a calibrated probe interfaces. For example, overall load pull system accuracy can be estimated by measuring gain difference *vs.* impedance [41]. *RF* researchers still working to improve the load-pull setups for large signal measurement procedure and its standards [42] - [45]

Another approach for an accurate large signal analysis is to perform the load pull simulation on fabricated or newly designed *RF* transistor. In this way, the instrumental measuring errors or calibration effects can be eliminated [46] - [47]. Computational Load-Pull (CLP) simulation technique is considered a well-known simulation method to characterize the *RF* devices under large signal behavior for different PAs [48] - [50]. The detail discussion on CLP method is in ***Chapter- 4***

3.4 References

[1] F. H. Raab, P. Asbeck, S. Cripps, P. B. Kenington, Z. B. Popovic et al. **"**Power mplifiers and transmitters for RF and microwave" *Journal IEEE Trans. Microwave Theory and Techniques*, v 50, n 3, p 814-26, 2002

[2] F. Rotella, G. Ma, Z. Yu and R. W. Dutton. "Modeling, analysis, and design of RF LDMOS devices using harmonic-balance device simulation" *Journal IEEE Trans. Microwave Theory and Techniques*, v 48, n 6, p 991-99, 2000

[3] Saad Al-Shahrani, Design of class-E radio frequency power amplifier, *PhD thesis, Virginia Polytechnic Institute and State university, Blacksburg, Virginia, U.S.A., 2001*

[4] http://www.educypedia.be/electronics/Images/rfdataspectrum.GIF

[5] R. Ludwing, and P. Bretchko, RF Circuit Design Theory and Applications, Prentice Hall, Inc , New Jersey USA,

[6] http://www.nxp.com/acrobat_download/other/campaigns/experience_rfpower /LDMOS_Transistors_in_Power_Microwave_Applications.pdf

[7] http://www.freescale.com/webapp/sps/site/training_information.jsp?code= WBNR_RF_POWER_MRF6VP11KH&fsrch=1#

[8] Olof Bengtsson, Design and characterization of RF-power LDMOS transistors, *Ph.D thesis Uppsala University, Sweden*, 2008 (ISBN 978-91-554-7269-6)

[9] Ted Johansson, The transistor, with emphasis on its use for radio frequency telecommunication, *Ph. D thesis Linköping University, Sweden*, 1998 (ISBN 91-7219-110-4

[10] F. van Rijs, and S. J. C. H. Theeuwen, "Efficiency improvement of LDMOS transistors for base stations: towards the theoretical limit," *Proc. of the IEDM*, p 1-4, 2006

[11] Thomas H. Lee, The design of CMOS Radio-frequency Integrated Circuits, 2nd Edn., *Cambridge University press, New York, USA.*

[12] J. H. K. Vuolevi, T. Rahkonen, and J. Manninen, "Measurement Technique for Characterizing Memory Effects in RF Power Amplifiers," *IEEE Trans. Microwave Theory Tech*, v 49, n 8, p 1383-1389, 2001

[13] Chistian Fager, Microwave FET modelling and Applications, PhD *thesis, Chalmers University of Technology, Göteborg, Sweden.* 2003 (ISBN 91-7291-286-3).

[14] Jaewoo Sim, Jaeyoung Choic, Kwon Kim, Myoungkyu Park, Wonwoo Kang, SeungGon Kim, Analysis and design of Doherty power amplifiers for digital pre-distortion linearizer, *Asia-Pacific Microwave Conference (APMC '07)*, p 1245-8, 2008

[15] David. M. Pozar, Microwave Engineering, 2nd Edn., John Willey & Sons, Inc. (ISBN 0-471-17096-8)

[16] Behzad Razavi, RF Microelectronics, 2nd *Edn, Prentice Hall, NJ, USA.*

[17] Ewing, G. G.**,** High-efficiency Radio-frequency power amplifier. *Ph.D Thesis, Oregon State University, Corvallis, Oregon, USA.* 1964

[18] N. Sokal, and A. Sokal, "Class E-A new class of high-efficiency tuned single-ended switching power amplifiers", J *IEEE Solid State Circuit*, v 10, n 3, p 168-176,1975

[19] T. Sowlati et al., "Low voltage high efficiency class E GaAs power amplifiers for wireless communications" *IEEE Journal of Solid-State Circuits*, p 1074-80, 1995

[20] F. Lépine, A. Ådahl, and H. Zirath, "L-Band LDMOS Power Amplifiers Based on an Inverse Class-F Architecture", *IEEE Trans. on Microwave Theory and Technique*, v 53, n 6, p 2007-12, 2005

[21] Frederick H. Raab, "Maximum Efficiency and Output of Class-F Power Amplifiers", *IEEE Trans. on Microwave Theory and Technique*, v 49, n 6, p 1162-66, 2001

[22] J. Lee, S. Kim, J. Nam, J. Kim, I Kim, and B. Kim. "Highly efficient LDMOS power amplifier based on class –E topology", *Microwave Optical Technology Letter*, v 48, p 789 –791, 2006

[23] H. M. Nemati, C. Fager and H. Zirath,"High efficiency LDMOS current mode Class- D power amplifier at 1 GHz", *36th European Microwave Conf. (EuMC)*, p 176-9, 2006

[24] Y-S Lee, and Y-H Jeong, "Applications of GaN HEMTs and SiC MESFETs in high fficiency Class- E power amplifier design for WCDMA applications", *IEEE MTT-S Dig.* , p 1099-1102, 2007

[25] A. Ouyahia, C. Duperier, C. Tolant, F. Temcamani, P. Eudeline, 'A 71.9 % power-added-efficiency inverse class- F LDMOS" *IEEE MTT-S Dig.* , p 1542-45, 2006

[26] P. Rakluea, J. Nakasuwan, "A 3.5 GHz WiMAX power amplifier using Si-LDMOS", *Int. Conf. on Control, Automation and Systems (ICCAS)*, p 1544-7, 2008

[27] Hui Li, K. Bathich, O. Bengtsson, G. Boeck, "A Si LDMOS Class AB Power Amplifier for UMTS LTE Base Stations" *2010 German Microwave Conference (GeMiC 2010)*, p 272-5, 2010

[28] Ki-Jae Song, Jong-Chul Lee, Byungje Lee, Jong-Heon Kim, and Nam-Young Kim, "High- efficiency class-C power amplifier module" *Microwave and optical technology letters*, v 40, n 2, p 164-67, 2004

[29] Ji-Yeon Kim, Dong-Hoon Han, Jong-Heon Kim, Stapleton, S.P. "A 50 W LDMOS current mode 1800 MHz class-D power amplifier" *IEEE MTT-S Int. Microwave Symposium*, p 1295-98, 2005

[30] A. Sheikh, C. Roff, J. Benedikt, P.J. Tasker, B. Noori, P. Aaen, and J. Wood, "Systematic waveform engineering enabling high efficiency modes of operation in Si LDMOS at both L-band and S-band frequencies" *2008 IEEE MTT-S Digest*, p 1143-6, 2008

[31] L. De Locht, Y. Rolain, and G. Vandersteen, "Designing power amplifiers? Use good excitation signals" *67th ARFTG Conf.*, p 211-13, 2007

[32] Y. Itoh, "Microwave & millimeter-wave amplifier design via load-pull techniques" *Technical Digest - GaAs IC Symposium*, p 43-46, 2000

[33] P. H. Aaen, J. A. PL´A, and J. Wood, "Modeling and characterization of RF and Microwave power FETs" *Cambridge University Press, 1st Edn.* 2007

[34] Sun Lingling, and Chen Xiane, "Load-pull simulation for large signal GaAsFET", *4th Int. Conf. on Solid-State and Integrated Circuit Technology*, p 601-3, 1995

[35] Z. Aboush, J. Lees, J. Benedikt, and P. Tasker, " Active harmonic load-pull system for characterizing highly mismatched high power transistors" *IEEE MTT-S*, p 1311-1314, 2005

[36] Seok Joo Doo, P. Roblin, V. Balasubramanian, R. Taylor, K. Dandu, J. Strahler, G.H. Jessen, and J.-P Teyssier, "Pulsed active load-pull measurements for the design of high-efficiency class-B RF power amplifiers with GaN HEMTs" *IEEE Trans on Microwave Theory and Techniques*, v 57, n 4, , p 881-89, 2009

[37] R. Actis, R. A.McMorran, R.A.Murphy, M.A. Hollis, R.W. Chick et al., "Large-signal characterization of millimeter-wave transistors using an active load-pull measurement system", *IEEE MTT-S Symposium Dig.*, v 2, p 835-8, 1989

[38] B. Hughes, A. Ferrero, and A. Cognata, "Accurate on-wafer power and harmonic measurements of mm-wave amplifiers and devices," in *IEEE MTT-S Symposium Dig*., p 1019–22, 1992

[39] D. Barataud, M. Campovecchio, and J-M Nebus, "Optimum Design of Very High-Efficiency Microwave Power Amplifiers Based on Time-Domain Harmonic Load–Pull Measurements" *IEEE TRANS ON MICROWAVE THEORY AND TECHNIQUES*, v 49, n 6, p 1107-12, 2001

[40] C. Jiang , R. Singh, Bo Liang, Xinwei Wang, Khoo Ee Sze, and H. Nakamura, "A two stages MMIC CDMA power amplifier using harmonic load pull simulation technique", *Asia Pacific Microwave Conf. (APMC'99)*, v 2, p 437-40, 1999

[41] M. Tutt, and E. Johnson, "Large signal RF characterization of bipolar transistors" *IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, p 66-73, 2007

[42] V. Teppati, A. Ferrero, and U. Pisani, "Recent advances in real-time load-pull systems" *IEEE Trans. on Instrumentation and Measurement*, v 57, n 11, p 2640-6, 2008

[43] Xian Cui, Seok Joo Doo, Patrick Roblin, Jeffrey Strahler, and Roberto G. Rojas-Teran, "High Efficiency RF Power Amplifier Designed With Harmonic Real-Time Active Load-Pull" *IEEE Microwave and wireless components letters*, v 18, n 4, p 266-68, 2008

[44] H. Arthaber, M. L. Mayer, A. Gafni, M. Gadringer, and G. Magerl, "A Time-Domain Large-Signal Measurement Setup" *Int. Journal of RF and Microwave Computer-Aided Engineering*, v 15, n 1, p 3-12, 2005

[45] G. Simpson, "High Power Load Pull with X-Parameters - a New Paradigm for Modeling and Design" *IEEE Annual Wireless and Microwave Technology Conf.* p 4, 2010

[46] J.M. Nebus, J.P Villotte, J.F. Vidalou, L. Hagerman, H. Jallageas, M.C. Albuquerque,n "Optimized C.A.D. of power amplifiers, for maximum added power or minimum third order intermodulation, using an optimization software coupled to a single tone source and load-pull set-up" *IEEE MTT-S Symposium Dig*., p 1049-1052, 1988

[47] Sun Lingling, and Chen Xiane, "Load-pull simulation for large signal GaAsFET" *4th Int. Conf.on Solid-State and Integrated Circuit Technology*, p 601-3, 1995

[48] P. A. Blackey, M. G. Khazhinsky, and G. H. Loechelt, "Direct Numerical Simulation of the Large-Signal RF behavior of Power Transistors," *Proc. EDMO'96*, p 14-19, 1996

[49] G. H. Loechelt, and P. A. Blakey, “A Computational Load-Pull System for Evaluating RF and Microwave Power Amplifier Technologies,” *IEEE MTT-S Symposium Dig.*, v 1, p 465–468, 2000

[50] R. Jonsson, Q. Wahab, S. Rudner, and C Svensson, “Computational load pull simulations of SiC microwave power transistors,” *Journal of Solid-State Electronics*, v 47, p 1921-1926, 2003

[51] N. Chevaux, M.M. De Souza, “Class-D power amplifiers using LDMOS and GaN power devices: a comparative analysis**”** *15th IEEE Mediterranean Electro-technical Conference*, p 691-4, 2010

[52] L.A. Montes, M. Villegas, and G. Baudoin, **“**Driving-signal optimization for LDMOS-SOI class E power amplifier efficiency enhancement**”** *IEEE 10th Annual Wireless and Microwave Technology Conf. (WAMICON)*, 4 p, 2009

Chapter 4

Optimization of LDMOS for PA Operation

Laterally diffused MOSFET (LDMOS) are pre-eminent technology of choice for medium and high power rating in the field of communication due to maturity as well as low cost. To fulfil the demands of wireless communication systems, LDMOS devices were improved with time by optimizing the structure in different ways. The source region is connected to the substrate with p-type deep sinker to eliminate the source bonding wire [1]–[2], utilizing the different alloys of polysilicon-silicides [3], steps in the drift region (two-stage drift techniques) [4], shortening the gate [5], the stacked layers of different doping in the drift region [6], dual implanted buried layer (n and p-type) at RESURF (reduced surface field) [7], additional field plate on the gate [8], and to apply a trench gate [9] etc. The ultimate goal of all these changes are to enhance the LDMOS device performance for *RF* applications.

The key point in the design of *RF*-LDMOS device is to achieve a best possible trade-off between BV_{DS} and R_{on}. In *RF*-LDMOS, a low doped drift (LDD) region is introduced between the gate and drain to increase the value of BV_{DS} as well as reduces a feedback capacitance (C_f). On the other hand, R_{on} increases which has dominant effect to degrade the *RF*- performance and also limit the frequency of operation. Thus, the drift length of LDD and channel region should be optimum with suitable value of breakdown voltage (usually 65 – 80 V is considered a suitable range for base station applications) [10]. LDMOS designers and process engineers are still trying to optimize this trade- off (BV_{DS} /R_{on}) in order to enhance the cut-off frequency for *RF* applications.

The first part of this chapter is about LDMOS design, our emphasis was to reduce the R_{on} while keeping the higher value of $BV_{DS.}$ We are very thankful to the Infenion Technologies AB, Sweden for providing a conventional LDMOS device structure (GM-V) as a case study (aimed for 28 V PAs operation with improved *RF* performance). The second part of the chapter describes the computational load-pull simulation methods to analyze the LDMOS device behaviour under large signal operation for different PAs operation.

4.1 About LDMOS Structure

Infenion Technologies AB, Sweden provided a conventional LDMOS transistor structure (GM-V). The structure was fabricated on a highly doped p^+ silicon substrate (~ 6-7 x 10^{18} cm^{-3}). A low doped p-type epitaxial layer of a doping in mid 10^{14} cm^{-3} is grown by conventional CVD technique. Source and Drain (n-type) regions were created by ion implantation. A low-doped n-type LDD region was introduced at the drain side. An implanted p-type body region was created below the source and gate regions to define channel length. The lateral diffusion of the dopants and the dimension of the p^- body region play an important role in controlling the threshold voltage and drain current saturation. After implantation and annealing, the channel length was 0.45 µm. The length of source and RESURF regions were 3.4 and 3.25 µm respectively. The gate oxide thickness is around 30 nm. A highly doped p-type (p^{++}) deep region (sinker) was implanted to connect the source internally with the substrate. The total length and width of the transistor structure for TCAD simulations is 12.7 µm in X- direction (along the surface) and 19 µm in Y- direction (top to bottom) respectively. Aluminium field plate is used at the top of gate and source to relax surface electric field under the edge of the gate electrode, and to prevent the hot electron degradation. Fig. 4.1 shows the schematic diagram of the LMDOS transistor's structure [Paper-I].

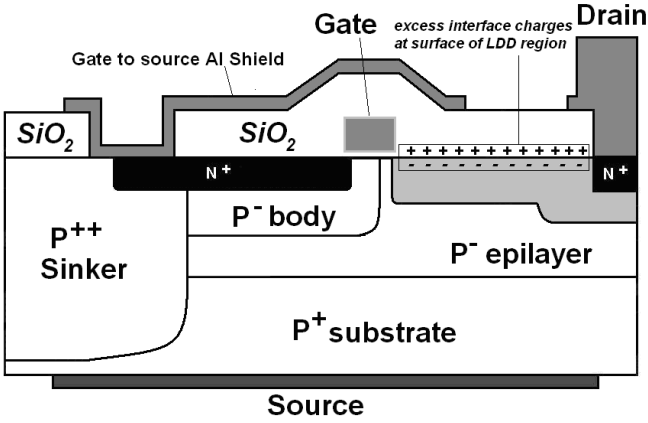


Fig. 4.1 ***Cross-sectional view of LDMOS structure with excess interface charges at the RESURF of LDD region***

4.2 DC Analysis of LDMOS

In the beginning, efforts were focused in TCAD simulations to match the drain current curves with measured data. Primarily some difficulties were faced to match the drain I-V curves by tuning the doping profiles of various regions such as sinker, p^- body, source and LDD etc. The optimization of doping profiles was not enough to match the upper and lower gate voltage curves properly, then we focused on process steps and its variations such as structure dimension, gate oxide thickness, and oxide interface charges at Si/SiO_2. Better correlation was observed between the simulated and measured drain current-voltage curves when interface state charges at the RESURF region were varied. The obtained results are shown in Fig. 4.2 [Paper-I], where the dotted lines are the simulated results while the solid lines are representing the measured current-voltage characteristics. (On-wafer measurements were performed to obtain *dc* characteristics using a semiconductor parameter analyzer HP4155/4156A). The on-wafer transistor has 1.2 mm gate width and metal frame connecting ground pads to the substrate with large deep P^{++} diffusion through the sinker region. The gate and drain terminal structure uses ground-signal-ground pads (a common test structure) to reduce self-oscillations. The bottom curve represents gate voltage of 3.5 V, and above this are from 4 to 8 V with 1 V step.)

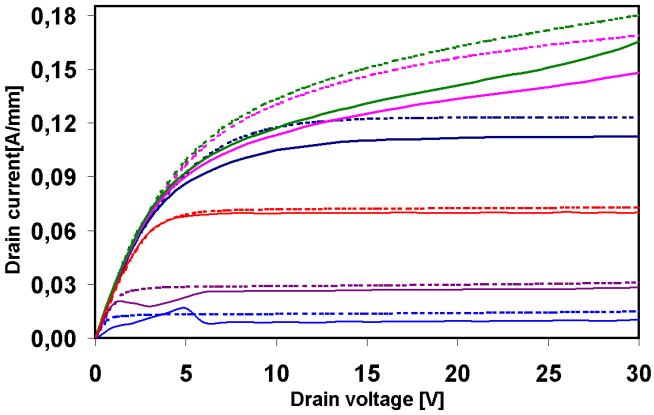


Fig. 4.2 ***I-V characteristics comparison of simulated (dotted lines) with measured data (solid lines). The gate voltages are 3.5 V and 4 to 8 V with 1 V step***

As can be seen from Fig. 4.2, the simulated drain current is matched reasonably good up to 6 V gate bias with the measured data, while above 6 V the simulated drain current is slightly higher. This discrepancy can be attributed to parasitic effects such as pad resistance etc. The input I-V characteristics of the reference LDMOS device at 5V drain bias provides a maximum transconductance (g_m) of 31 mS. R_{on} is calculated from the linear part of the drain I-V characteristics and has a value 23.5 Ω. mm. while the obtained value of BV_{DS} is ~ 77 V [**Paper-I**]. The optimal RESURF condition was also verified by studying the distribution of electrostatic potential as a function of drift length and potential contour lines as mentioned in **Paper - II**.

4.3 Optimization of LDMOS

As discussed above, low R_{on} is always stipulated for *RF* applications [11], because the power handling capability of a transistor is directly proportional to $(BV_{DS})^2/R_{on}$. In LDMOS, R_{on} is mainly dependent on the resistance of drift region; therefore we focused only on the LDD region of LDMOS (neglecting the channel and accumulation resistances). In conventional way, the current in the drift region can be defined by the carrier drift velocity in saturation as following [12];

$$I_{drift} = \mu_{eff} . q_{sheet} . \frac{v_{drift}}{L_{drift}} . W_{drift} \qquad (4.1)$$

Where, L_{drift} and W_{drift} represent the length of drift region and width of the transistor respectively. Therefore, R_{drift} can be defined by using equation (4.1) is;

$$R_{drift} = \frac{V_{drift}}{I_{drift}} = \frac{L_{drift}}{W_{drift}} . \rho . \left(1 + \frac{v_{drift}}{L_{drift} . E_{sat}} \right) \qquad (4.2)$$

Where, ρ and E_{sat} represent the resistivity and saturated electric field. BV_{DS} depends on L_{drift} and N_{eff} (net doping concentration) of LDD region. The electric field is sensitive to the net doping concentration (N_{eff}) and the thickness (t) of the region. Hence, a condition, N_{eff} x t = surface carrier density (S), must be equal or less then 3 x 10^{12} cm^{-2} for conventional breakdown [13]. This indicates that R_{on} will be reduced with the increment of surface charge carriers (q_{sheet}) at the surface of LDD region. Hence in optimization, the excess interface state charges were used at the RESURF region to maximize the drain current as shown in Fig. 4.1.

The interface charges (Si/SiO_2) at the RESURF region are expected to be higher as compare to the gate region. The reason is, gate oxide is grown in a very clean environment with a great care, while oxide and nitride layers on the RESURF region are deposited using LPCVD or Plasma CVD techniques. The interface charges depend on several parameters like, deposition techniques, deposition conditions, growth rates and the oxide/nitride layer thickness etc. During processing steps, these layers undergo few thermal stress cycles. Therefore, such charges are expected to be higher at the RESURF region. In the literature, the density of interface state charges deposited by plasma enhanced CVD technique and annealing with hydrogen is reported from 1.1x 10^{12} to 5.8 x 10^{11} eV cm^{-2} [14]. Therefore in device fabrication process, if the interface state charges at the RESURF can be controlled to a specific value by different techniques then it might be possible to increase the LDMOS performance.

To reduce R_{on}, the interface charge carrier was optimized in the range of 0.7 - 1.4 x 10^{12} cm^{-2}. The input I-V characteristics at 5 V drain bias are shown in Fig. 4.3 with excess interface charges together with provided

LDMOS structure (solid line represents reference LDMOS (GM-V)) [Paper-II]. By the excess interface charge technique, $I_{d\ (sat.)}$ increases to 282 mA, this is ~ 135 mA higher than GM-V results. A drastic reduction is also achieved in R_{on} to a value of 12 Ω.mm.

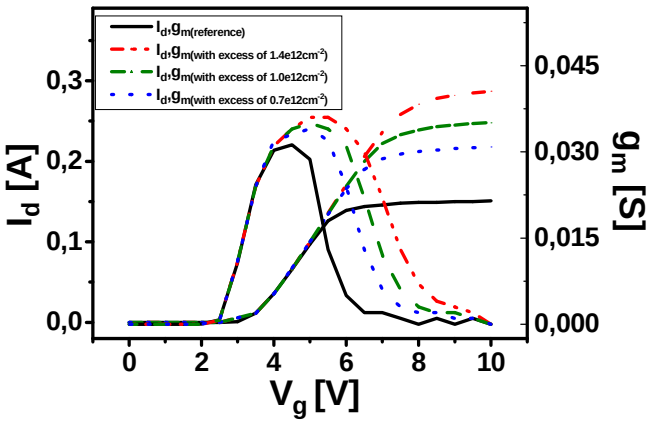


Fig. 4.3 ***Input I-V characteristics with excess interface charges at the RESURF of LDD region at 5V drain bias***

Fig. 4.4 shows distribution of the electric field, where dashed and dotted lines represent the behaviour of an optimized LDMOS structure (having excess interface charges) as a function of drift length. While solid line represents the reference case (GM-V) [Paper-II].

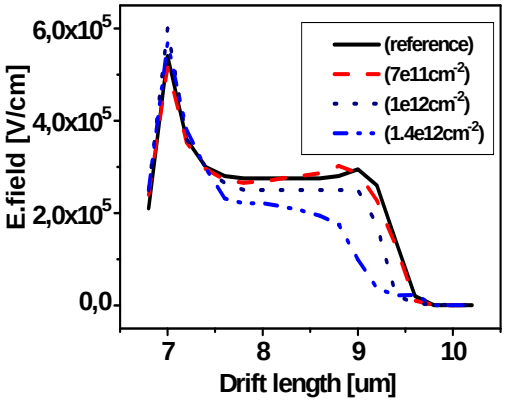


Fig. 4.4 ***Electric field distribution with excess interface charges at the RESURF of LDD region***

The electric fields of excess interface charges have slightly larger peak at the overlap region on the gate side while the other region showed uniform electric field. The results at different excess interface charges at the RESURF of LDD region are also summarized in Table 4.1. The optimized performance of LDMOS having the surface carrier density of 1.0×10^{12} cm^{-2} provides the 43% reduction in R_{on} together with 70V of BV_{DS} [Paper-II].

Table 4.1 ***DC characteristics of excess interface charges at the RESURF LDMOS structure [Paper-II]***

Excess interface charges at the RESURF corresponds to surface carrier density (cm^{-2})	**BV_{DS} (V)**	**R_{on} (Ω. mm)**	**$Id_{(sat)}$ (mA)**
7.0×10^{11}	**74.9**	**14.9**	**214**
1.0×10^{12}	**70**	**13.5**	**246**
1.4×10^{12}	**56**	**12.0**	**282**

The optimized LDMOS transistor provides promising results compared to the recent LDMOS devices from different manufactures. We have also compared the effect of excess interface charges on LDMOS device with a famous dual-layer surface doping technique at LDD region as explained in [7] while keeping the same doping profile of other region. As a result, 60 % enhancement is observed in our optimized LDMOS device [Paper–II]. Because the surface doping technique needs an implanted dose with specific thickness according to Gaussian phenomena while in case of interface charges, a thin layer is created easily at the RESURF of LDD region.

The process step might be complex in case of optimization, but still LDMOS structure is considered as an ideal FET device for *RF*-applications due to the advantage of two terminals at the top which reduces the inductive parasitic effect. Still no *RF*- device has such type of advantage to reduce the parasitic effectively as well as to support in packaging. Therefore, there is a need to optimize the LDMOS device continuously for achieving the advantage of low cost and easy implantation in integration circuits such as *RFICs.*

4.4 Computational Load-Pull (CLP) in TCAD for RF Analysis

In PA design, the accurate matching networks depend on transistor's input and output impedances, where the complex part depends on operating frequency. The transistor showing excellent *dc* characteristics is not always expected to produce good *RF* performance. Today computational load-pull (CLP) simulation technique shows potential to study the large signal analysis of the *RF* transistor in an accurate way before fabrication or maturing the active device for the different types of PA operation. The CLP simulation technique is developed first for CAD software by G.H. Loechelt and P.A. Blackey [15]-[16]. While our group at Linköping University developed further this technique in TCAD [17].

TCAD solves the Poisson and carrier distribution equations based on finite element methods to describe the device structure with material properties and doping concentrations. CLP set-up is built in a mixed mode of TCAD for a certain instant of time using transient simulations to solve the set of differential equations. After achieving steady state conditions, final steady state simulation time is used to produce the large signal behavior [17]. In TCAD, the time step is important in transient simulations because the time step decide the consecutive solution for achieving steady state solution in a particular time instant. Normally, the time step is not the same in TCAD simulations due to the convergence problem, which is not favorable for Fast Fourier Transformation (FFT) analysis. Therefore, TCAD transient data is needed to shift to other software (e.g. MATLAB) for equidistant sampling by using the spline interpolation or such kind methods. (Note: we used spline interpolation in MATLAB for FFT analysis). After FFT transformation, the resulting voltages and currents (V (f) and I (f)) provides the large signal parameters of PA such as impedances, gain, power added efficiency (PAE), and *RF* output power (P_{out}) by following equations.

$$Z_L(f) = \frac{V_L(f)}{I_L(f)} \qquad (4.3)$$

$$P_{out}(f) = \frac{1}{2} Re([V_L(f)][I_L(f)]^*) \qquad (4.4)$$

$$PAE = \frac{P_{out}(f) - P_{in}(f)}{P_{dc}} \qquad (4.5)$$

Large signal analysis in TCAD provides better precisions in accuracy, but it is considered a time consuming method in earlier period because it took very large computational time. Today modern computer having high speed and large storage capacity reduces the computational time and make it attractive technique for present and future *RF* applications.

4.4.1 Passive CLP Analysis

The CLP simulation technique in TCAD can be implemented in both passive and active loads. A schematic of the passive CLP simulation technique is shown in Fig. 4.5 [7].

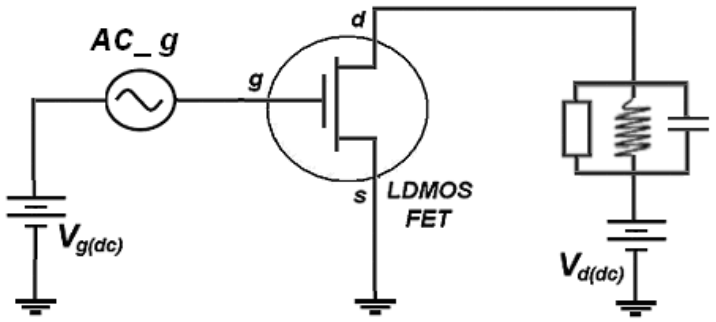


***Fig. 4.5** Schematic of Passive CLP setup [7]*

In passive CLP set-up, Q-value of the resonant network is important to adjust the time instant of transient simulation for steady state. Low Q- value reach steady state faster, but on the other hand it will decrease the isolation and other harmonic effects. While high Q-value of the resonant network increases the length of computational time of simulation. The adequate advantage of the passive CLP is that, its transient simulation in TCAD provides the actual current and voltage waveforms of the circuit [18]. For good accuracy in passive CLP, several unnecessary *RF* cycle periods are required in transient TCAD simulation before steady state, which may be

a burden on computers. A complexity in the device's structure increases the computational time and convergence issues.

4.4.2 Active CLP Analysis

The active CLP technique allows a complete circuit environment in device simulations with active matching at the input and output. In active CLP, the transistor is directly driven by sinusoidal *ac* voltage sources both at input and output as shown in Fig. 4.6 [18].

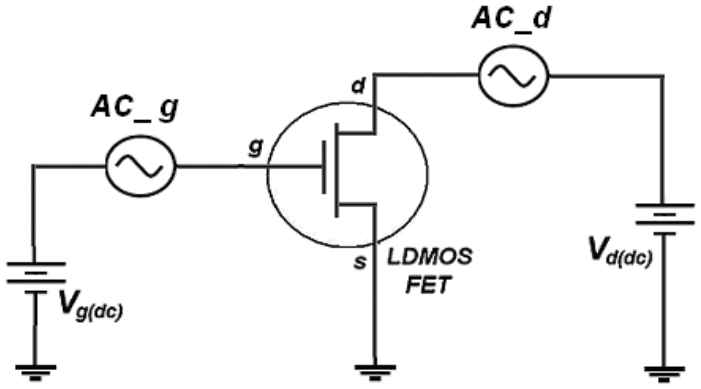


***Fig. 4.6** Schematic of Active CLP setup [18]*

At the input (gate terminal), *dc* bias was selected for different classes of amplifiers such as, class A, AB and so on. The simulation is performed in time domain by applying the large sinusoidal signal to the gate terminal (at the input) and the resulting drain current and voltage signals (at the output) are then used to extract the parameters such as output power, efficiency, gain and impedances [17]. At the drain terminal, *ac* signal is simultaneously applied at the same fundamental frequency of the gate but with 180^0 phase difference. In this way, CLP technique extract true impedances at the interface of physical transistor's terminals without any external parasitic e.g. bond wires, pad capacitance etc. Active CLP analysis is an efficient way to extract large signal parameters in a short time. In active load pull, full *RF* power delivered to the load can be computed from the time domain output current and voltage waveform as following;

$$P_{out} = \frac{1}{T}\int_0^T \left(V_{L(t)} - V_D\right).i_{D(t)}.dt \qquad (4.6)$$

Where, $V_{L(t)}$ is the time varying voltage swing across the load and *T* is the time period of duty cycle. Therefore, optimum load impedance is determined on which the maximum output power is transferred to the load resulting in high power efficiency.

The simulation time is short compared to passive CLP, only 2-3 *RF* cycles of the carrier frequency is sufficient to obtain the state steady. After steady state, the resulting drain current and voltage signals were transformed into frequency domain using Fast Fourier Transformation (FFT). Hence, the large signal parameters of PA such as impedances (Z), gain (G), power added efficiency (PAE), and *RF* output power (Pout) can be calculated. Another advantage of the active CLP is that it resolves only the fundamental tone due to ideal sine wave voltage source and shorted all higher harmonics. Therefore, it is possible to estimate the optimal performance of *RF* transistor intrinsically.

Through active CLP simulation technique, we studied optimized LDMOS transistor under large signal operation. 28 V *dc* bias was selected at the drain terminal to bias the transistor, while gate biases were 6 and 4.5 V *dc* for class A and AB respectively. In order to observe the optimum impedance at any frequency for both classes of amplifiers, the matching conditions were adjusted by changing the drain *RF* voltage amplitude and phase difference variation between gate and drain *RF* voltage signals. Fig. 4.7 shows complex conjugate output impedance on smith chart with normalized to 50 Ω for class AB operation at 2 GHz. The arrows indicate changes in amplitude from left to right (from 30 - 40 V_{p-p}) and the phase variation from top to bottom (from 0 - 35 degree). The corresponding optimum impedance was about 124+ j17.7 Ω.

The *RF* output power ~ 1.54 W/mm is obtained with 49 % PAE. We observed that impedance values are not scattered on the smith chart and were optimized by simply adjusting phase delay. The optimized impedance value was obtained at the amplitude of 40 V_{p-p} with 20^0 phase delay at 2 GHz. Similarly simulations were performed upto 4 GHz. The results are summarized in Table 4.2. These results indicate that the optimized LDMOS are playing an important role in *RF* performance [for further detail see *Paper-1*].

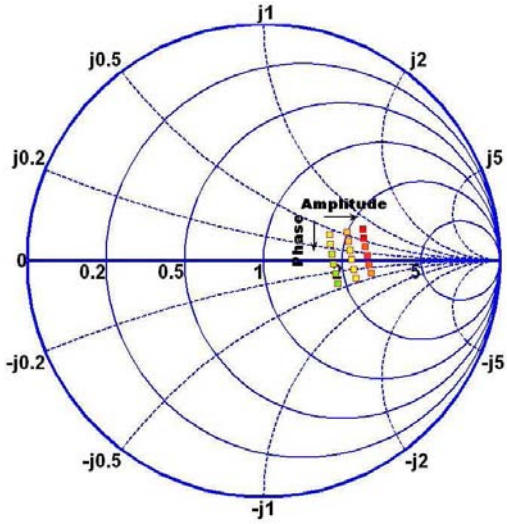


Fig. 4.7 ***Conjugate output impedances on normalized smith chart to 50 Ω for class AB PA at 2 GHz with amplitude and phase variation***

Table 4.2 ***Large signal RF time domain active CLP simulation results in TCAD for class A and AB operation at 1, 2, 2.5, 3 and 4 GHz***

Frequency (GHz)	Class A PA operation			Class AB PA operation		
	Output RF power (W/mm)	PAE (%)	Gain (dB)	Output RF power (W/mm)	PAE (%)	Gain (dB)
1	1.35	28.1	30.2	1.59	51.0	29.0
2	1.28	26.5	24.4	1.54	49.0	23.5
2.5	1.24	25.4	22.6	1.51	48.0	21.6
3	1.20	25.2	20.9	1.47	45.0	20.3
4	1.05	21.1	18.6	1.37	41.2	18.1

4.5 CLP technique for non-linear analysis

RF designers have great interest to understand the non-linear behavior of *RF* transistors, especially when power factor is important such as in the case of power amplifier [20]-[22]. Any FET transistor traversed strong nonlinearities under large-signal and there is a need to identify transistor behavior such as current turn-on and current saturation imposed by the load line. In wireless communication, the in-band third-order inter-modulation distortion (IMD_3) is an important non-linear parameter which is generated by two input signals, carrier frequency (f_1), and the second tone (f_2). This two-tone modulated signal, appear at the output spectrum as IMD_3 sidebands at frequencies $2f_1 - f_2$ and $2f_2 - f_1$. Two-tone measurements mainly depend on the signal excitation (both in amplitude and frequency) and load impedances which depend on the behavior of drain current of LDMOS.

In two-tone method, the excitation voltage (v_{in}) at the input is defined by;

$$v_{in(t)} = A[\cos(2\pi f_1 t) + \cos(2\pi f_2 t)] \qquad (4.7)$$

Where, A is the amplitude of the signal.

To analyze the IMD behavior in PA operation, it is essential to implement proper output current transfer function (TF), which means the transistor characteristics in combination with the drain bias, load impedance and transistor parasitic elements [23]. The non-linear model of the transistor provides the behavior of IMD close to experiment by implementing an accurate current source generator to define a proper TF at the cost of huge experimental data and several iterations of the fabrication.

An active CLP technique is further extended by a mimic concept of two-tone analysis as shown in Fig. 4.8. *RF*-LDMOS transistor is biased by *dc* voltage sources, $V_{g\ (dc)}$ and $V_{d\ (dc)}$ to the gate and drain terminals respectively. To create a two-tone signal at the input, the carrier frequency (f_1) and second tone of frequency (f_2) are generated through ideal *ac* voltage sources, *V*in_1 and *V*in_2, in series to the gate terminal. At the output on drain terminal, the time varying signal generators is applied (*V*out_1 and *V*out_2) as an active load at the same frequency of the input signal, but with 180° out of phase, as shown in Fig. 4.8 [Paper-IV].

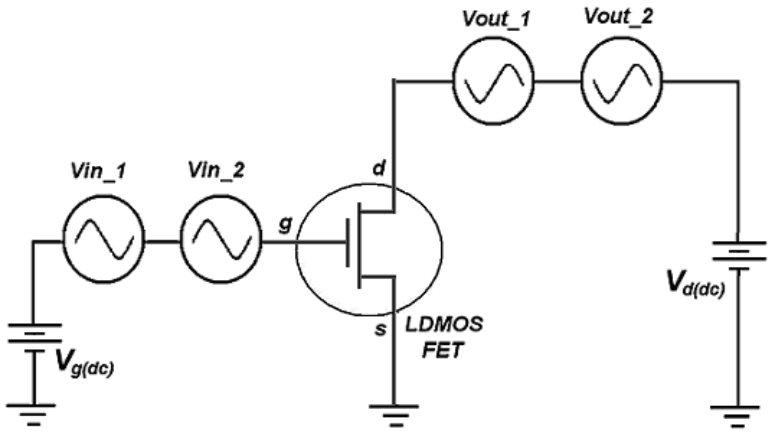


***Fig. 4.8** Schematic of Two- Tone Test setup in TCAD*

A periodic modulated signal is generated across the gate and drain, by these two tones and inter-modulation distortions (IMDs). The periodic drain modulated signal of LDMOS transistor in class AB PA operation at 1 GHz is shown in Fig. 4.9 [Paper-IV]

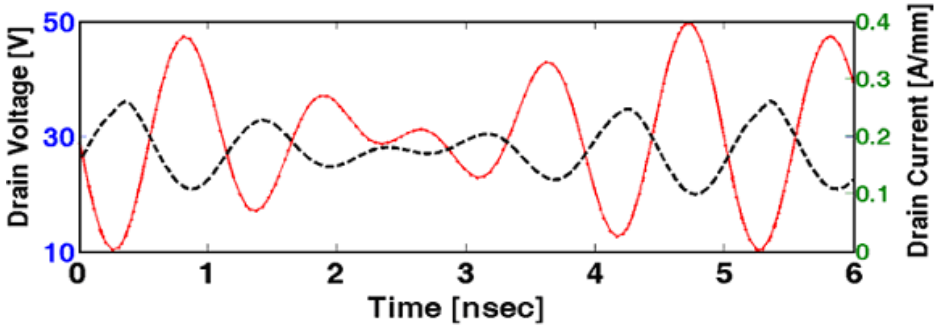


***Fig. 4.9** Modulated Two-Tone signal in TCAD at the drain of RF-LDMOS in class AB PA*

The maximum amplitude of the drain voltage (solid line) swing holds below breakdown and above threshold voltage with tolerances. Thus in this way, TCAD nonlinear approach provides the real environment as is used in the measurements.

In this technique, tone spacing ($f_2 - f_1$) is also an important factor in order to investigate the isolation of the carrier with other close signals, which cause the interferences in the same communication band. As TCAD time domain simulation takes large computational time due to the finite element method (e.g. the finite matrices such as Jacobian method). Therefore, relatively large tone spacing is selected to minimize the computational time for least isolation levels. For example, carrier frequency was selected at 1 GHz with 200 MHz tone spacing for a complete modulated signal in five *RF* duty cycles as shown in Fig. 4.9.

The resulting modulated drain current and voltage signals in simulation are then transformed from time to frequency domain using the Fast Fourier Transformation (FFT) in the same way as explained in active CLP technique. The resulting output power is obtained by calculating the *RF* current flowing through the real part of the carrier impedance. Thus the carrier, second tone and inter-modulations (IMD*s*) currents were observed precisely together with other even and odd harmonic products. The IMD*s* and output intercept point (OIP_3) is obtained by plotting output power (P_{out}) *vs.* input voltage signal (V_{in}) as shown in Fig. 4.10 [Paper-IV]

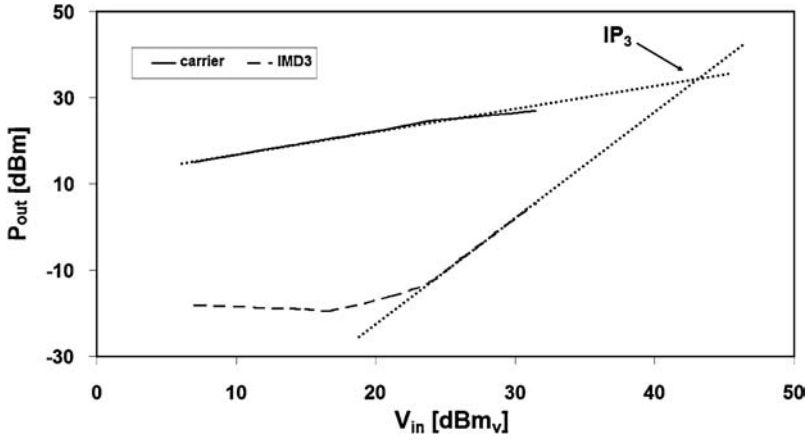


Fig. 4.10 ***A graph of RF output power (P_{out}) vs. input voltage signal (V_{in}) of LDMOS in class AB PA***

4.5.1 Validation by fabricated PA

To validate TCAD non-linear simulation approach, PA was designed and fabricated on similar LDMOS transistor. The Rogers RO4350B substrate was used in PA fabrication. The fabricated PA is shown in Fig. 4.11 [Paper-IV].

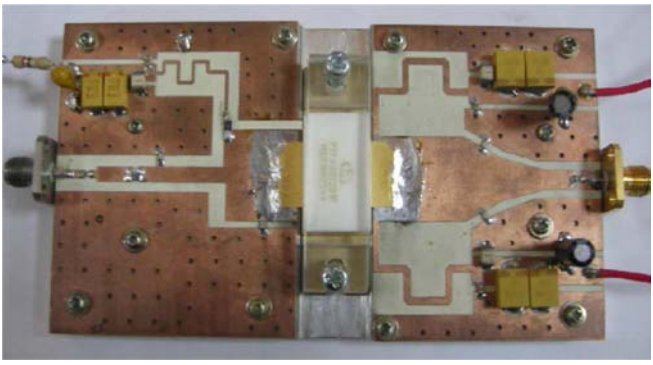


***Fig. 4.11** A photograph of fabricated PA based on LDMOS device*

The fabricated PA produced an *RF* output power of 49 dBm at P_{1dB} together with 17.4 dB power gain at 900 MHz. The measured two-tone results showed 47 dBm *RF* output power at P_{1dB}, while the lower IMD_3 level was obtained around −16.5 dBc. Similarly −30.3 dBc isolation is achieved at 5 dB back-off condition. An output intercept point (OIP_3) of 56.5 dBm was achieved by extrapolation of the carrier and 3rd harmonic curves. In comparison, 1-dB compression point (P_{1dB}) was considered as a reference. At P_{1dB}, the level of IMD_3 was around −22 dBc in TCAD while the fabricated PA shows −16.5 dBc as tabulated in Table 4.3 [Paper-IV]. The

***Table 4.3** Comparison of non-linear analysis of LDMOS transistor in TCAD, and fabricated PA [Paper-IV]*

Non linear Analysis **IMD3 level at**	**Units**	**TCAD analysis of intrinsic LDMOS**	**Fabricated PA based on LDMOS**
P_{1dB}	**dBc**	**-22**	**-16.5**
5 dB back-off	**dBc**	**-32**	**-30.3**
10 dB back-off	**dBc**	**-36**	**-35.8**
OIP_3 above P1dB	**dBm**	**10**	**9.5**

lower value of IMD_3 in fabricated PA comes either due to the package parasitic which was not incorporated in case of TCAD simulation or may other additional passive effects etc.

Hence TCAD non-linear approach provides a realistic operation of the physical LDMOS transistor. Through this technique, the transistor design in terms of structure (thicknesses and doping concentrations of various layers/regions) can be optimized directly at device level in a reduced design cycle of time. Therefore, TCAD provides conjecture about the physical function of *RF* transistor without external circuitry.

4.6 Modification in CLP for Switching Analysis

Today digitally modulated communication standards, such as WCDMA, and WLAN etc, demand development in the power amplifier (PA) to transfer and amplify the complex modulated signals with high efficiency and less distortion. The demand of high-data-rate transmission is increasing in multimedia communications. As a solution, switching PA (e.g. class- F and F^{-1} mode) in combination with digital pre-distortion is getting more and more attractive to achieve the goals of high efficiency together with output *RF* power compared to class B or AB [24]–[26]. Nowadays different switching PA modes, such as, class-C, D, E, F and F^{-1} are successfully functioning in different communication systems, such as phase array radar, multi-band antennas etc. [27]-[29].

4.6.1 CLP technique for pulsed mode PAs

In our group we have developed a switching CLP technique in 2008 [33] by applying a pulse signal at the gate terminal of the device while keeping the sinusoid signal at the drain terminal. This is referred as pulsed input class-C operation, and the technique is sufficiently good for the study of switching behavior of the input (gate) terminal of the transistor. The schematic of the pulsed CLP simulation setup for switching PA is shown in Fig. 4.12 [30]. Hence by the pulse-mode at input, the function of device can be studied under pulse-mode conditions from 10 to 50 % duty cycle of the fundamental frequency in order to observe switching parameters, such as switching losses, under large signal parameters.

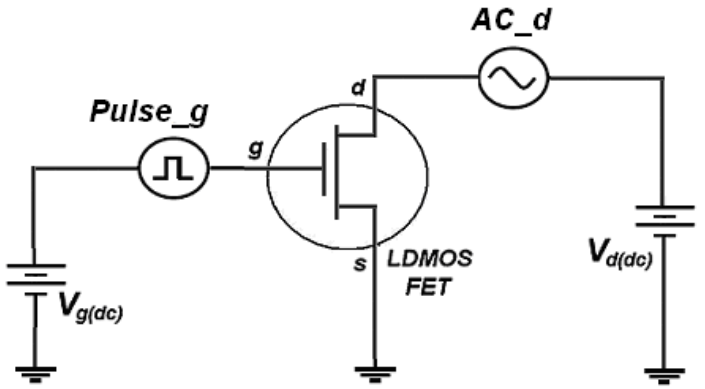


***Fig. 4.12** A setup of CLP simulation for pulsed class- C PA [30]*

Through this, 10 % pulsed duty cycle of the carrier frequency (2 GHz) was applied at the input terminal of LDMOS transistor. The pulse height was 8 V. At the output, *dc* supply was set to 28 V and *ac* voltage signal of $40V_{p\text{-}p}$ was applied in opposite direction (180^0 output of phase) as shown in Fig. 4. 13. The dissipated power (switching loss) was 0.356 W/mm. The stored charges during transition of pulse as resistive (R) and capacitive (C) part of the drain current during OFF state is shown as dashed area in Fig. 4.13.

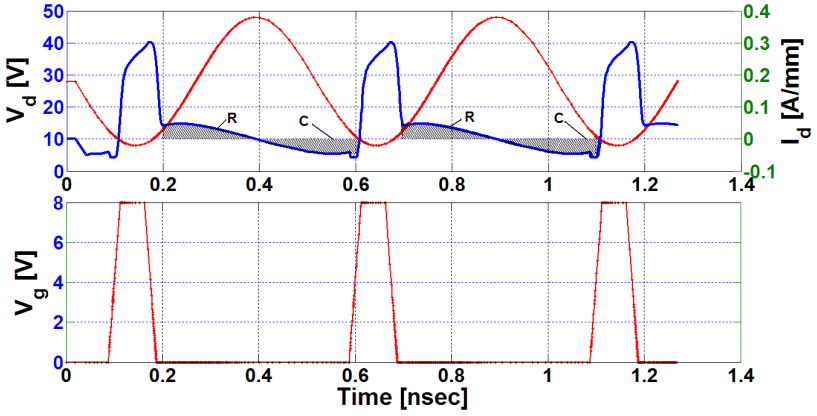


***Fig. 4.13** Time –domain drain current and voltage signals together with applied input pulse voltage signal (10% of 2 GHz).*

After FFT transformation of Fig. 4.13, the PAE of 67 % achieved with 21 dB of power gain. The major drawback of this technique, there is no way of separating the harmonic loads as required in case of new switching classes like class E, F and F^{-1} etc.

4.6.2 CLP technique for switching PAs (class-F)

In switching PAs, an ideal drain efficiency of 100% can be attained theoretically. However, in practice, the active device is no longer operating as an ideal switch due to the finite on-resistance and parasitic capacitances. The switching response of the transistor is already discussed in [30] or section 4.6.1. However in this approach, the separation of the harmonic load was not considered as required in class, like E, F and F^{-1}etc. Therefore, we still focus to explore the minimum overlap condition between output current and voltage signals.

Nowadays, class-F PA deliver high output power at high efficiency by generating ideally half-sinusoidal current and square voltage waveforms. These waveforms can be obtained by creating zero impedance at all even harmonics and finite impedance at all odd harmonics. However, in practice, class-F PA mainly depends on second and third harmonic controls only [25]. To achieve the optimal high efficiency, a set-up of class F PA is built in TCAD as shown in Fig. 4.14.

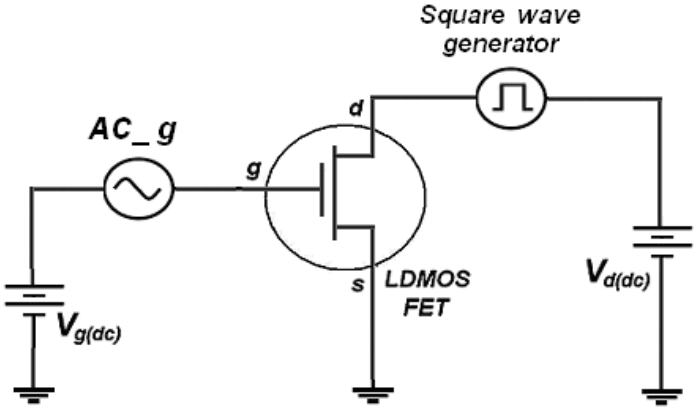


***Fig. 4.14** A setup of CLP simulation for switching class-F PA*

A fixed bias voltage was applied at the gate (Vg_dc) and drain (Vd_dc) respectively. An *ac* voltage source is applied at the gate terminal of the *RF*-transistor to create *RF* signal at the input. To achieve class-F PA condition, an ideal square wave signal generator is used at the output of the transistor to act as a short for even harmonics, while open for odd harmonics. The power losses are related to the on-resistance and output capacitance of transistor, which plays a major role in the current dissipation. So, it is essential to minimize the overlap condition between the drain voltage and the drain current waveforms during switching transition; this reduces the current dissipation in turn enhances efficiency. Hence in this technique, a square wave voltage generator controls the harmonic terminations by adjusting the ramp rate, minima and maxima to reduce the overlap condition for achieving high efficiency together with *RF* output power.

After adjusting the ramp rate of the *RF*-LDMOS transistor at 130 ps, a narrowband *RF* signal is applied at the input. The obtained time domain class-F result in TCAD is shown in Fig. 4.15. A solid line represents the drain voltage signal, while the dotted line shows the obtain drain current. The peak of capacitive current is due to abrupt changes in derivative of the drain voltage pulse.

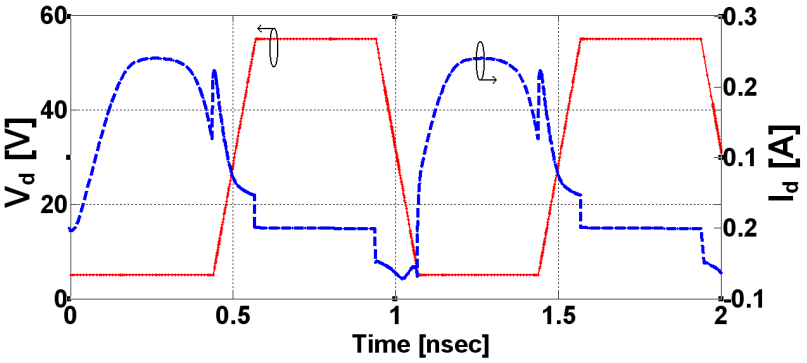
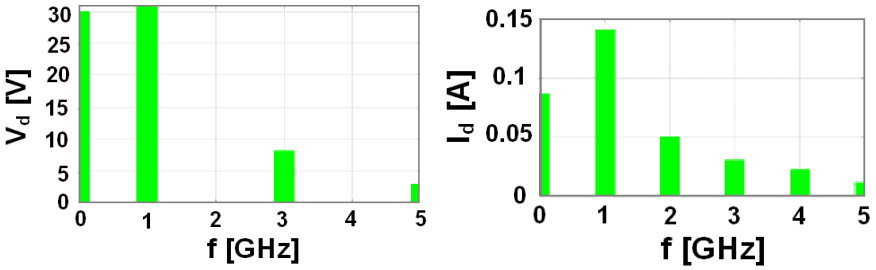


Fig. 4.15 ***Time –domain obtained results in form of drain current and voltage signal.***

Fig. 4.16 shows the FFT analysis of Fig. 4.15 in a graphical form. The amplitudes of the drain voltages are observed at *dc* bias, resonant frequency (f_0), and odd harmonic voltages ($3f_0$ and $5f_0$). No even harmonic voltages are observed at $2f_0$ and $4f_0$ according to the class-F definition. Similarly, the drain current co-efficient corresponds to I_{dq}, f_0, and other frequencies ($2f_0$, $3f_0$

etc) as shown in Fig. 4.16 (b). *RF* output power of 1.97 W/mm is achieved at *dc* power level of 2.42 W resulting a PAE around 81.2 %.

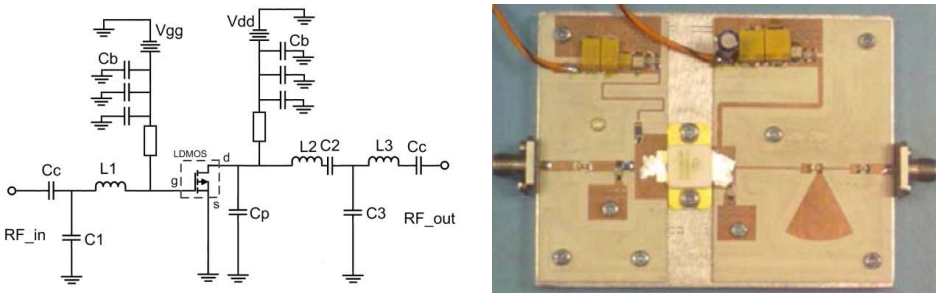


(a) (b)

Fig. 4.16 ***Drain Fourier co-efficients a) voltage vs. frequency, and b) current vs. frequency***

4.6.3 Validation by fabricated Class- F PA

To validate the CLP technique for switching PAs, a class F PA was designed and fabricated on Roger Duroid substrate of TMM4 having thickness of 1.27 mm. The schematic and photograph of fabricated class F PA is shown in Fig. 4.17. Fixed gate-to-source voltage is used to set the quiescent point (I_{dq}), while the drain voltage is applied to bias the LDMOS device. Matching networks are designed for the impedance transformation to 50-Ω system. L-type network is used in the matching, which consists of a series inductor and shunt capacitor as shown in Fig. 4.17. The combination of resonant circuit and matching to 50-Ω system is critical in class-F PA design.



(a) (b)

Fig. 4.17 ***Class- F PA based on LDMOS a) Schematic diagram in ADS, and b) photograph of fabricated PA***

In measurement, the input power (P_{in}) was swept from 20 to 34 dBm. We obtained results close to the simulated results of TCAD at 900 MHz. *RF* output power of 47 dBm is achieved with PAE around 76 %. This difference is due to the parasitic effects of lumped components used in matching networks. While 100 MHz shift might be due to the improper output matching network or some discrepancies in large signal model of the device [31].

4.7 Advantage of CLP method in the designing of Broadband PA ICs

Today the communication systems need to handle multi-bands for different applications such as cellular phones, satellite communication and various types of phased array antenna systems [32] - [34]. A broadband power amplifier (BPA) is mandatory for multi-standard multi-frequency base station transmitter with optimal performance such as higher output power, efficiency and linearity. However, BPA design is not a simple task because the transistor input and output impedances vary with frequency, signal level, and bias points. Therefore, the broadband matching networks has a classical problem of impedance mismatch in order to obtain the desired *RF* performance [35] - [37].

Nowadays on-chip broadband power amplifier integrated circuit (PA ICs) has capability to handle the output power equivalence with discrete modules of PAs as well as its price is quite revolutionary. PA ICs also provide a cost effective solution for the driver applications in the base station transmitters [38]. To overcome impedance mismatch problems both in PA ICs and discrete devices, *RF* designers are searching a simple way to study the optimal behavior of the active transistor with output matching under a large signal operation.

The time domain CLP simulations in a mixed mode of TCAD is a simple way for broadband circuit analysis by coupling the physical structure of the active device (such as transistors or diodes) together with spice model of lumped elements and sources. As a result, it is easier to design an accurate matching network of the amplifier. It reduces the iterative process for fabrication. The characteristic (or optimal) impedance (Z_f) is extracted and used in the design of broadband matching network without any additional

circuitry. The steps followed in the designing of a broadband PA in TCAD are as following:

1. Design the *RF* transistor's structure to obtain the maximum drain current and breakdown voltage, together with low on-resistance in *dc* solution.
2. Selection and verification of an optimal bias point with respect to the input signal level close to 1-dB compression point (P_{in} *vs*. P_{out}).
3. CLP simulation in large signal analysis to obtain data of the load and source impedances as a complex conjugate at desired operating frequencies.
4. Designing of matching networks with the help of the characteristic impedances (Z_f) obtained by CLP simulations.
5. Finally verification of the broadband PAs operation is done in a mixed mode of TCAD by time domain analysis.

We already observed in ***Paper-I*** that the LDMOS transistor has a delay response of 27.8 ps in class AB operation. For BPA design, the impedances of the LDMOS transistor were tuned accordingly to the phase delay 19^0,21^0,23^0, and 25^0 for the operating frequencies of 1.9, 2.1, 2.3 and 2.5 GHz respectively. Fig. 4.18 shows the complex conjugate of source and load impedances of the *RF*- LMDOS transistor on normalized smith chart. The optimal load impedance (Z_f) is shown by a rectangular box on a smith chart.

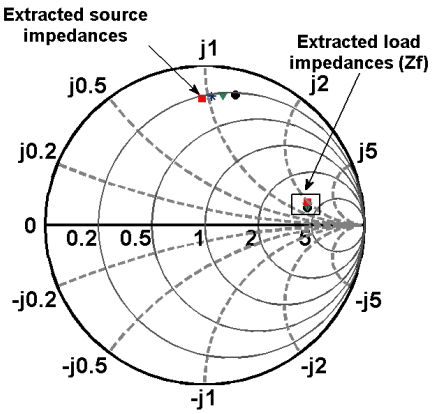


Fig. 4.18 ***Optimum extracted impedances of RF-LDMOS transistor at 1.9, 2.1, 2.3 and 2.5 GHz class AB PA on Smith chart***

The corresponding large signal parameters of the CLP analysis for Broadband PA design are shown in Fig. 4.19. The PAE is around 53.2 $\pm$ 0.6 % together with power gain (G) of 22.3 $\pm$ 1 dB. The slope in power gain is due to gain roll-off phenomena with the increase of frequency and can be make flat by an additional circuitry at the input matching network as described in [34] and [39]. An *RF*-output power of 30.9 dBm was achieved.

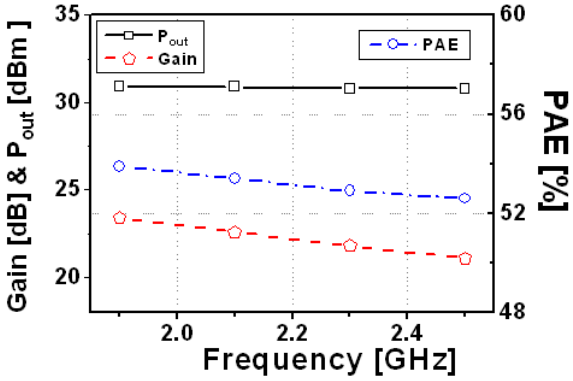


Fig.4.19 ***Gain, P_{out} and PAE vs. frequency points obtained by CLP simulations [Paper-VI]***

4.8 RF performance comparison through CLP Analysis

The *RF* performance of the optimized LDMOS transistor structure was analyzed in TCAD through different methods of CLP simulation techniques in order to analyze the transistor behaviour for different PAs. A summary about *RF* performance of an optimized LDMMOS transistor structure is shown in Table- 4.3. (*Note:* transistor has width of 1 mm at z- direction).

Table 4.4 ***RF performance of optimized LDMOS structure for different PAs***

PA Classes	frequency [GHz]	RF-output power [dBm]	Gain [dB]	PAE [%]	References
A	**3.0**	**30.7**	**22.6**	**25.2**	**Paper-I**
A	**4.0**	**30.0**	**18.6**	**21.1**	**Paper-I**
AB	**3.0**	**31.7**	**20.3**	**45.0**	**Paper-I**
AB	**4.0**	**31.4**	**18.1**	**41.2**	**Paper-I**
C	**2.0**	**28.5**	**21.0**	**67.0**	**------**
F	**1.0**	**32.0**	**23.0**	**81.2**	**Paper-V**
Broadband class AB	**1.9 - 2.5**	**30.9**	**22.3 $\pm$ 1**	**53.2 $\pm$ 0.6**	**Paper-VI**

4.9 References

[1] A. Wood, C. Dragon, and W. Burger, "High-performance silicon LDMOS technology for 2 GHz RF power amplifier applications". *IEEE Int. Elec. Dev. Meet. (IEDM) Tech. Dig.*, p 87–90, 1996

[2] C. Kim, J. Park, and H. Yu, "Trenched sinker LDMOSFET (TS-LDMOSFET) structure for high power amplifier application above 2 GHz". *IEEE Int. Elec. Dev. Meet. (IEDM) Tech. Dig.*, p 887–90, 2001

[3] I. Yoshida, "2-GHz Si power MOSFET technology" *IEEE Int. Elec. Dev. Meet. (IEDM) Tech. Dig.*, p 51–4, 1997

[4] S. Xu, P. Foo, J. Wen, Y. Liu, F. Lin, and C. En," RF LDMOS with extreme low parasitic feedback capacitance and high hot-carrier immunity" *IEEE Int. Elec. Dev. Meet. (IEDM) Tech. Dig.*, p 201–04, 1999

[5] M. Shindo, M. Morikawa, T. Fujioka, K. Nagura, K.Kurotani, K. Odaira, T. Uchiyama, and I. Yoshida, "High power LDMOS for cellular base station applications", *Int. Symp. Power Semiconductor Devices ICs*, p 107-110, 2001

[6] J. Cai, C. Ren, N. Balasubramanian, and J. K. O. Sin, "A novel high performance stacked LDD RF LDMOSFET" *IEEE Elec. Dev. Let.*, **v** 22, p 236–38, 2001

[7] J. Olsson, N. Rorsman, L. Vestling, C. Fager, J. Ankarcrona, H. Zirath, K.-H. Eklund, "1 W/mm RF power density at 3.2 GHz for a dual-layer RESURF LDMOS transistor" *in IEEE Electron Device Letters*, v 23, issue 4, p 206 – 08, 2002

[8] I. Cortes, P. Frenandez-Martinez, D. Flores, S. Hidalgo, J.REbollo, "Analysis of punch-through breakdown in bulk silicon RF power LDMOS transistors" *J Microelectronics Reliability*, v 48, n 2, p 173-180, 2008

[9] I. Cortés, P. Fernández-Martínez, D. Flores, S. Hidalgo, J. Rebollo, "Analysis of trench gate power LDMOS transistors in thin SOI technology", *13th In.t Symp. on Silicon-On-Insulator Technology and Devices (ECS Transactions)*, v 6, n 4, p 191-96, 2007

[10] Gordon Ma, Qiang Chen, Olof Tornblad, Tao Wei, Carsten Ahrens, Rolf Gerlach, "High frequency power LDMOS technologies for base station applications status, potential, and benchmarking", *in Int. Elec. Dev. Meet.(IEDM)*, p 361-64, 2005

[11] G. Charitat, M.A. Bouanane, P. Austin, and P. Rossel, "Modelling and improving the on-resistance of LDMOS RESURF devices" *Journal Microelectronics*, v 27**,** n 2-3, p181-190, 1996

[12] M. Yuto, C. Ping, L. Hancheng, M. James, et al.," Compact Model for LDMOS for circuit simulation" *8th ICSICT-2006*, p 1380, 2007

[13] A. J Apples, G. M. Collet, A. P Hart, M. H. Vaes, et al. "Thin layer high-voltage devices (RESURF devices)" *Journal Philips*, v 35, n 1, p 1-13, 1980

[14] Cheolhyum LIM, Junichi Hanna,“ Improvements in electrical characteristics of plasma enhanced chemical vapour deposition – Tetraethylorthosilicate-SiO2 by atomic hydrogen passivation via hot wire technique” *Japanese Journal Applied Physics*, v 45, n 48, p L1270-72, 2006

[15] Sun Lingling, and Chen Xiane, “Load-pull simulation for large signal GaAsFET” *4th Int. Conf .on Solid-State and Integrated Circuit Technology*, p 601-3, 1995

[16] P. A. Blackey, M. G. Khazhinsky, and G. H. Loechelt, “Direct Numerical Simulation of the Large-Signal RF behavior of Power Transistors,” *Proc. EDMO’96*, p 14-19, 1996

[17] G. H. Loechelt, and P. A. Blakey, “A Computational Load-Pull System for Evaluating RF and Microwave Power Amplifier Technologies,” *IEEE MTT-S Dig.*, v 1, p 465–468, 2000

[18] R. Jonsson, Q. Wahab, S. Rudner, and C Svensson, “Computational load pull simulations of SiC microwave power transistors,” *Journal of Solid-State Electronics*, v 47, p 1921-1926, 2003

[19] O. Bengtsson, L. Vestling , J. Olsson, “ A computational load-pull method with harmonic loading forhigh-efficiency investigations” *Journal of Solid-State Electronics*, v 53, p 86–94, 2009

[20] S. A. Maas, “How to model intermodulation distortion” *IEEE Microwave Symposium Dig. (MTT-S)*, p 149-52, 1991

[21] Q. Hao, J. Benedikt, and P. Tasker, “A novel approach for effective import of nonlinear device characteristics into CAD for large signal power amplifier design” *IEEE Microwave Symposium Dig. (MTT-S)*, p 477-80, 2006

[22] W.R Curtice, J.A. Pla, D. Bridges, T. Liang, E.E. Shumate, “A new dynamic electro-thermal nonlinear model for silicon RF LDMOS FETs” , *IEEE Microwave Symposium Dig. (MTTS)*, p 419-22, 1999

[23] R. Van Langevelde, L.F. Tiemeijer, R.J.Havens, M.J. Knitel, R.F Roes et al. “*RF*-distortion in deep-submicron CMOS technologies” *IEEE Electron Device Meeting (IEDM)*, p 807-10, 2000

[24] A. Sheikh, C. Roff, J. Benedikt, Paul J. Tasker, B. Noori, J. Wood, et al. “Peak class F and inverse class F drain efficiencies using Si LDMOS in a limited bandwidth design”, *IEEE Microwave and Wireless Components Lett*., v 19, p 473-75, 2009

[25] J. Kim, J. Moon, S. Hong and B. Kim. “A highly efficient class-F power amplifier for wideband linear power amplifier applications”, *Microwave and Optical Technology Let.*, v 51, p 2323-26, 2009

[26] F. M. Ghannouchi, and M. M. Ebrahimi, and M. Helaoui, “Inverse class F power amplifier for WiMAX applications with 74 % efficiency at 2.45 GHz” *IEEE Int. conf. on Communications Workshops*, p 1-5, 2009

[27] F. Raab, Class-E, Class-C, and Class-F power amplifiers based upon a finite number of harmonics, IEEE *Trans Microwave Theory and Tech.*, v 49, pp. 1462-68, 2001.

[28] P. Colantonio, F. Giannini, G. Leuzzi, and E. Limiti. On the class-F power amplifier design, *Int. J. RF and Microwave Computer Aided Eng.*, v 9, pp. 129-149, 1999

[29] A. Inoue, A. Ohta, S. Goto, T. Ishikawa, and Y. Matsuda, "The efficiency of class F and inverse class F amplifiers", *IEEE MTT-S Dig.*, p 1947-50, 2004

[30] S. Azam, C. Svensson, and Q. Wahab, "Pulse input class C power amplifier response of SiC MESFET using physical transistor structure in TCAD" *Journal of Solid-State Electronics,* v 52, p 740–44, 2008

[31] S. Azam, R. Jonsson, C. Svensson and Q. Wahab, *Microwave Journal*, v 53, p 184-192, 2010

[32] T. K. Quach, P. M. Watson, W. Okamura, E. N. Kaneshiro, A. K. Oki, D. Sawdai, R. D. Worley, " ultrahigh-efficiency power amplifier for space radar applications. *IEEE Journal Solid State Circuit*, v 37, p 1126, 2002

[33] Z. Lei, A. Pavio, B. Stengel, and B. Thompson, "A 6 watt LDMOS broadband high efficiency distributed power amplifier fabricated using LTCC technology" *IEEE Microwave Symposium Dig. (MTT-S)*, p 897, 2002

[34] H. E. Mokari-Bolhassan, and W. K. Wong "Design and analysis of large signal microwave power amplifiers", *Int. Symposium on Circuit and Systems (ISCAS)*, p 2231- 34, 1989

[35] H. Zhang, H. Gao, and Li Guann- Pyng "A Novel Tunable Broadband Power Amplifier Module Operating from 0.8 GHz to 2.0 GHz" *IEEE Microwave Symposium Dig. (MTT-S)*, p 661-4, 2005

[36] H. Katta, H. Kurioka, and Y. Yashima, "Tunable Power Amplifier Using Thin-Film BST Capacitors" *IEEE Microwave Symposium Dig.(MTT-S)*, p 564-67, 2006

[37] P. Colantonio, F. Giannini, and L. Scucchia "Matching network design criteria for wideband high-frequency amplifiers" *Int. Journal of RF and Microwave Computer-Aided Eng.*, v 15, pp. 423, 2005

[38] C. D. Shih, J. Sjöström, R. Bagger, P. Andersson, Y. Yu, G. Ma, Q. Chen and T. Åberg. "RF LDMOS power amplifier integrated circuits for cellular wireless base station applications" *IEEE Microwave Symposium Dig. (MTT-S)*, p 889-92, 2006

[39] F. M. Ali Al-Rai "A systematic technique for the designing of wideband RF Power amplifiers" *IEEE Int. RF and Microwave Conf.*, p 39- 42, 2006

Chapter 5

Conclusion

LDMOS transistors are considered important device in wireless communication technology for power amplification. It will be remaining in future due to mature silicon technology, and cost-effective solution.

We optimized intrinsic physical structure of LDMOS transistor in TCAD, and obtained promising results to enhance the performance of LDMOS devices. The optimization was made by introducing the excess interface charges at the RESURF of LDD region, which is also compared with a famous dual-layer surface doping technique (other parameters and dimensions were the same). 60 % additional enhancement is observed in our optimized LDMOS transistor. The reason is surface doping technique needs an implanted dose with specific thickness according to Gaussian phenomena while in case of interface charges, a thin depletion layer is created at the RESURF. Thus interface charges are more effective than additional n-type implanted dose in LDD region.

The CLP simulation technique in TCAD is a novel way to study the *RF* analysis of the transistor for PA design. It provides extraction of impedances of the active device without including any parasitic effects, and helpful for PA designers to match the device properly. Therefore, it can be used to design narrowband, tunable and broadband matching networks. CLP simulation technique is extended to study the non-linear behavior of *RF*-power transistors under a real large signal operation. Through this the non-linear capacitances of the device are simulated directly as a load. The CLP

technique is also further extended to understanding of transistor behavior for high efficiency PA operations, such as class-F. Through these, *RF*-transistor's response can be studied at different frequencies, and bias points for optimal performance. These CLP techniques provide an initial ground work to understand the mechanisms of new and fabricated *RF* transistors to improve over-all performance of the system.