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Optimization of MDP, Mask Writing, and Mask Inspection for Mask Manufacturing Cost Reduction

Masaki Yamabe, Mask Design, Drawing, and Inspection Technology Research Department (Mask D2I), Association of Super-Advanced Electronics Technologies (ASET), Tokyo Dia. Bldg. 1/8F, 1-28-38 Shinkawa, Chuo, Tokyo 104-0033, Japan**; Tadao Inoue,** SII NanoTechnology Inc., Tokyo, Japan**; Masahiro Shoji,** NIPPON CONTROL SYSTEMS CORP., Tokyo, Japan**; Akio Yamada,** ADVANTEST CORP., Tokyo, Japan**; Hiromichi Hoshi,** JEOL Ltd., Tokyo, Japan**; Kenichi Takahara,** NuFlare Technology, Inc., Yokohama, Japan

ABSTRACT

As the feature sizes of LSI become smaller, the increase in mask manufacturing time (TAT) and cost is becoming critical and posing challenges to the mask industry and device manufacturers. In May 2006, ASET Mask D2I launched a 4-year program for the reduction in mask manufacturing TAT and cost, and the program was completed in March 2010. The focus of the program was on the design and implementation of a synergetic strategy involving concurrent optimization of MDP, mask writing, and mask inspection. The strategy was based upon four key elements: a) common data format, b) pattern prioritization based on design intent, c) an improved approach in the use of repeating patterns, and d) parallel processing. In the program, various software and hardware tools were developed to realize the concurrent optimization. After evaluating the effectiveness of each item, we estimated the reduction in mask manufacturing TAT and cost by the application of results obtained from the Mask D2I programs. We found that mask manufacturing TAT and cost can be reduced to 50% (or less) and to about 60% respectively.

1. Introduction

As the feature size of LSI becomes smaller, the increase in mask manufacturing time (TAT) and cost is becoming critical and posing challenges to the mask industry and device manufacturers. These increases are caused by the increase in the number of patterns on the mask, and to

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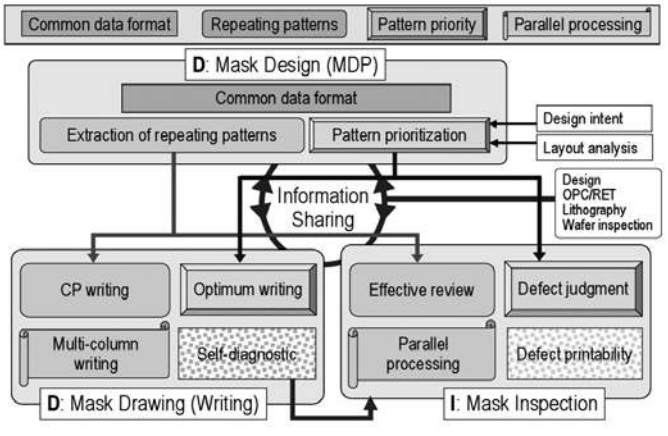

Figure 1. Interaction and synergy of four key items

TAKE A LOOK INSIDE:

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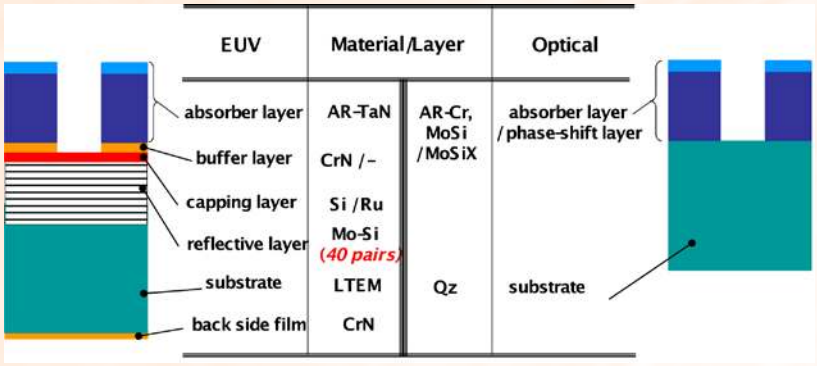
EDITORIAL

"EUV mask readiness in 2013"

Naoya Hayashi, Dai Nippon Printing Co., Ltd.

EUV Lithography expected to be used in production earliest at 2013. There are several issues to be solved by that time. Based on the survey results of EUVL Symposium since 2005, "EUV mask readiness" was always one of the top three focused items for the pilot line in 2011/2012 and high volume manufacturing in 2013. Most recently, "defect control" of EUVL mask has been the most important issue. The printability of the defect may be critical according to the superior resolution of EUVL. In ITRS mask table, the size of the defect which should be detected and removed will be 25nm in 2013. Currently, there is no solution exist to detect all printable defects on EUVL mask with this size. We definitely need the eye to see such the critical defect to control and improve it. So that, "EUV Mask Infrastructure" development program called EMI has been launched by SEMATECH to accelerate the development and to release the practical defect inspection tools in time. A Japanese consortium is also considering the EUVL mask infrastructure development program including various types of defect inspection tools.



The main technical barrier for the defect control of EUVL mask is the complexity of its structure. Compared with optical mask blank, EUVL mask blank has the excessive number of materials and stack of layers. In general, the optical mask blank consists of only 2-3 layers of absorber and/or phase-shifting material with Qz substrate. On the other hand, EUVL mask blank has maximum 8 different materials and more than 85 layers, consisting of absorber layer, buffer layer, capping layer, reflective layers (40 pairs of Mo/Si, total 80 layers!!), on the low thermal expansion material with thin metal conductive layer on the back side. Based on several researches, printable defect of the blank was originated from pit and/or bump defect on the substrate surface during polishing, and reflective layer deposition on those defects will make so called "phase defects" which will be strongly printable rather than particles on the mask surface. The substrate polishing and cleaning technologies have been improved through several development activities, such as SEMATECH's MBDC, to reduce such pit and/or bump defect. However, there may be the chance to get particle during deposition of reflective layer and/or other functional layers, and substrate handling during blank manufacturing processes. Do you really believe that we can get 25nm defect free EUVL mask blank in 2013? May be not. Recent report shows that a single-digit number of defect may be mitigated with shifting the patterns to cover the defects by the absorber material. How about the yield of the EUVL mask blank with only a single-digit number of defect? May be very low. Then, we should accept the risk of certain printable defects and consider how to mitigate those by further defect control and repair technologies with appropriate defect inspection tools.

At the 18th Photomask Japan, which will be held from April 13th to 15th, we will have a panel discussion titled, "EUV mask readiness in 2013", to discuss about defect specifications, readiness of inspection tools, and defect mitigation and repair technologies, to clarify the realistic EUVL mask solution in 2013. There will be the panelists from blank suppliers, consortia, inspection tool vendor, and EUVL users. We expect very interesting panel, so let's join the discussion at there!

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Managing Editor/Graphics Linda DeLano
Advertising Al Ragan
BACUS Technical Group Manager Pat Wight

SPIE

P.O. Box 10, Bellingham, WA 98227-0010 USA
Tel: +1 360 676 3290 or +1 888 504 8171
Fax: +1 360 647 1445
SPIE.org
customerservice@spie.org

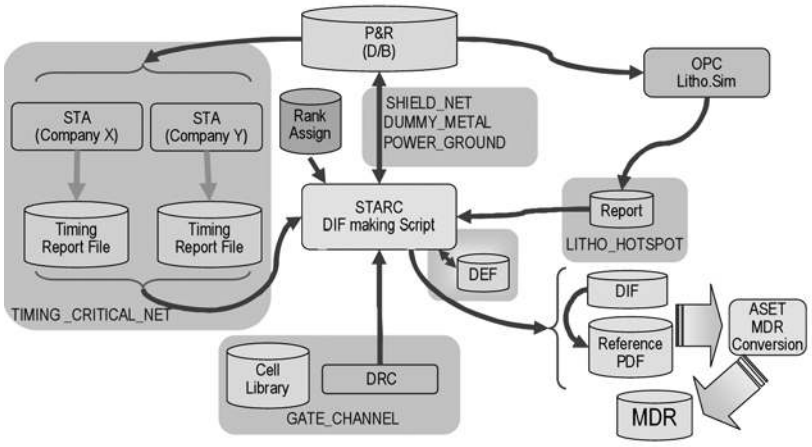


Figure 2. DIF extraction and MDR conversion flow.

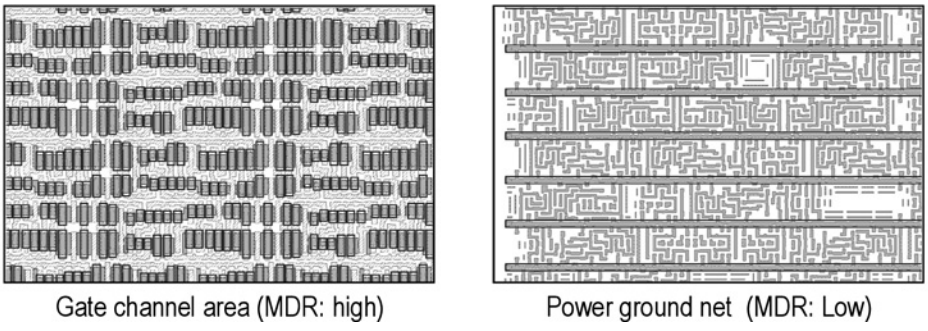


Figure 3. Examples of MDR.

a greater extent by the increase in the number of OPC artifacts, etc. to perform low k1 lithography. In May 2006, the Mask Design, Drawing, and Inspection Technology Research Department (Mask D2I)[1] of ASET launched a 4-year program for reducing mask manufacturing TAT and cost, and the program was completed in March 2010 as scheduled.

The program focused on the design and implementation of a synergetic strategy involving concurrent optimization of MDP, mask writing, and mask inspection. The strategy was based upon four key elements: a) common data format, b) pattern prioritization based on design intent, c) an improved approach in the use of repeating patterns, and d) parallel processing.

In this program, software and hardware tools were developed in order to realize the concurrent optimization based on the four key elements mentioned above. Furthermore, the effectiveness of the concurrent optimization strategy was evaluated on the basis of TAT reduction and cost reduction.

In this paper, the strategy of ASET Mask D2I, its activity, and results are presented.

2. Four Key Elements for the Optimization

We identified four key elements for the synergetic strategy involving concurrent optimization of the three stages of mask manufacturing, MDP, mask writing, and mask inspection. These four elements are: a) common data format for MDP, mask writing, and mask inspection, b) pattern prioritization based on the design intent, c) an improved approach in the use of repeating patterns, and d) parallel processing. Each of these four elements is designed to address all three manufacturing stages, namely MDP, mask writing, and mask inspection. Figure 1 shows the interaction and synergy of these three manufacturing stages with the above four elements.[2]

Mask pattern priority (we have adopted the term Mask Data Rank or MDR) is extracted from the original design, and used for the optimization of mask writing and mask inspection. Repeating patterns are extracted from mask pattern data and used mainly in CP (Character Projection) writing in the mask writing process. An MCC (Multi Column Cell) parallel writing system with CP writing function was developed for mask applications. Additionally, an integrated diagnostic system for the e-beam mask writer, and defect printability verification function for mask inspection were also developed.

3. Mask Data Rank (MDR) and its Utilization

The motivation behind MDR is that all mask patterns should not be judged under the same set of rules, since such an approach can be an over-kill. We regard the principle of pattern prioritization as a kind of DFM. In a broader context DFM serves as feed backs from manufacturing to design and vice versa. We treat feed-forward flow as a sub-routine of Mask DFM and call it Design Aware Manufacturing or DAM. DAM is considered as a tool that reduces mask manufacturing load, and makes the job simpler and faster. Our idea of pattern prioritization is to construct a feed-forward flow of design intents to make the manufacturing of mask more efficient.[3]

We designed a format for MDR based on OASIS format. Here the

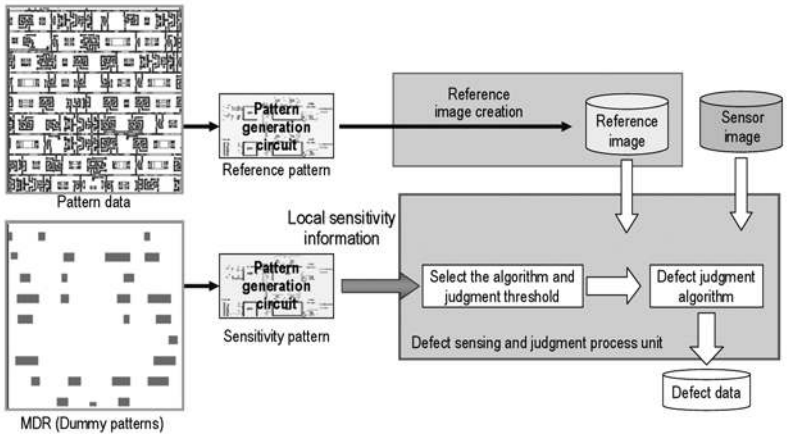


Figure 4. Mask inspection flow utilizing MDR.

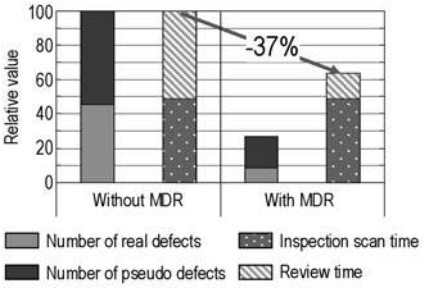


Figure 5. Reduction in the number of defects and inspection time by using MDR (45nm Logic, Metal 2 layer).

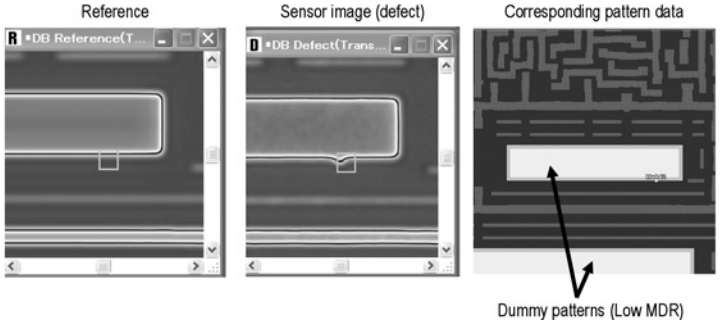


Figure 6. Mask pattern defect on dummy pattern edge.

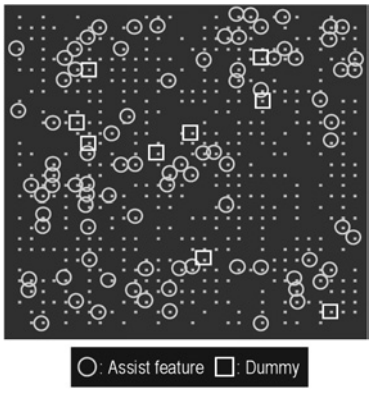


Figure 7. Decrease of the number of defects by using MDR and layout analysis (Defects with square mark [9 defects] are on dummy pattern edge and defects with circle mark [88 defects] are on assist feature. They can be treated allowable.)

MDR data is retained as a side file and the priority is expressed as polygon records with data type values, which identify the criticality of the areas. The specification of MDR format will soon be posted on ASETwebsite.[4]

3.1 Extraction of design intents and its conversion into MDR

In order to realize the feed-forward flow of the design intents to MDR, we constructed software tools in collaboration with Semiconductor Technology Academic Research Center (STARC), a research consortium for SoC design technologies in Japan. Figure 2 shows a developed flow. First, we make design intent files (DIF) from the output of commercial EDA tools. Shield, dummy metal, power net, and ground net are then extracted from the output information of P&R tool. Timing critical net is extracted from the output of the timing report of STA tool. Also, gate channels are extracted from DRC tool. The DIF files and reference pattern data files are input to MDR converter that creates MDR. Figure 3 shows examples of the extracted MDR.

3.2 Utilization of MDR in mask writing

In mask writing, MDR is used to optimize writing conditions such as beam settling wait time and maximum beam size to reduce the writing time and to reduce shot count. For low MDR mask patterns (low priority), we can shorten the beam settling wait time and use larger maximum beam size, since these treatments would reduce mask writing time. In order to realize variable beam settling wait time in mask writing e-beam tool, we developed a beam settling time selector circuit for the mask writing tool. The circuit selects a pre-determined beam settling wait time depending on input MDR and deflection distance, etc. Beam settling wait time is experimentally determined by the behavior of beam position measured by the output signal of deflection amplifiers. For example, beam settling wait times for MDR A (high priority), MDR B (medium priority), and MDR C (low priority) at 2um sub deflection are classified as 45ns, 62ns, and 85ns respectively. The wait times become longer as the deflection distance increases. At 10um deflection the wait times become 69ns, 160ns, and 290ns respectively. As for maximum beam sizes for each MDR, we determined them considering beam blur caused by Coulomb effects of e-beam.

We evaluated the effectiveness of MDR in mask writing by simulation. For the evaluation, we used 45nm Logic data. Unfortunately, shot count reduction and writing time reduction by using MDR was less than 10%. We believe that many smaller shots generated by aggressive OPCs obscured the effectiveness of MDR in mask writing.

3.3 Utilization of MDR in mask inspection

In mask inspection, MDR is used to set local sensitivity information.[5] Depending on MDR and sensitivity, to be concrete, defect

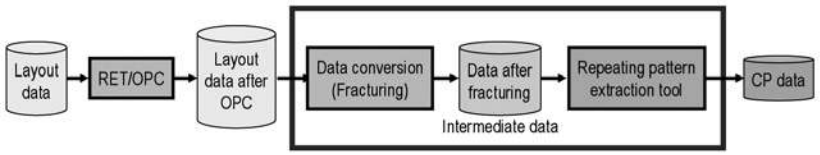


Figure 8. Repeating pattern (CP) extraction flow.

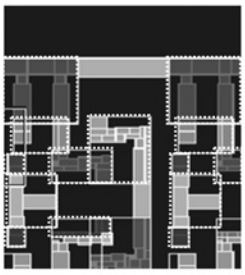


Figure 9. Example of CP extraction (Dotted squares are CPs. They are overlapping.).

judgment threshold and algorithm are changed locally. For low MDR mask patterns, lower sensitivity is selected. To realize this function in mask inspection tool, we developed a multilayer database pattern generator that can treat MDR data as well as other input pattern data. In the pattern generator, results from a layout analyzer are treated in the same way as MDR is. This treatment is especially useful to identify assist features and critical regions that are not expressed in design intents. Figure 4 shows a mask inspection flow utilizing MDR.

We evaluated the effectiveness of the utilization of MDR in mask inspection. First, we estimated the reduction of the number of detected defects (real defects and pseudo defects) and inspection TAT by an empirical method. In the evaluation, we used 65nm Logic patterns and 45nm Logic patterns. We assumed 2-hour inspection scan time and 30- second review time for each real defect, and 60-second review time for each pseudo defect. Numbers of real and pseudo defects are empirically estimated by the observation of mask patterns. Figure 5 shows one of the evaluation results. In this case, number of real defects and pseudo defects is greatly reduced by using MDR, and review time is also greatly reduced. Next, we checked the effectiveness of MDR in mask inspection by using an actual mask with programmed defects. We made masks for 45nm Logic with programmed defects (80nm to 120nm in size on mask). Figure 6 shows an example of a defect at the edge of a dummy pattern that is ranked to low MDR, and hence low inspection sensitivity is applied. Figure 7 shows a defect map of a mask. Defects with square marks are on the dummy pattern edge and defects with circle marks are on the assist feature patterns, and these can be treated as allowable defects. In this case, 97 defects among 521 defects were allowable.

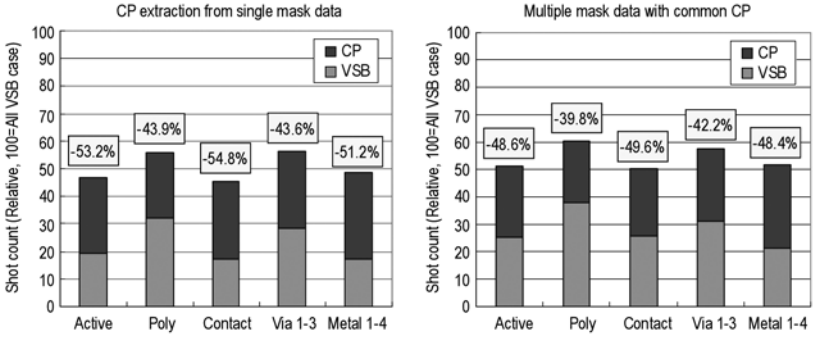


Figure 10. Shot count reduction by CP writing (Average).

3.4 Design intents of analog circuit

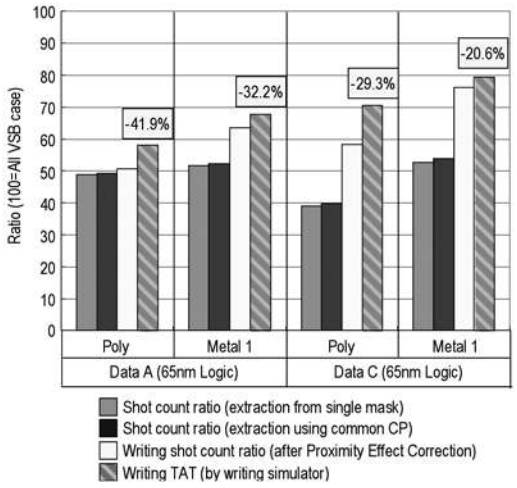
In recent days analog circuits of LSI require higher accuracy in manufacturing where the necessity of design intent utilization has been increasing. From this point of view, we developed a method to extract design intents from analog circuits and to send them to MDR in collaboration with The University of Kitakyushu. We paid special attention to transistor groups of current mirrors and differential pairs that needed higher relative accuracy between them. In order to extract the design intents of these circuits, we developed two complementary methods. One of them is the extraction from schematics. In the extraction from schematics, candidates of current mirrors and differential pairs are extracted based on relationships of Gate, Vdd, and Gnd. These candidates include circuits other than the target, such as inverters. The other method is an extraction from the layout. In this method, we extract the target circuits from the regularity of the layout such as array structure and row-line structure. The result is also redundant. By comparing the result from schematic-base extraction and layout-base extraction, we can find the target circuits.

4. The Use of Repeating Patterns

Repeating patterns are mainly used for Character Projection (CP) mask writing. By using CP writing, shot count in mask writing can be reduced. We developed software tools that extract repeating patterns from mask pattern data. And, we evaluated how shot count and writing TAT can be reduced by CP writing. In mask writing tool technology we developed an e-beam writing system with CP writing function, and we evaluated the system by actual VSB / CP mixed writing.

4.1 Extraction of repeating patterns from mask pattern data after OPC

We developed software tools that extract repeating patterns from mask pattern data after OPC. CP writing is already used in e-beam direct writing (EBDW). CP data extraction in EBDW is downstream that starts from the cell library. In mask writing, however, this approach is difficult because there is a diversity in pattern shapes due to OPC, even if they happen to be the same cell in their original design. Figure 8 shows developed flow to extract repeating patterns from mask pattern data after OPC. In the flow, we extract repeating patterns from the data after fracturing.[6] In the tool, repeating patterns are searched by checking the identity of the combination of fractured polygons under the conditions of maximum square size surrounding the combination (CP size) and maximum opening ratio. Figure 9 shows an example of repeating pattern (CP) extraction. We also developed a software tool that enables common CP extraction from multiple mask data. In the flow, extracted CP pattern data from the multiple mask data are merged and CP pattern data, that has greater shot count reduction effects in multiple mask data, are selected as common CP. For new mask data, we can search CP based on the common CP that already exists. Next improvement in CP extraction is sample



CP extraction conditions

CP size	Max. number of CP	CP max opening ratio
2um	2,080	50%

Writing simulation conditions

Parameter	Value
Current density	24A/cm^2
Resist sensitivity	30uC/cm^2
Maximum shot size	1.3um
Shot waiting time	54ns

Figure 11. Shot count and writing TAT reduction by using CP (65nm Logic).

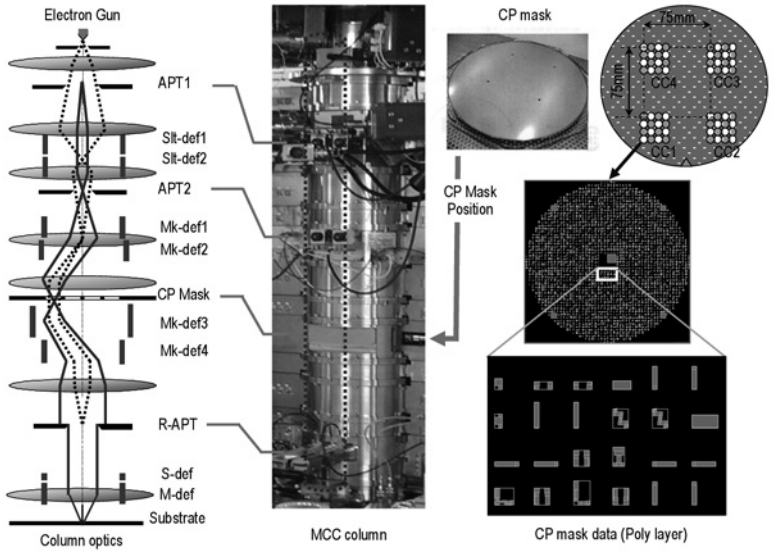


Figure 12. Optical structure of CP e-beam column and CP mask.

extraction. We found that the optimum CP size varies depending on the kind and the layer of the mask pattern data. To manage this issue, we developed a sample extraction method. In this method, CP extractions with different CP sizes are repeated for some sample areas in mask pattern, and CP size with best shot count reduction is selected as the optimum CP size.

4.2 Shot count and mask writing TAT reduction by using CP

Shot count reduction was examined by using actual Logic device data.[7] Data are 65nm Logic and 45nm Logic. Total number of chips was 25 and total number of layers was 155. Figure 10 shows averaged results of shot count reduction. For the CP extraction from a single mask, shot count reduction was 49% on the average. For the CP reduction using common CP, it was 46% on the average.

We evaluated mask writing TAT reduction by using 65nm Logic data. In this evaluation, we made an actual CP mask and mask writing data of 65nm Logic device. In the data flow, the disassembling of CP shot into VSB shots to correct proximity effect was taken into consideration. For the TAT evaluation, we used a writing simulator. This simulator is actually stage speed determination software of e-beam tool and gives precise TAT. Figure 11 shows the results along with CP extraction condition and simulation condition.

4.3 CP e-beam writing tool and writing results

A Proof-of-Concept (POC) system for CP ebeam writing was developed.[8] The CP writing function is developed as one function of Multi Column Cell parallel writing system that we discuss later in some detail. Figure 12 shows the optical structure of a CP e-beam column and a photograph of the column and schematics of CP mask. We made a CP mask of 65nm Logic device as shown in Figure 12. The mask has 2080 deflection selectable CP characters in an area.

In CP writing, there are mainly three issues to be addressed. They are focus shift caused by Coulomb effect of e-beam (current dependence), current density uniformity after character selection on CP mask (position dependence), and image distortion after character selection on CP mask (position dependence). To correct focus shift, we adopted a set of quadrupole focus electrodes and realized focus correction without beam position shift and beam astigmatism. Current density measurement after deflection for character selection showed current density variation of +/- 0.2% and this variation can be easily corrected by shot time control of the e-beam tool. Possible image distortions after character selection are isotropic and anisotropic magnifications, diagonal distortion, and rotation. Measured results of these distortions were below 2nm which happens to be within the permissible level.

We exposed 65nm Logic mask pattern by VSB and CP mixed exposure. Figure 13 shows the exposure results. Stitching error between VSB exposed part and CP exposed part was below 5nm.

5. Parallel Processing in Mask Writing

Parallel processing has been used in MDP process and data processing in mask inspection. In our Mask D2I program, we extended the parallel processing to mask writing. For this purpose, we developed a multi-column e-beam exposure system named “Multi Column Cell (MCC)” that is composed of four e-beam columns.[9] We checked the basic performance of the system and evaluated the writing TAT reduction by precise simulation.

5.1 Necessity of parallel mask writing

With the feature scaling and complex OPCs, shot count of mask writing goes up to hundreds of Giga shots, and writing time becomes much longer. There can be few approaches to manage the longer mask writing time. One is to increase the current density of the e-beam of the mask writing tool, and the other is to make beam-settling time shorter by a fast DACAMP. Our approach is to address this issue by utilizing CP writing mentioned earlier and apply parallel processing that is being addressed here.

In a sense, high-speed writing will be established if we can deliver more charge onto the writing substrate in shorter time. This means that we need a larger current. However, because of the increase

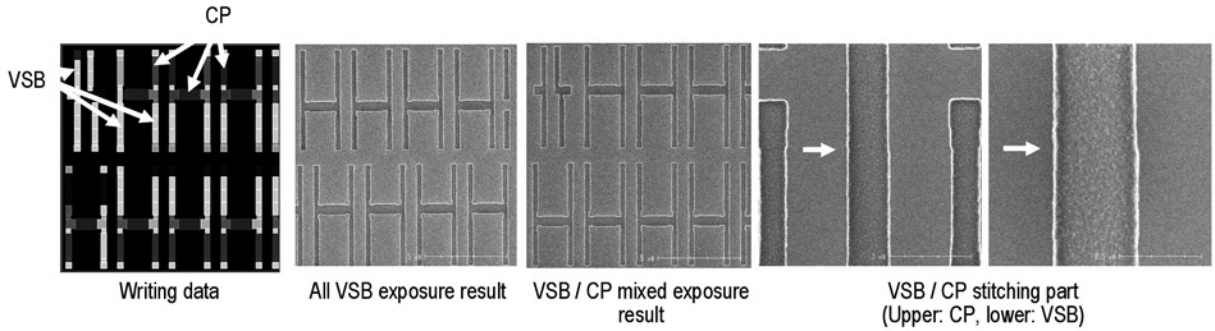
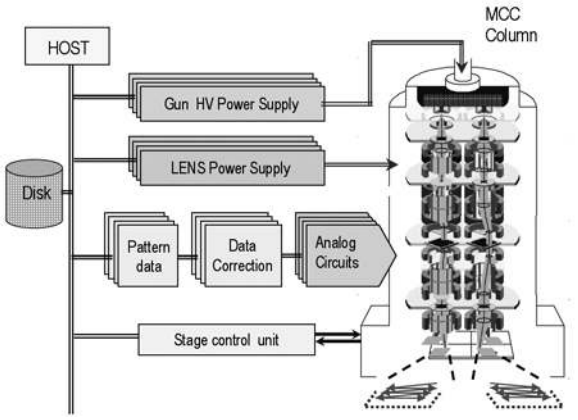


Figure 13. Exposure results of VSB / CP mixed exposure (CC-1 of MCC system. Similar results are obtained in other CCs.)



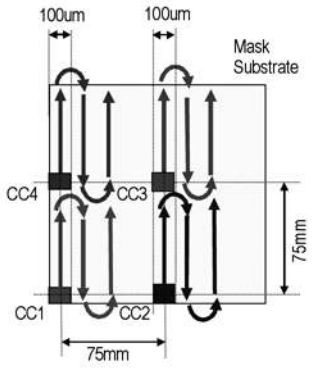


Table 1. Specification of MCC system.

Number of columns	4
Interval between column	75mm
Acc. Voltage	50kV
Current density	24A/cm^2
Main field size	100um
Sub field size	10um
Beam	CP and VSB
CP mask magnification	10 X
Mix. CP size on the substrate	2um sq.
Max. character number	2080

Figure 14. Outline of MCC system.

of beam blur at larger current, there is a limitation to how high the current can go. The objective behind parallel writing is to divide a total beam current into multiple beams with smaller currents. Parallel writing also has an advantage that it can share overhead time such as time taken by stage motion and beam settling time. There are two approaches to realize this objective. One is to divide the total beam current into massive parallel point beams like it is done in MAPPER[10] and PML2.[11] The other is to divide the total beam current into a limited number of Variable Shaped Beam (VSB) or CP beams. The latter is a simple extension of the current technologies where we can make use of the existing technologies that are well established. Because of this reason, we have chosen multi VSB / CP approach. We call our multi VSB / CP system as Multi Column Cell (MCC).

5.2 Multi Column Cell (MCC) parallel e-beam system

MCC is simply a bundle of single column VSB/CP systems as illustrated in Figure 14. Table 1 shows its specification. The MCC system has four column cells; each column cell has its own set of electron gun, lenses, blanking deflector, character selection deflectors, and exposure deflectors. Four columns are located at the interval of 75nm, and they write patterns simultaneously and independently. Figure 15 shows main units of MCC system and integrated system. The system is equipped with air-bearing / air-actuation stage.

5.3 Cross-talk between Column Cells

There are many issues with a parallel writing system. Among them, cross-talk between parallel beams would be most critical because if there is a cross-talk, accurate writing would be practically impossible. We checked the cross-talk of deflection in the MCC system. We applied a saw tooth deflection signal to X-direction main deflector of CC-2 and measured the beam position of CC-1 by knife edge method. We used FFT method to detect cross talk at higher sensitivity. FFT spectrum of knife edge signal in X-direction and in Y-direction did not have any peak corresponding to peak in the FFT spectra of applied signal, and this means that there is no cross-talk between CCs.

5.4 Basic performance of MCC system

We evaluated the basic performance of the MCC system. Figure 16 shows the resolution performance of the system. As shown in the figure, the MCC system has the resolution capability of 30nm in each CC. We also evaluated the main field stitching accuracy of the system. The main field stitching accuracy was about 7nm (3s) in single writing. The result of quadruple writings with different field boundaries was about 3nm (3s) (Figure 17). The stitching accuracy between the CCs was about 17nm (3s) in single writing case. We did not evaluate the image placement accuracy of MCC system, instead, we measured the overlay accuracy of the system. In the evaluation, all chip marks in the entire writing area (160mm by 160mm) were detected prior to the writing with corresponding CCs. So, the grid. The result was 3.5nm (3s) for both X and Y direction in quadruple writing.

5.5 Writing TAT reduction by MCC system

Writing TAT reduction compared with conventional single column system was investigated.[8] Table 2 shows a set of parameters for

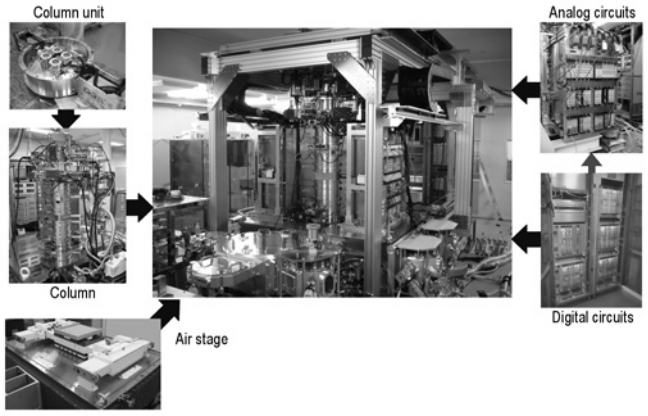


Figure 15. Main units of MCC system and integrated system.

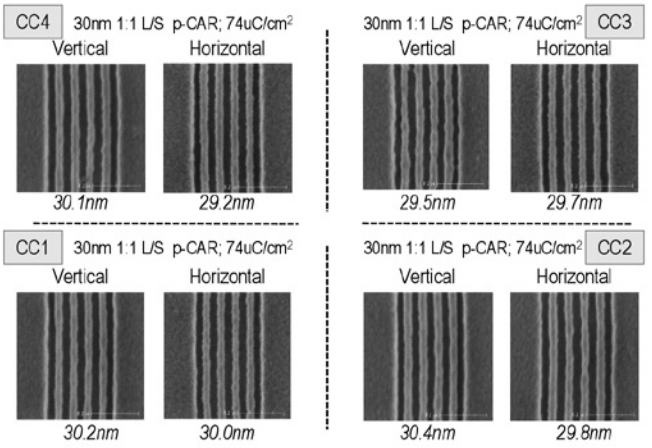


Figure 16. Resolution performance of MCC system.

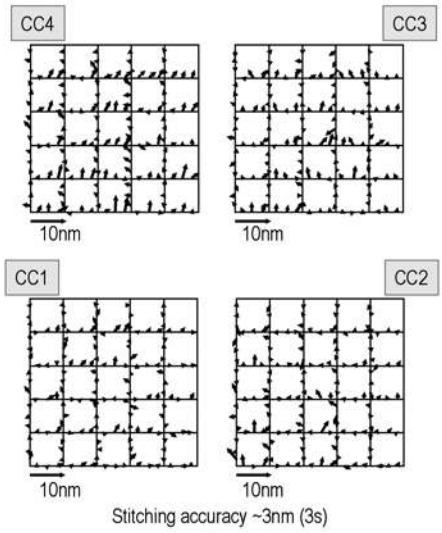


Figure 17. Main field stitching accuracy of MCC system (quadruple writings).

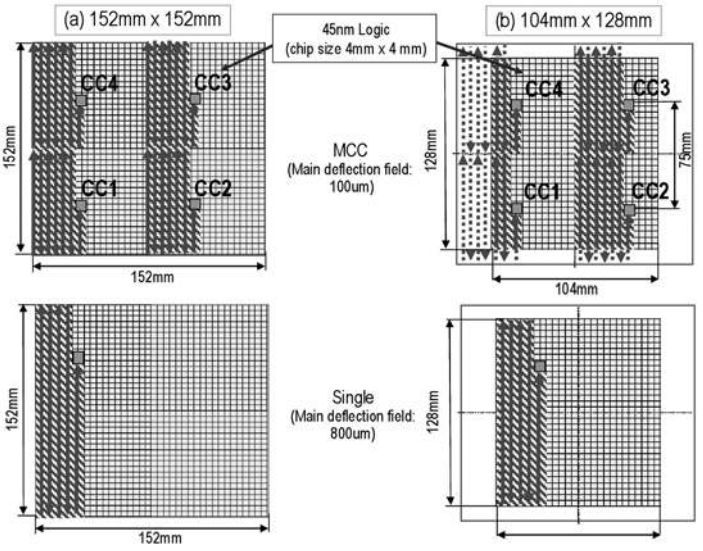


Figure 18. Relative motions between the column and substrate.

the comparison. The single column system in Table 2 corresponds to our conventional e-beam system where the field size is different from that of the MCC system. Furthermore, beam settling times of the two systems are not identical. The beam settling time of the MCC system is shorter than that of a single column system.

Figure 18 shows the relative motion between the column and a substrate during the on-the-fly (OTF) movement of the stage in the MCC system and single column system. The stage of the MCC system travels in a vertical direction along the stripes of about 75mm in length and 100um in width. At the end of the stripe it turns around after moving horizontally by an stripe width of 100um. The process continues until the stripe position has moved horizontally to about 75mm. In the single column system, the stage moves to cover the whole region of a substrate with the stripes of 800um in width.

We assumed two layouts in writing TAT simulation as shown in Figure 18. In the first layout, mask pattern of a 45nm Logic device with 4mm by 4mm was laid out in a 152mm by 152mm area (layout (a), total 38 x 38 = 1444 chips). In the other layout, same pattern was laid out in a 104mm by 128mm area (layout (b)). Using VSB writing data of the device pattern with a maximum shot size of 1um by 1um, we simulated the writing time by using writing simulator mentioned earlier in this paper. Shot count of M1 layer in layout (b) was 106.5 G shots. Figure 19 shows the simulated writing TAT ratio (MCC / single).

The ratio of layout (a) is about 1/4, which is the result of a fourfold increase of the number of column cells. In M1 layer and M2 layer the ratio is smaller than 1/4. That is because of the difference in beam settling time of the two systems. The ratio is about 1/3 for the pattern layout (b). On the marginal region of the layout (b) in Figure 18, CCs of the MCC system should wait without writing any patterns. On the other hand, the single column system can write without any wait.

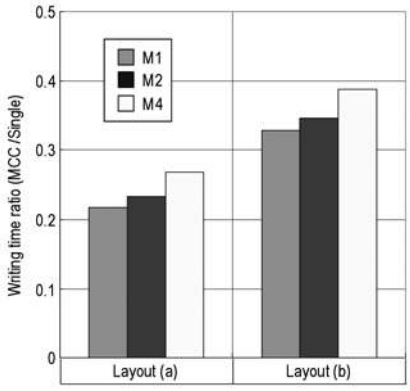


Figure 19. Writing time ration (MCC/Single).

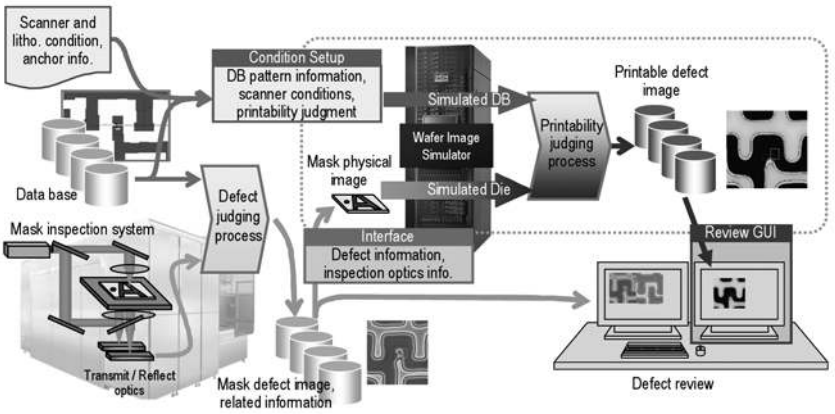


Figure 20. Outline of defect printability verification function.

Table 2. Parameter for writing TAT comparison.

	MCC	Single
Number of columns	4	1
Acc. Voltage (kV)	50	50
Current density (A/cm^2)	24 (for each CC)	24
Main field size (um)	100 x 100	800 x 800
Sub field size (um)	10 x 10	80 x 80
Exposure mode	VSB only	VSB only
Resist sensitivity (uC/cm^2)	30	30

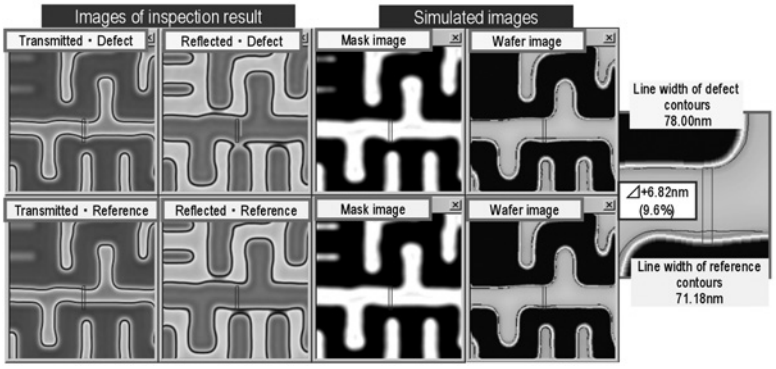


Figure 21. Printability evaluation example of an edge extrusion.

6. Defect Printability Verification Function in Mask Inspection

The shapes of mask patterns are becoming finer and more complex with the shrink of device pattern size. Moreover, extremely complicated mask pattern that is very different from designed pattern is beginning to appear. One example of such a mask is SMO (Source-Mask-Optimization) mask. In mask inspection, these complex masks result in a large number of defects including pseudo defects and it is becoming more difficult to judge whether detected defect is a real or pseudo defect. The idea of defect printability verification is to manage these issues by verifying the wafer printability of detected defects. In the Mask D2I program, we developed a defect printability verification function on a mask inspection system.[12] The function is lithography process simulator base. We evaluated the function through the inspection of actual masks and found that the function is very useful in mask inspection.

6.1 The outline of defect printability verification function

Figure 20 shows an outline of the defect printability verification function. The function is lithography process simulator base one. Mask inspection system performs the inspection in a normal way, where detected mask defect images and related information such as defect positions are stored. The mask defect image is handed to the simulator for the reconstruction of the mask physical image. This is system is not identical to the mask physical image because of the influence of optical system of the mask inspection system. Based on the reconstructed mask physical image, the simulator performs wafer aerial image simulation, and resist pattern simulation within the process windows. Using defect position data, the simulator reads data-base polygon data around the defect position and then generates wafer aerial image and resist pattern image as a reference in the same manner as that of the detected defect. Two kinds of simulated images are compared and the degree of image error such as CD change is measured. Based on the degree of image error we can judge the detected defect.

6.2 Evaluation of the defect printability verification function

We evaluated the defect printability verification function using 199nm mask inspection proto-type system that is being developed by NuFlare Technology, Inc. In the evaluation, masks of 45nm Logic device mentioned earlier in this paper were used.

Figure 21 shows the results of an edge extrusion defect. Images in the upper side of the figure show transmission defect image, reflection defect image, simulated mask physical image, and simulated wafer aerial image. Images in the lower side are the corresponding images of the references. We found that printed wafer linewidth at the defect position is 6.82nm wider than the reference. This corresponds to 9.6% linewidth error. Figure 22 shows an example of the negligible defects. Although the mask inspection system detected a defect on the mask, simulated linewidth change on wafer was 3.8nm (5%) which can be disregarded using 7% linewidth criteria.

Table 3 shows an example of defect elimination by the defect

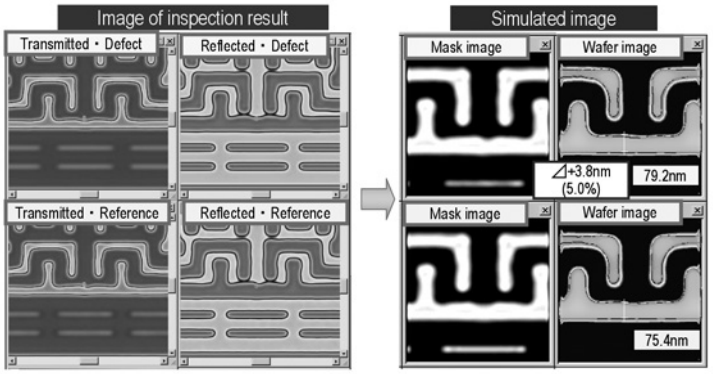


Figure 22. Example of a non-printable defect.

Table 3. Defect elimination by the defect printability verification (example).

	High sensitivity inspection result	Printability verification result (7% CD error)	
		Judged as printable	Judged as non printable
Real defect	81	38	43
Nuisance defect	5	1	4

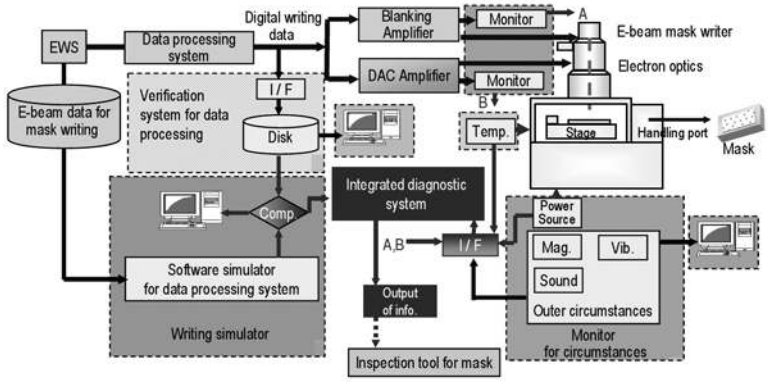


Figure 23. Outline of the integrated diagnostic system.

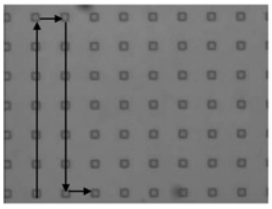


Figure 24. Pattern used in the evaluation (1um sq., 5um pitch pattern. Arrow shows writing sequence).

printability verification. In this case, 47 defects among 86 detected defects are judged as non printable defects by the verification.

7. Integrated Diagnostic System for E-Beam Mask Writer

In the Mask D2I program, we developed an integrated diagnostic system for e-beam mask writer.[13] This system detects data flow error in e-beam writer and monitors analog signals and circumstances around the e-beam writer. When error or change in circumstances occurs, the system records its type, occurrence time, and position of occurrence on the substrate. These records are retained as a log file and delivered to mask inspection tool. Depending on the severity of the event, we can select a next action, such as the suspension of mask writing or close inspection of corresponding position in mask inspection. We believe this system would be useful to identify the origins of writing error.

7.1 The outline of the integrated diagnostic system

Figure 23 shows an outline of the integrated diagnostic system for an e-beam mask writer. The system consists of a verification mechanism for data processing, exposure simulator, and monitoring for circumstances. The verification system for data processing collects and stores digital exposure data in an e-beam writer. On the other hand, "exposuresimulator" performs software simulation of the exposure data. Its result should be identical to the above mentioned digital exposure data. Both data are compared and the result is reported to the integrated diagnostic system. The system is equipped with a monitoring device to keep track of the surrounding circumstances such as temperature, magnetic field, vibration, and so on. It also monitors error in blanking amplifier and deflection amplifier. Error data is also reported to the integrated diagnostic system. The integrated diagnostic system outputs the error report to mask inspection system.

7.2 Evaluation of the integrated diagnostic system

We installed a developed system into a real mask writer and checked the functions of the system by applying intentional error or circumstance change. In the evaluation, we mainly used the pattern shown in Figure 24. While the ebeam writer wrote this pattern, we applied intentional change to the outer circumstances of the writer. Figure 25 shows the result of magnetic field detection test. In the test, we applied AC 50Hz magnetic filed shown in the left hand side of the figure. The center part of the figure shows the error field information and position on the job where magnetic field error occurred. The right side of the figure shows the results of coordinate measurement of the written patterns. Pattern position errors in Y direction were clearly observed at the position where the error occurred.

8. Mask MFG. TAT and Cost Reduction by the Results

The objective of the Mask D2I program is the reduction of mask manufacturing TAT and cost. In this session, we discuss how mask manufacturing TAT and cost can be reduced by applying the results of the program. In the estimation of TAT and cost reduction, we used a model that predicts mask manufacturing TAT and cost.

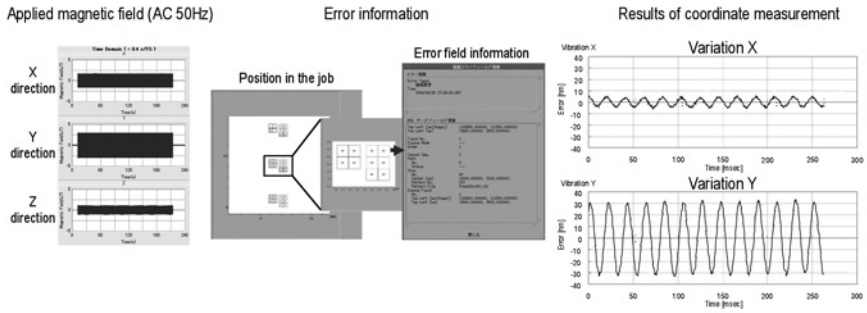


Figure 25. Monitoring of the influence of magnetic fields.

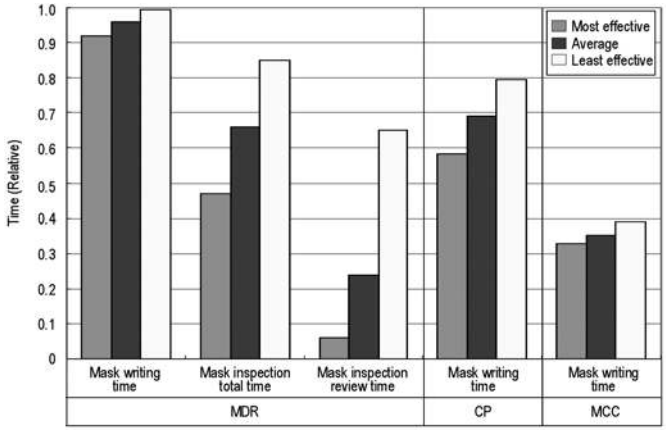


Figure 26. TAT reduction by each item.

8.1 Evaluation of the integrated diagnostic system

Figure 26 shows how time for mask writing or mask inspection is reduced by applying the results of the program. Each bar in the graph shows the time reduction when a corresponding item is applied individually. For the writing time reduction by MDR, we used the results of writing simulator for 45nm Logic device. For the inspection time (total time and review time) reduction, we used the empirical estimation mentioned above. For the writing time reduction by CP, we used the results of writing simulator for 65nm Logic device. For the writing time reduction by MCC, we used the results of writing time comparison mentioned above and assumed 104mm by 128mm layout. We found that MDR has a great effect in the reduction of mask inspection time. As for mask writing time reduction, MCC is most effective and CP is next in its effectiveness.

8.2 Model for mask manufacturing TAT and cost estimation

We used a model that expresses the mask manufacturing cost by the following equation.

[Mask mfg. cost] = [MDP cost] + {[Mask writing cost] + [Mask inspection cost] + [Mask process cost] + [Cost of mask substrate, etc.]} / [Yield]

For the cost relating to tools such as mask writing mask inspection, and mask process, we considered the depreciation of the tool, operating cost, maintenance cost, and time for the related work (writing, writing and mask inspection time, we assumed necessary time for 65nm Logic and assumed that the time changes as the device node changes. Figure 27 shows the shot count and mask writing time that we assumed. Figure 28 also shows our assumption of mask inspection time for three times inspections. In Figure 27 and Figure 28, estimated results, by applying the results of Mask D2I program, are also shown. We also assumed that at 65nm Logic, 60% of the total mask manufacturing cost is occupied by mask writing and mask inspection, 5% by MDP, and the rest by process and mask substrate.

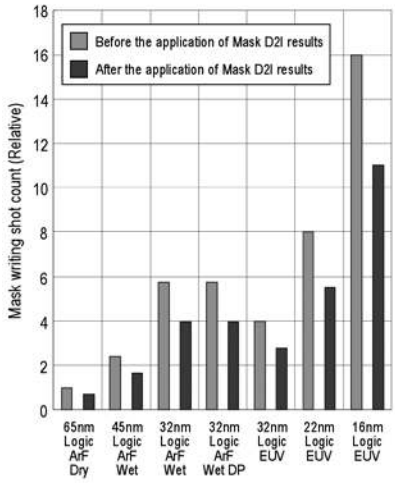
In the estimation of mask manufacturing TAT, we took into account only mask writing time, mask inspection time, and MDP time. This is because it was difficult to estimate other manufacturing related times. In our estimation, mask manufacturing time is expressed by the following equation.

[Mask mfg. TAT] = [MDP time] + {[Mask writing time] + [Mask inspection time]} / [Yield]

8.3 Mask mfg. TAT and cost reduction by the results

First, we estimated mask manufacturing TAT and cost without applying the Mask D2I program results for 65nm Logic and beyond. We assumed 193nm dry lithography for 65nm Logic, 193nm immersion for 45nm and 32nm Logic, 193nm immersion double patterning for 32nm Logic, and EUV lithography for 32nm, 22nm, and 16nm Logic.

Next, we estimated mask manufacturing TAT and cost after the application of the Mask D2I program results. In the estimation, we mainly used the average value of Figure 26. Other than the effectiveness shown in Figure 26, we assumed that data volume is reduced to 70%, yield is enhanced by 1.1, overhead time by using



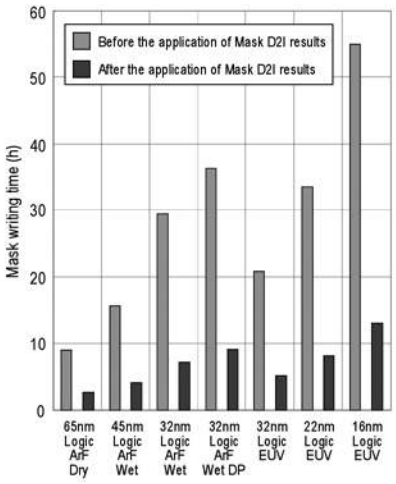


Figure 27. Shot count and writing time for mask writing (assumption).

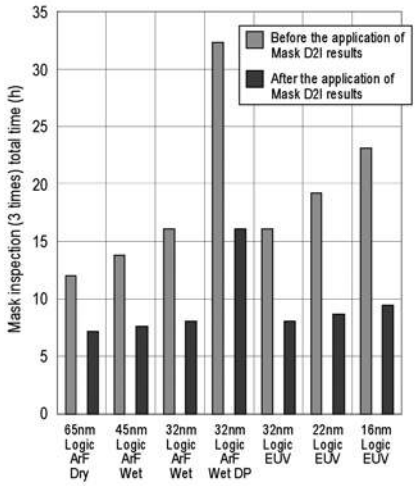


Figure 28. Mask inspection (3 times) total time (assumption).

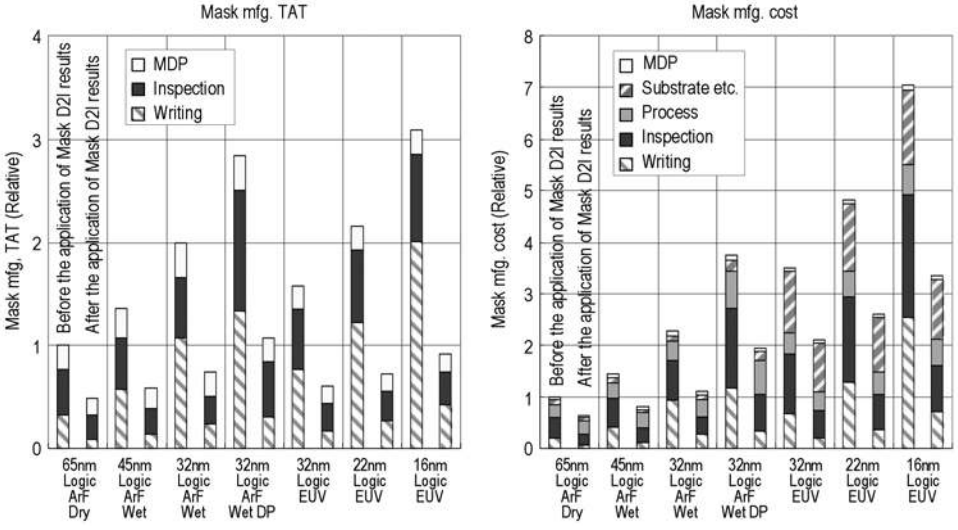


Figure 29. Mask mfg. TAT and cost before and after the application of Mask D2I results.

MCC becomes half, and mask inspection review time is reduced to 85% by the defect printability verification function.

Figure 29 shows estimated mask manufacturing TAT and mask manufacturing cost before and after the application of Mask D2I program results. We found that mask manufacturing TAT is reduced to 50% or below by the application of Mask D2I program results. We also found that mask manufacturing cost is reduced to about 60%.

9. Conclusion

ASET Mask D2I launched a 4-year program for mask manufacturing TAT and cost reduction in May 2006, and the program was completed in March 2010. The focus of the program was on the design and implementation of a synergetic strategy involving concurrent optimization of MDP, mask writing, and mask inspection. The strategy was based upon four key elements: a) common data format, b) pattern prioritization based on design intent, c) an improved approach in the use of repeating patterns, and d) parallel processing. In the program, software tools that extract design intents and convert them into MDR were developed. This is the realization of DAM (Design Aware Manufacturing) in mask area. Repeating pattern (CP) extraction tools and related software tools are also developed. As for the realization of parallelism in mask writing, we developed Multi Colum Cell (MCC) parallel e-beam writing system. We also developed the defect printability verification function in mask inspection and integrated diagnostic system for e-beam mask writers.

The effectiveness of these tools and our strategy of concurrent optimization were evaluated by using the actual device data. We found that MDR reduces mask inspection TAT to 65% on the average, CP reduces mask writing TAT to 70%, and MCC reduces mask writing TAT to 35%. Mask manufacturing TAT and cost estimation using a model showed that mask manufacturing TAT is reduced to 50% or below and the cost is reduced to about 60% by the application of Mask D2I program results.

10. Acknowledgments

This work was supported by NEDO. We are grateful to NEDO. In addition, we thank National Institute of Advanced Industrial Science and Technology (AIST), The University of Kitakyushu, MEIJO UNIVERSITY, Semiconductor Technology Academic Research Center (STARC), Advanced Mask Inspection Technology (AMiT) for their cooperation.

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Industry Briefs

Technology and Cost Considerations for HBLED Lithography

by **M. Ranjan, D. Anberg, W.Flack,** Ultratech Inc., San Jose. CA USA

High-brightness light-emitting diodes (HBLED) can provide cost reduction for solid-state lighting. Manufacturing enhancements are related to four to six lithography steps on sapphire wafers. Contact and proximity printers use a full wafer mask, the shadow of which defines the structure on the wafer. For an aligner, the mask to wafer gap is a compromise between near contact for best image quality and a large gap to minimize damage due to mask to wafer contact. Because the resolution for HBLED can be 5µm, the gap is typically set to ~10µm. 2-inch sapphire substrates can have 50µm bow as a result of the MOCVD in HBLED. As a result, the mask will contact the substrate across the wafer, producing defects. The present solution is to frequently clean the mask. Another important advantage of projection lithography steppers for HBLED is the ability to image on warped substrates. A projection system can re-focus from field to field, so the gap variations across the wafer can be eliminated, defects are not generated and the mask is never replaced. As warpage increases with wafer sizes, the ability to compensate for substrate warpage becomes more critical.

1X projection steppers can provide resolution down to 0.8µm. Two steps demonstrate the advantages of projection lithography. The first is a patterned sapphire substrate (PSS) step that acts as a reflector under the LED to increase the light extraction and consists of a repeating grid etched into the sapphire to scatter light. Its efficiency increases as the size of the grid is reduced to 1µm. The second step is a current spreading layer to enhance the brightness of the LED, with small widths to maximize the current injection area across the device while minimizing the area of the LED blocked by the current spreading structures. Projection lithography provides better CD control than a wafer aligner. CD uniformity for large 10µm features on Si wafers showed 2% variation for the 1X stepper and 6% for the wafer aligner. It provides better overlay than a full wafer aligner: 3-sigma 0.4µm for a 1X stepper vs. 2.0µm for the full wafer aligner. Because each field is independently exposed and aligned, a stepper can correct systematic errors such as grid and orthogonality.

ITRS 2010: What Happened During This Off-Year?

by **Laura Peters,** contributing editor

The year 2010 is an even-numbered year, so the update to the International Technology Roadmap for Semiconductors (ITRS) generally undergoes few changes, saving the major changes for odd-numbered years. Nevertheless, changes occurred in 2010, including boosts in the timelines for NAND flash and DRAM device rollouts, backup plans for lithography forced by EUV delay, impending device and interconnect structural changes, and progress in 3D packaging. When the roadmap committee talks about low power, they mean low. In 2010, in low-power logic, off-current Ioff is reduced from 50 pA/µm to 10 pA/µm. The power supply voltage (Vdd) was lowered to similar voltages as those of high-performance technology to reduce dynamic power. As a result, operating speed will be reduced by 20%-57%, but will still maintain adequate levels for operation. In the low power regime, Vdd has reduced speed by 14%-34%, yet still meets performance targets.

Half-pitch scaling was bumped up from 2011 to 2010 for NAND flash and DRAM. DRAM adoption of FinFET structures is delayed to 2012, vertical channels are expected in 2013, and the cell size change to 4F2 is delayed by two years. In flash memory, bit size accelerated by one year, while a transition to 3D stacking is delayed from 2014 to 2015. The change to 4 bits/cell, expected in 2012, is delayed until 2019. At 22 nm, flash memory will continue to use 193i with double patterning (DP) awaiting a mature EUV infrastructure. The key challenges for EUV remain: defect-free masks, adequate source brightness, and resist systems. Mask metrology for EUV is nonexistent. Looking forward, to surpass 16nm patterning capability, numerical aperture (NA) will have to be increased. Incidence angles may need to be increased, requiring thinner absorbers and mitigation of flare. The roadmap architects point out that scanner throughput has been increased dramatically, making double patterning more production worthy especially with registration and overlay also been improved. The roadmap further indicates that while flash manufacturers are likely to stick with 193nm immersion, logic and DRAM have time to consider the alternative NGL, including DP at k1 of 0.15 for 22nm half pitch, maskless lithography or imprint lithography, also facing infrastructure challenges.

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