Optimization of OFET Performance with Pentacene as Organic Material

Abhishek Singh[1], Manish Kumar Singh[2*]

[1,2*]Electronics Engineering Department, Harcourt Butler Technical University, Kanpur, UP, INDIA-208002

[*]Corresponding author's e-mail: manish.rs.mst14@iitbhu.ac.in

***Abstract*— Pentacene is widely used in organic transistors as an organic semiconductor material. The conductivity of pentacene is enhanced in recent days, which helps in improving the device characteristics of organic transistors providing additional benefit of low-cost and flexible devices. Modeling and simulation of such devices are constructive in analyzing device characteristics. Here, in this paper modeling and simulation of four different configurations of organic transistor – two on the basis of the bottom gate and two on the basis of the top gate – is done in order to analyze the transfer and output characteristics. Off current of 10^{-15} A, and low subthreshold swing of 0.347 V/decade was observed.**

Keywords*— *Flexible electronics, finite element modeling, top gate configuration, bottom gate configuration, organic transistors.

1. Introduction

Technology is enhancing at a rapid pace, and miniaturization of the devices is also done to build more compact products and to increase a more significant number of transistors on integrated circuits (ICs). Organic electronics have emerged in the last decade, and it has opened a new field of flexible electronics enabling a higher level of miniaturization compared to conventional electronics. Devices made in organic electronics provide certain extra features compared to conventional electronics such as – processing at low-temperatures, low cost, mechanical flexibility, high compatibility with various flexible substrates – glass, paper, plastic, and so on [1-6]. Here in this work, a comparison of organic transistors is made depending on various geometries of the organic transistors.

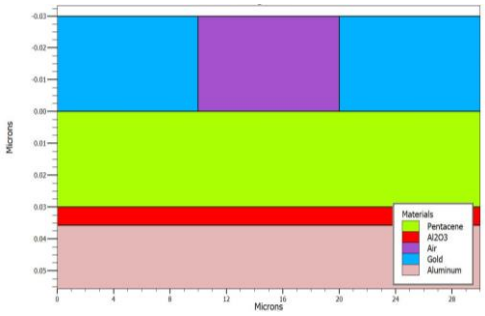
An organic transistor consists of organic semiconductor (OSC) material as an active layer material where channel formation takes place. Output current is modulated by varying the voltages applied across – source, drain and gate; thus, it's also known as the voltage-controlled current device. These transistors work in the accumulation mode of operation, and channel formation takes place due to the accumulation of the charges in the OSC material when the gate voltage above the threshold is applied. On the basis of, electrodes location with respect to OSC material and position of gate terminal in the device, these are classified into the top gate and bottom gate configuration devices [7-9].

Various OSC material that can be used in organic field effect transistors are – Tetracene, Anthracene, Rubrene, Fullerene, Pentacene, graphene and so on. Different materials provide variation in properties such as – compatibility level with various substrates, lab processability, environmental stability, mobility and so on [8]. Pentacene is lab processable, highly stable, provides high compatibility with flexible substrates and novel material like graphene, and has high hole mobility and due to these properties, it has been taken as active layer material here in modelling different device structures. Graphene can also be used as OSC material to obtain maximum current in the milliampere range and enhanced on/off ratio. Graphene is highly compatible with pentacene and it can be used along with pentacene forming hybrid OSC material [10-11].

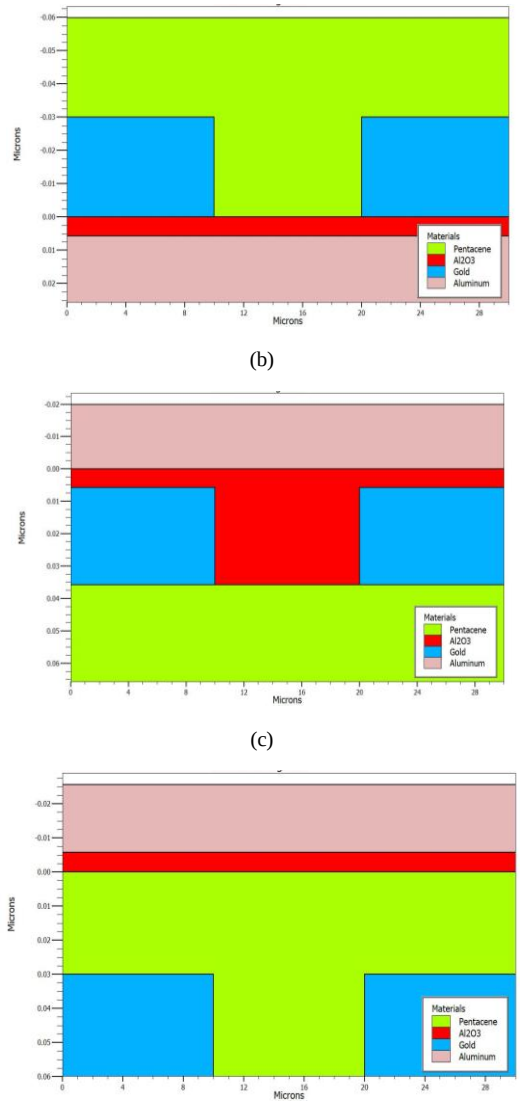
2. Structure of Device

Organic transistor or Organic field effect transistor (OFET) having gate terminal at bottom of device is known as bottom gate configuration of organic transistor. When, drain & source electrodes are placed at top of OSC material then it's known as top contact bottom gate device and when the drain & source electrodes are placed at the bottom of OSC material then it's known as bottom contact bottom-gate organic transistor.

In a similar way OFET having gate at top of device is known as top gate configuration and based on the location of drain & source electrodes with respect to OSC material; it is also further divided into top contact and bottom contact. Two-dimensional modulated device structure of all the four different device structure is shown below in figure 1.



(a)



(b)

(c)

(d)

Figure 1. Modulated two-dimensional device structures (a) Bottom gate top contact (BGTC), (b) Bottom gate bottom contact (BGBC), (c) Top gate top contact (TGTC), and (d) Top gate bottom contact (TGBC).

Modeling and simulation of these different device structures are done using SILVACO ATLAS TCAD tool, it consists of various models and here in this work Poole-Frenkel mobility model was used in tool. Pentacene was used as the active layer material in these organic transistors, and Aluminium dioxide (Al_2O_3) was taken as the dielectric material. Various parameters of modeling are listed in Table 1, and device specifications are listed in Table 2 [12-16].

TABLE 1. VARIOUS PARAMETERS OF MODELING AND SIMULATION

Parameters	**Values**
Effective density of states in conduction (N_c) & valence (N_v) band	1×10^{21} cm^{-3}
Bandgap at 300K	2.8 eV
Doping concentration	7×10^{17} cm^{-3}
Permittivity of pentacene	4.0
The work function of Au (Source & Drain)	5.1
Al work function (Gate)	4.28
Poole-Frenkel factor (hole)	7.75×10^{-5} $eV(cm/V)^{1/2}$
Zero field activation energy (hole)	1.79×10^{-2} eV

TABLE 2. VARIOUS DEVICE DIMENSIONS USED IN THE BOTTOM-GATE CONFIGURATION

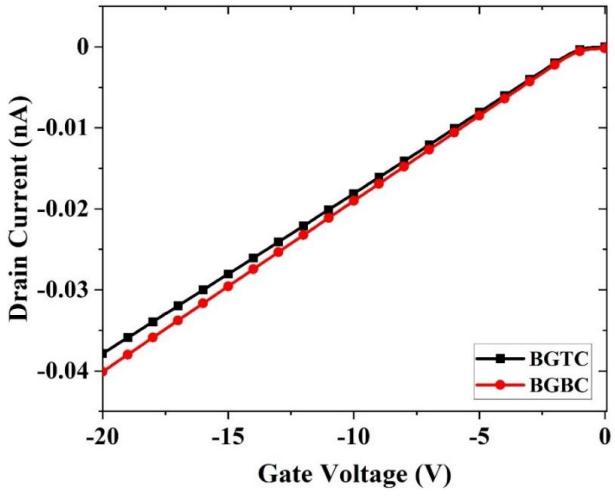
Dimensional Parameters	**Values**
Drain & source electrode thickness	30 µm
Gate electrode thickness	20 µm
Length of channel	10 µm
Width of channel	220 µm
Organic semiconductor thickness	30 nm
Dielectric thickness	5.7 nm

The transfer curve and output curve of the modeled device were obtained, and comparison was made for both the top and bottom gate configuration of devices.

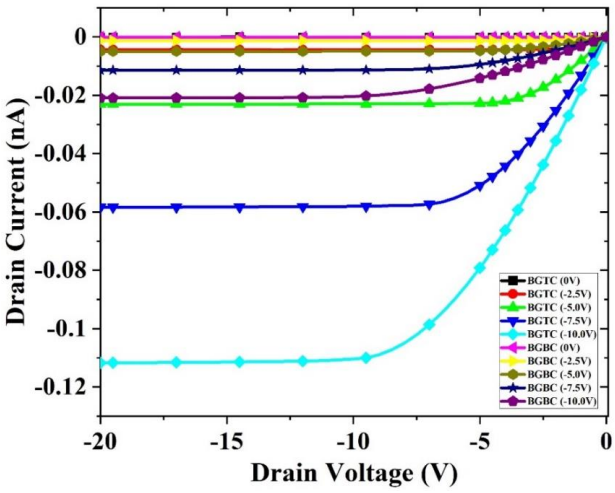
3. Results and Discussion

3A. Bottom gate configuration

Gate voltage was swept from 0V to -20V to obtain the transfer curve of both the device structures. The output curve was obtained by varying drain voltage from 0V to -20V and gate voltage variation from 0V to -10V having a step size of -2.5V. These curves are shown in figure 2.

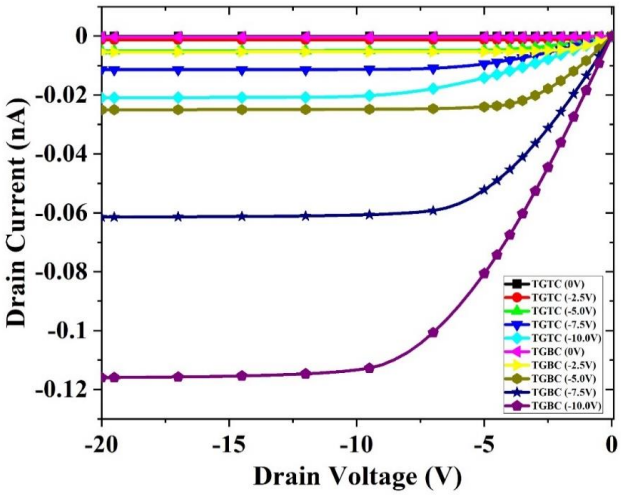


(a)



(b)

Figure 2. Electrical characteristics curves for bottom gate device configuration where BGTC is bottom gate top contact and BGBC is bottom gate bottom contact, (a) Transfer Curve, and (b) Output curve.



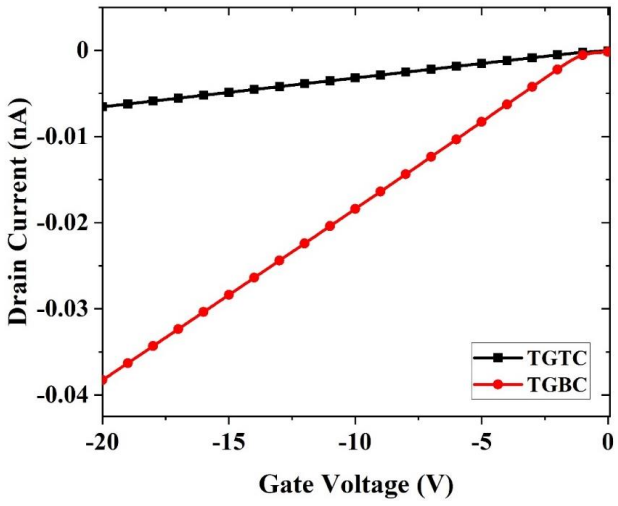
(b)

Figure 3. Electrical characteristics curves for top gate configuration where TGTC is top gate top contact and TGBC is top gate bottom contact, (a) Transfer curve, and (b) Output curve.

It can be seen clearly from figure 2 that curves obtained for both the configurations are approximately the same, but a slight variation is observed in both the curves and bottom gate bottom contact shows better results compared to bottom gate top contact device. This variation is due to the difference in the contact resistance of both device structures.

3B. Top gate configuration

Gate voltage was varied from 0V to -20V to obtain the transfer curve of both the structures. The output curve was obtained by ranging drain voltage from 0V to -20V and gate voltage variation from 0V to -10V having a step size of -2.5V. These curves are shown in figure 3.



(a)

Figure 3 clearly shows that there are variations in transfer curves and output curves. At lower voltage ranges, results obtained in both the configurations are approximately but, variations were observed at higher applied voltages. This variation in results is due to the device geometry and placement of the electrodes with respect to OSC material, which in turn affects contact resistance, affecting the overall performance of the device at a higher voltage range.

Various electrical characteristics observed in all the four different device configurations were recorded and are stated in table 3.

TABLE 3. ELECTRICAL CHARACTERISTICS OF VARIOUS DEVICE CONFIGURATIONS

Device Type	**Threshold Voltage (V)**	**I_{ON}**	**I_{OFF}**	**I_{ON}/I_{OFF}**	**Subthreshold swing (V/decade)**
Bottom gate top contact (BGTC)	-0.525	-3.785×10^{-11}	-5.424×10^{-15}	6.97×10^{3}	0.347
Bottom gate bottom contact (BGBC)	-0.494	-4.009×10^{-11}	-1.757×10^{-13}	2.28×10^{2}	1.314

Top gate top contact (TGTC)	-0.026	-6.545×10^{-12}	-3.796×10^{-14}	1.72×10^{2}	0.874
Top gate bottom contact (TGBC)	-0.423	-3.826×10^{-11}	-1.758×10^{-13}	2.17×10^{2}	1.318

Conclusion

After Modeling and simulation of various device structures were performed successfully, and it was observed that there was a slight variation in curves obtained in bottom-gate configurations at higher voltage range. However, in the case of top-gate configuration, there was slightly more variation at higher voltage range compared to that of lower voltage range. This variation was due to the different device geometry, as the device geometry/materials thickness plays a decisive role in the performance of electronic devices. Further, as per the requirement and application any suitable optimized geometry can be chosen and fabrication can be done.

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