Optimization on Layout Style of ESD Protection Diode for Radio-Frequency Front-End and High-Speed I/O Interface Circuits

Chih-Ting Yeh, Ming-Dou Ker, *Fellow, IEEE*, and Yung-Chih Liang

***Abstract*—The diode operated in forward-biased condition has been widely used as an effective on-chip electrostatic discharge (ESD) protection device at radio-frequency (RF) front-end and high-speed input/output (I/O) pads due to the small parasitic loading effect and high ESD robustness in CMOS integrated circuits (ICs). This work presents new ESD protection diodes drawn in the octagon, waffle-hollow, and octagon-hollow layout styles to improve the efficiency of ESD current distribution and to reduce the parasitic capacitance. The measured results confirmed that they can achieve smaller parasitic capacitance under the same ESD robustness level as compared to the stripe and waffle diodes, especially for the diodes drawn in the hollow layout style. Therefore, the signal degradation of RF and high-speed transmission can be reduced because of smaller parasitic capacitance from the new proposed diodes.**

***Index Terms*—Diode, electrostatic discharge (ESD), layout, radio-frequency (RF).**

I. Introduction

ELECTROSTATIC discharge (ESD) has become the major concern of reliability for integrated circuits (ICs) in nanoscale CMOS technology. The thinner gate oxide and shallower diffusion junction seriously degraded the ESD robustness of ICs and raised the difficulty of ESD protection design for ICs implemented in nanoscale CMOS technology [1]–[3]. In order to sustain the required ESD robustness, such as 2 kV in human-body-model (HBM) [4] and 200 V in machine-model (MM) [5], the on-chip ESD protection devices must be drawn with large enough device dimension. However, the parasitic loading effects of the ESD protection devices with large device dimension will obviously degrade the circuit performance of signal transmission, especially for radio-frequency (RF) front-end and high-speed input/output (I/O) circuits [6], [7]. In order to reduce the circuit performance degradation, the parasitic capacitance (C_{ESD}) of the ESD protection devices must be minimized, but the ESD robustness is still kept at the reasonable level [8]. ESD protection designs for RF front-end and high-speed I/O interface circuits must be optimized with consideration of parasitic capacitance and ESD protection capability.

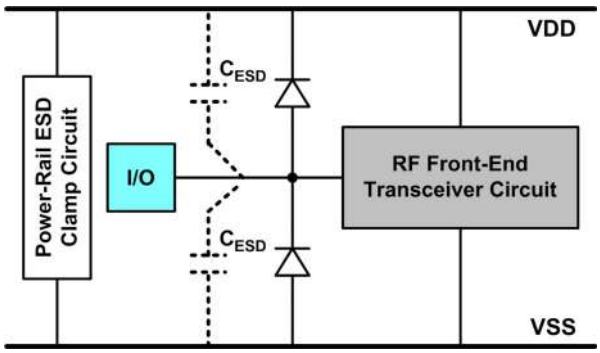

Fig. 1. Typical ESD protection scheme with double diodes for RF front-end or high-speed I/O applications.

A typical on-chip ESD protection scheme for RF front-end or high-speed I/O applications is shown in Fig. 1, where two ESD diodes at I/O pad are cooperated with the turn-on efficient power-rail ESD clamp circuit to discharge ESD current in the forward-biased condition. Through the turn-on efficient power-rail ESD clamp circuit, the device dimensions of these two diodes can be significantly shrunk to meet the circuit performance and ESD requirement simultaneously. In order to minimize the parasitic capacitance caused by the ESD protection diodes and to achieve satisfactory ESD robustness, the high frequency characteristics and the ESD levels of the ESD protection diodes in a 90-nm CMOS process were evaluated in this work to obtain the dependence of device size on ESD robustness and parasitic capacitance. Furthermore, the layout style of ESD protection diode will also directly affect its ESD robustness and parasitic capacitance. In previous studies [9]–[12], the ESD protection diodes realized in the waffle layout style have been verified to achieve better figure-of-merit (FOM) than that of stripe diodes under careful size optimization, which is suitable to RF front-end and high-speed I/O applications [9], [10].

Generally, the most important FOM used to evaluate the performance of the ESD protection diode is $I_{\mathrm{CP}}/C_{\mathrm{ESD}}$, where I_{CP} is the current level at which the measured I–V curve deviates from its linearly extrapolated value by 20% [9]. Consequently, it is desired to implement the ESD protection diode with a

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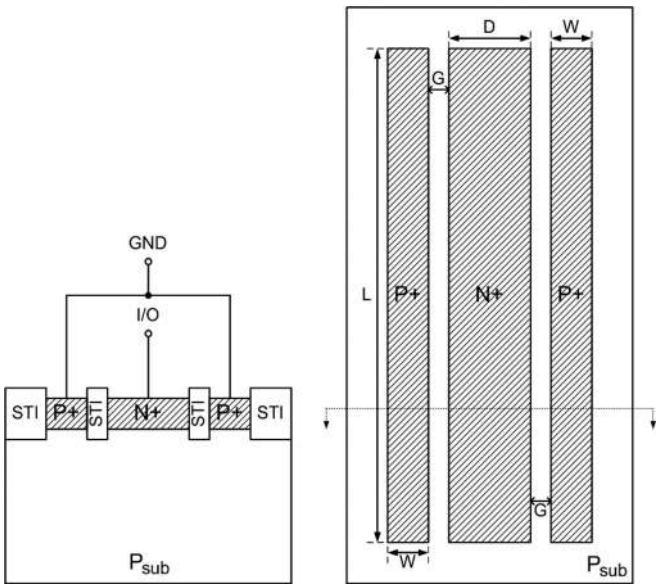

Fig. 2. Device cross-sectional view and layout top view of the ESD protection diode with typical stripe layout style.

large ratio of $I_{\rm CP}/C_{\rm ESD}$. It is better for the ESD protection diode to achieve higher $I_{\rm CP}$ and lower $C_{\rm ESD}$ at the specific layout style and device size. In order to further improve the $I_{\rm CP}/C_{\rm ESD}$, the area of active junction region in ESD protection diode must be minimized to attain low parasitic capacitance, but its junction perimeter must be maximized to enhance the ESD robustness. In this work, the ESD protection diodes realized in stripe, waffle, octagon, waffle-hollow, and octagon-hollow layout styles are fabricated in a 90-nm CMOS process and compared with each other. According to the measured results, the ESD protection diodes with octagon and hollow layout styles can successfully boost the $I_{\rm CP}/C_{\rm ESD}$ to make the diodes more profitable to RF front-end and high-speed I/O applications.

II. ESD Protection Diodes

For the $\rm N+/P_{sub}$ diode, the GND and I/O nodes are electrically connected to $\rm P+$ diffusion and $\rm N+$ diffusion, respectively. Under normal circuit operation, the diode is kept off due to the reverse-biased condition between the $\rm P_{sub}$ and $\rm N+$ diffusion regions. Although the diode is turned off, there is still an intrinsic junction capacitance of the diode seen by the signals at the I/O pad. On the other hand, the diode should be turned on to conduct ESD current at forward-biased condition under ESD stresses. Therefore, the junction capacitance of diode at reverse-biased condition and the ESD protection capability of diode at forward-biased condition are the important parameters to be investigated in the following.

A. Diode With Stripe Layout Style

The device cross-sectional view and layout top view of the ESD protection diodes with stripe layout style are shown in Fig. 2, which is the typical layout style to be often implemented in IC products. This typical stripe diode is realized with $\rm P+$ stripe on both sides of the $\rm N+$ stripe to give it with twice the conducting perimeter. Moreover, the width of $\rm N+$ stripe is twice as large as that of each $\rm P+$ stripe because the width of $\rm N+$ stripe is kept equal to the sum of each $\rm P+$ stripe, in order to avoid the current crowding at the $\rm N+$ stripe region. Based on the typical stripe diode, the diodes with the new proposed layout style will be discussed in the following sections to improve the characteristics of diodes for ESD protection and circuit performance.

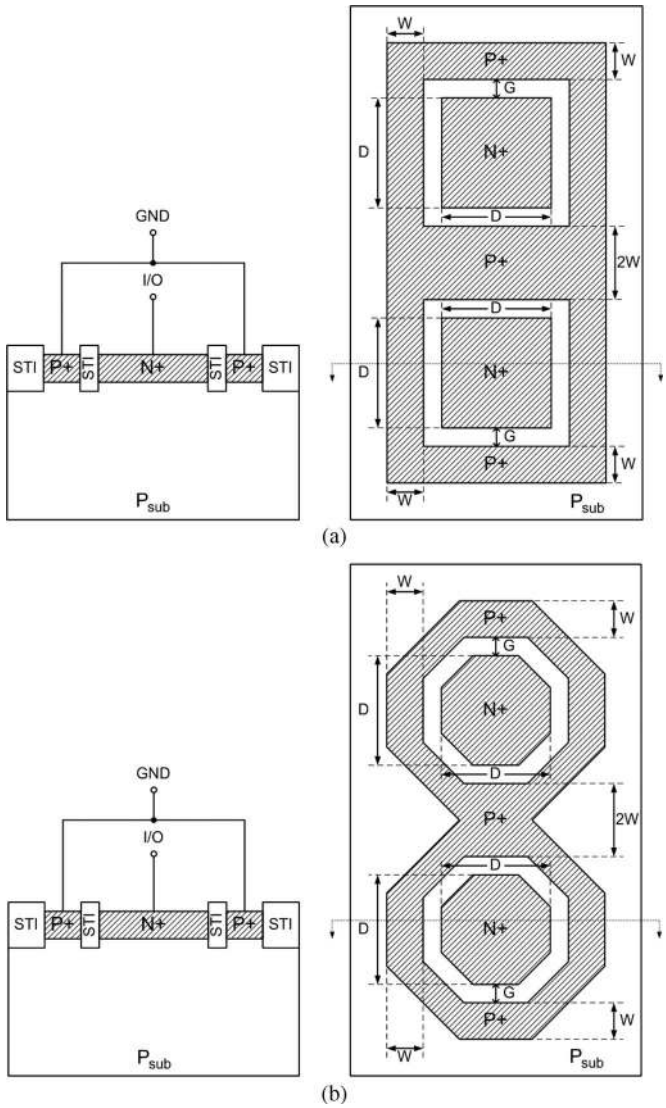

Fig. 3. Device cross-sectional view and layout top view of the ESD protection diodes with (a) waffle and (b) octagon layout styles.

B. Diodes With Waffle and Octagon Layout Styles

The device cross-sectional view and layout top view of the ESD protection diodes with waffle and octagon layout styles are shown in Fig. 3(a) and (b), respectively. The octagon layout style is formed from waffle layout style but the four corners are cut off. When the junction area of waffle and octagon diodes is reduced, they can achieve lower parasitic capacitance. Compared to the waffle diode, the junction perimeter and junction area of the octagon diode are simultaneously smaller than those of the waffle diode by 17%. It means that all FOMs based on physical characteristics of the waffle and octagon diodes would

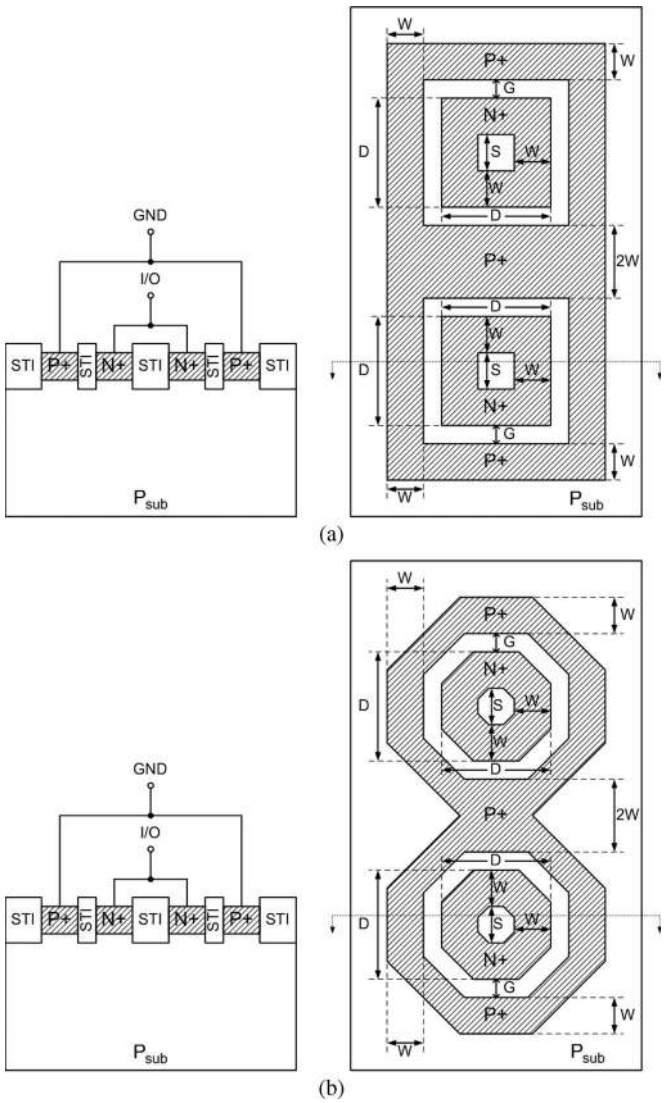

Fig. 4. Device cross-sectional view and layout top view of the ESD protection diodes with (a) waffle- and (b) octagon-hollow layout styles. The center region is drawn with the STI region to effectively reduce the parasitic capacitance.

be totally the same. Fortunately, the risk of damages located at the corner can be reduced by forming octagon layout style because the corner angle of octagon diode is larger than that of waffle diode. Therefore, the octagon diode can be supposed to have better ESD level than waffle diode.

C. Diodes With Waffle- and Octagon-Hollow Layout Styles

The two new proposed diodes investigated in this study are illustrated in Fig. 4(a) and (b), which are called as the waffle- and octagon-hollow layout styles, respectively. Generally, the parasitic capacitance of the diode is proportional to the active junction area, and the ESD robustness is related to the active junction perimeter. For RF front-end and high-speed I/O applications, the parasitic capacitance of the ESD protection diode is the key factor to directly affect the performance of RF front-end and high-speed I/O circuits. Therefore, it is desirable to implement the ESD protection diode with high ESD robustness but low parasitic capacitance.

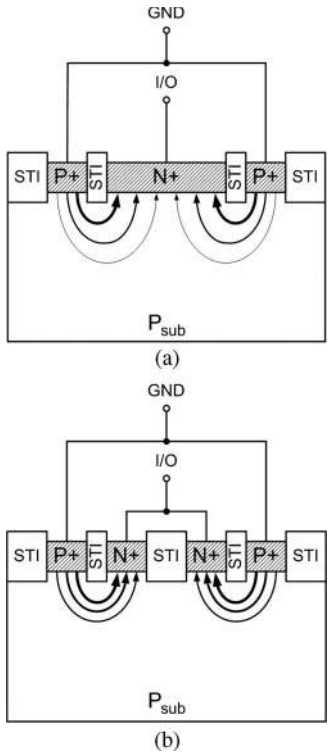

Fig. 5. Device cross-sectional view to explain ESD current flows in the diodes with (a) waffle and (b) waffle-hollow layout styles.

The purpose of forming the hollow layout is to reduce the active junction area and to keep the active junction perimeter at the same time by removing the $\mathrm{N}+$ central diffusion region off. For instance, the cross-sectional views to explain ESD current flows in the diodes with waffle and waffle-hollow layout styles are shown in Fig. 5(a) and (b), respectively. According to the device cross-sectional view in Fig. 5(a), the ESD current could not uniformly flow through whole $\mathrm{N}+$ active junction region in the waffle diode because the current always tends to flow through the shortest path between two nodes. Therefore, there is only a small part of total ESD current discharging through the $\mathrm{N}+$ central diffusion region, where still contributes parasitic capacitance to RF front-end and high-speed I/O circuits at normal circuit operation. By removing the $\mathrm{N}+$ central diffusion region to form the hollow layout style, the ESD current can be effectively concentrated in restricted region of the diode, as shown in Fig. 5(b). Consequently, the diodes with hollow layout style can be expected to attain a great reduction of parasitic capacitance without degrading ESD robustness severely at the same time. Similarly, all FOMs based on physical characteristics of the waffle-hollow are also the same as those of octagon-hollow diodes.

Based on the waffle layout style studied in previous works [9], [10], the octagon, waffle-hollow, and octagon-hollow layout styles are proposed and fabricated in a 90-nm CMOS process to investigate the dependence between ESD robustness and parasitic capacitance on diode layout styles. The important layout parameters of those investigated diodes are listed in Table I, where the different spacings are also marked in Figs. 2–4, respectively. It has to be noticed that the dimensions of the stripe diode in this work are not optimum.

TABLE I
MEASURED DEVICE CHARACTERISTICS AND PREVIOUS EVALUATION VALUE OF DIODE UNDER DIFFERENT LAYOUT STYLES

Layout Style	Stripe	Waffle			Octagon			Waffle-hollow			Octagon-hollow		
Size	D	A	B	C	A	B	C	A	B	C	A	B	C
Sizes of Device (μm)	W=1 G=0.5 D=2 L=40	W=1 G=0.5 D=3	W=1 G=0.5 D=4	W=1 G=0.5 D=5	W=1 G=0.5 D=3	W=1 G=0.5 D=4	W=1 G=0.5 D=5	W=1 G=0.5 D=3 S=1	W=1 G=0.5 D=4 S=2	W=1 G=0.5 D=5 S=3	W=1 G=0.5 D=3 S=1	W=1 G=0.5 D=4 S=2	W=1 G=0.5 D=5 S=3
N+ Junction Perimeter (μm)	80	24	32	40	19.92	26.56	33.20	24	32	40	19.92	26.56	33.20
Total N+ Junction Area (μm^2)	80	18	32	50	14.94	26.56	41.50	16	24	32	13.28	19.92	26.56
N+ Junction Perimeter / Total N+ Junction Area	1.00	1.33	1.00	0.80	1.33	1.00	0.80	1.50	1.33	1.25	1.50	1.33	1.25

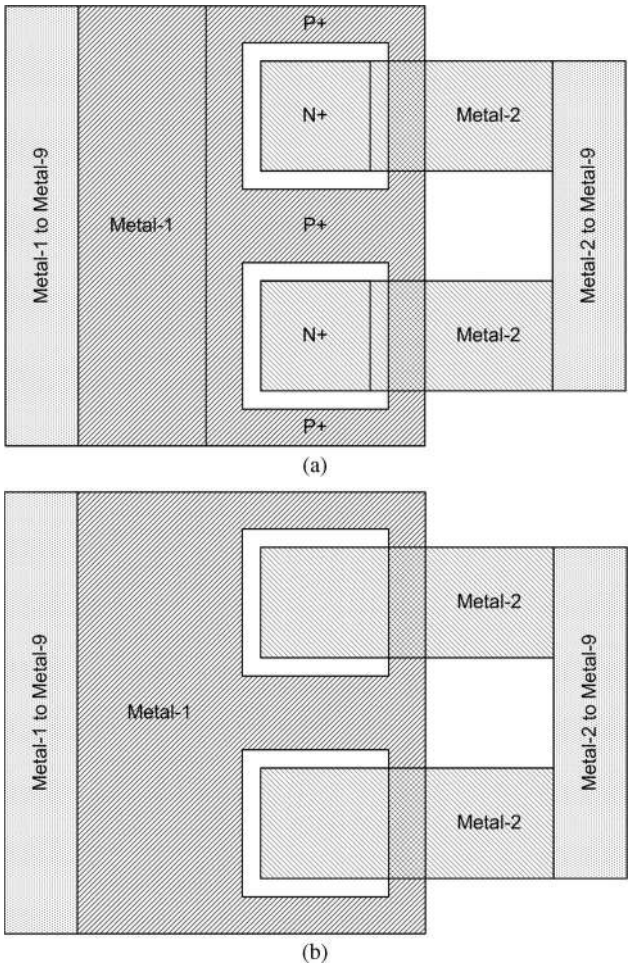

Fig. 6. Metal layout arrangement for the (a) interconnect routing of diodes and the (b) open pad structure.

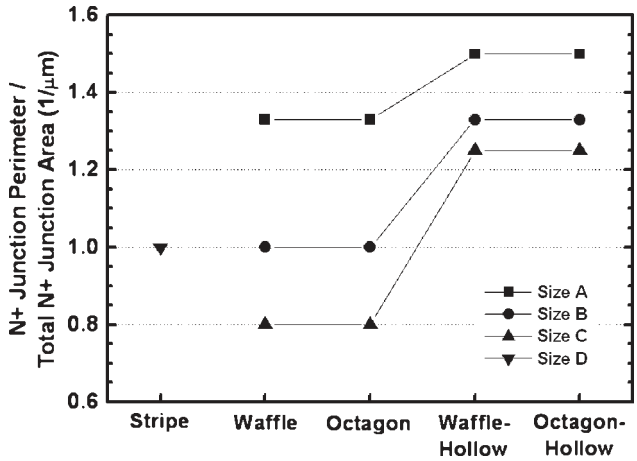

Fig. 7. Performance evaluations with the factors of $(\mathrm{N}+\text{junction perimeter})/(\text{total N}+\text{junction area})$ under different diode layout styles.

D. Interconnect Routing of the Diodes

To effectively reduce the impact from the parasitic resistance and capacitance of the interconnect routing in the layout of ESD diodes, the arrangement of metal lines to connect the ESD diodes should be considered with the de-embedding operation. The layout scheme of interconnect routing of ESD diodes is shown in Fig. 6(a). The width of metal line from the diode to the pad is drawn as large as possible to reduce the parasitic resistance of interconnect routing. With the large width of metal line, the parasitic resistance of interconnect routing (that can be estimated manually with the sheet resistance provided by foundry) can be quite smaller than the turn-on resistance of the ESD diodes. About the parasitic capacitance of interconnect routing, the layout scheme of the open pad structure for de-embedding calculation is shown in Fig. 6(b). The metal-1 layer that was originally connected to P+ region is remained, and the metal-2 layer that was originally connected to N+ region is also remained. With the measured S-parameters of the open pad structure, the parasitic capacitance of interconnect routing can be de-embedded to obtain the pure junction capacitance of the ESD diodes.

E. Performance Evaluations

Before implementing the diodes, there is a useful evaluation to imply the goodness of the diodes. This evaluation, discussed in the following paragraphs, is based on the physical dimensions of diodes listed in Table I.

This important evaluation is the factor of $(\mathrm{N}+\text{junction perimeter})/(\text{total N}+\text{junction area})$. This is the most commonly used evaluation to estimate the diodes, as that illustrated in Fig. 7. The N+ junction perimeter is related to ESD

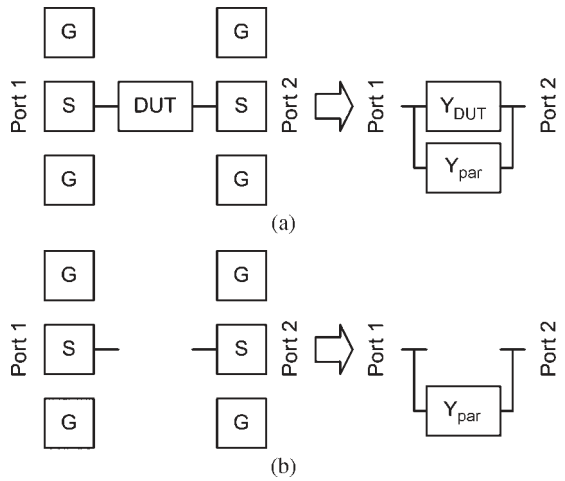

Fig. 8. Layout top views for de-embedded calculation to extract the parasitic capacitance of the fabricated ESD diodes with (a) including- and (b) excluding-DUT patterns.

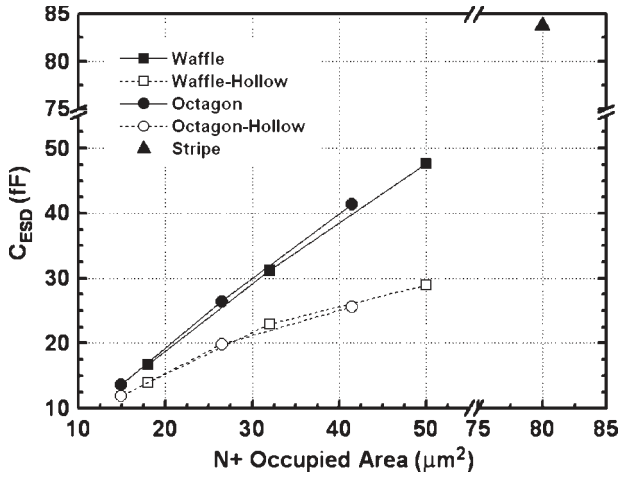

Fig. 9. Dependence of C_{ESD} extracted from S-parameter at 2.5 GHz under zero DC bias on the N+ occupied area of diode devices with different layout styles.

robustness, and the total N+ junction area is corresponded to parasitic capacitance at normal circuit operation. Undoubtedly, this evaluation is expected to be large to sustain high enough ESD robustness and minimize the degradation of circuit performance for RF front-end and high-speed I/O applications. In Fig. 7, the diodes with hollow layout styles obviously have the highest values at the specified diode size. Moreover, the large-size diodes with hollow layout styles can achieve comparable level to that of small-size diodes with non-hollow layout style. This result inspires us to consider a way not to continuously shrink the diode size to avoid any capacitance penalty from the junction perimeter [8]–[10]. Although the diode with stripe layout style has the smallest width, its evaluation is not the highest because the diode with stripe layout style cannot give the N+ junction perimeter as much as those of the diodes with other layout styles. The performance evaluation is also listed in Table I.

III. Experimental Results

The test chips of diodes with the stripe, waffle, and new proposed layout styles have been fabricated in a 90-nm CMOS process. These diodes are prepared with the consideration of two-port S-parameter measurement, transmission line pulsing (TLP) measurement, and HBM ESD robustness measurement. In this work, each diode structure was tested four times from four separated dice.

A. Parasitic Capacitance

The diode devices are arranged with ground–signal–ground (G–S–G) pads to facilitate on-wafer two-port S-parameter measurement. During the S-parameter measurement, the P+ and N+ diffusion regions of the diode devices are connected to ports 1 and 2, respectively, and they are both biased at 0 V.

In order to extract the characteristics of the intrinsic device at high frequency, the parasitic effects of the pad and the interconnect routing must be de-embedded [13]–[15]. The test structures, one including the DUT and the other excluding the DUT (open pad structure), as shown in Fig. 8(a) and (b), were implemented in the same test chip [13], [14]. The Y_{22}-parameter can be obtained from the measured two-port S-parameters by

$$Y_{22} = \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{Z_0\left((1+S_{11})(1+S_{22})-S_{12}S_{21}\right)} \tag{1}$$

where Z_0 is the termination resistance of 50Ω [15]. The measured Y-parameter of the including-DUT pattern is labeled as $Y_{22-\mathrm{meas}}$, and the measured Y-parameter of the excluding-DUT pattern (open pad structure) is labeled as $Y_{22-\mathrm{open}}$. The intrinsic device characteristics, $Y_{22-\mathrm{DUT}}$, can be obtained by subtracting $Y_{22-\mathrm{open}}$ from $Y_{22-\mathrm{meas}}$. The parasitic capacitance (C_{ESD}) of each diode can be extracted from the Y-parameter of the intrinsic device by

$$C_{\mathrm{ESD}} = \frac{\mathrm{Im}(Y_{22-\mathrm{DUT}})}{2\pi f} \tag{2}$$

where f is the operating frequency. The extracted parasitic capacitances of the fabricated diode devices at 2.5 GHz under zero DC bias are listed in Table II and shown in Fig. 9.

From the measured results of the diode devices with stripe, waffle, and octagon layout styles, the extracted parasitic capacitances are obviously proportional to the N+ occupied area. Meanwhile, the reductions of parasitic capacitances can achieve 16%, 26%, and 39% by modifying the diodes in sizes A, B, and C from waffle to waffle-hollow layout styles, respectively. Similarly, it can achieve the reductions of parasitic capacitance of 13%, 25%, and 38% by modifying the diodes from octagon to octagon-hollow layout styles. The reduction of parasitic capacitance is exactly meeting the theoretical calculations. This great reduction of parasitic capacitance is the key factor to significantly improve the FOM of the diodes with hollow layout style.

B. Transmission Line Pulsing (TLP) Measurement

In order to investigate the device behavior during high ESD current stress, a transmission line pulsing (TLP) generator with a pulse width of 100 ns and a rise time of ∼2 ns is used

TABLE II
MEASURED RESULTS AVERAGED FROM FOUR SEPARATED DICE AND FOM OF DIODE DEVICES WITH DIFFERENT LAYOUT STYLES

Layout Style	Stripe	Waffle			Octagon			Waffle-hollow			Octagon-hollow		
Size	D	A	B	C	A	B	C	A	B	C	A	B	C
C_{ESD}(fF)	83.71	16.70	31.18	47.64	13.65	26.44	41.39	13.92	22.95	28.95	11.85	19.89	25.61
It_2(A)	3.338	0.948	1.418	1.851	0.861	1.241	1.636	0.944	1.281	1.639	0.840	1.178	1.481
I_{CP}(A)	2.873	0.755	1.192	1.675	0.664	1.026	1.434	0.737	1.118	1.428	0.656	0.981	1.282
V_{HBM}(kV)	6.6	1.7	2.6	3.5	1.4	2.2	2.9	1.7	2.3	3.1	1.4	2.0	2.7
R_{ON}(Ω)	0.885	1.690	1.280	1.024	1.912	1.460	1.156	1.693	1.314	1.093	1.967	1.509	1.299
I_{CP}/C_{ESD} (mA/fF)	34.32	45.21	38.23	35.16	48.64	38.80	34.65	52.95	48.71	49.33	55.36	49.32	50.06
V_{HBM}/C_{ESD} (V/fF)	78.84	101.8	83.39	73.47	102.6	83.21	70.07	122.1	100.2	107.1	118.1	100.6	105.4
$R_{ON} \times C_{ESD}$ (Ω-fF)	74.08	28.22	39.91	48.78	26.10	38.60	47.85	23.57	30.16	31.64	23.31	30.01	33.27

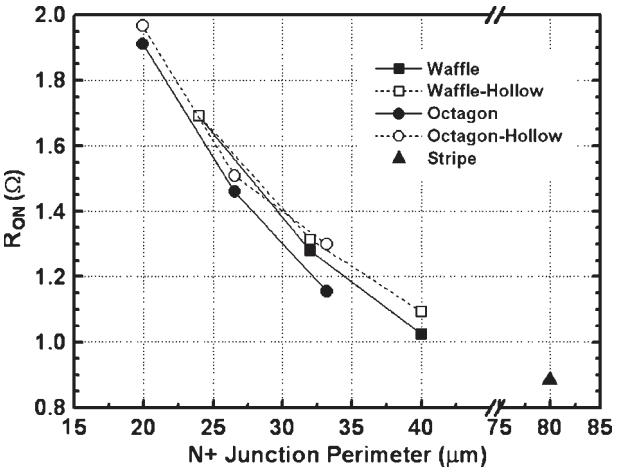

Fig. 10. Dependence of TLP-measured $R_{\rm ON}$ on the N+ junction perimeter of diode devices with different layout styles.

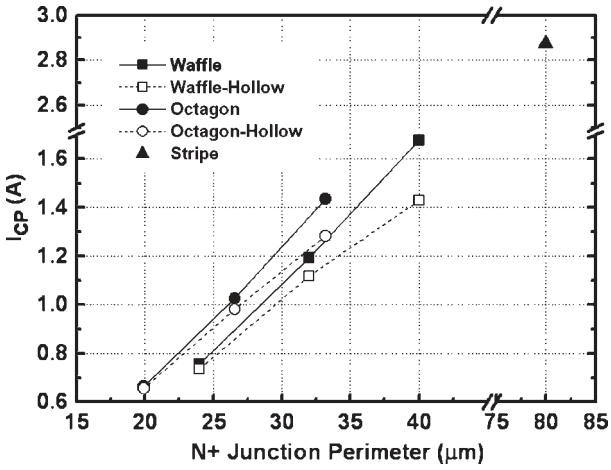

Fig. 11. Dependence of TLP-measured $I_{\rm CP}$ on the N+ junction perimeter of diode devices with different layout styles.

to measure the second breakdown current (It_2) of the device [16]. For the ESD protection diode, it is suggested that an appropriate upper-bound current level, $I_{\rm CP}$, is utilized because the ESD protection diode should never be designed to discharge ESD current near its failure level [9], [10]. By using TLP, the on-resistance ($R_{\rm ON}$), It_2, and $I_{\rm CP}$ derived from It_2 of the diode devices under positive stresses at the P+ diffusion region with grounded N+ diffusion region are measured and listed in Table II. The $R_{\rm ON}$ and $I_{\rm CP}$ versus the N+ junction perimeter of the diodes are illustrated in Figs. 10 and 11, respectively. Apparently, the $R_{\rm ON}$ is decreased and the $I_{\rm CP}$ is increased with the increased N+ junction perimeter.

When the diode is modified from non-hollow to hollow layout style, the drop on $I_{\rm CP}$ of the diode with large device size is greater than that of the diode with small device size. The line current densities, which are the ratio of $I_{\rm CP}$ to N+ junction perimeter, of waffle and octagon diodes are calculated in Table III. The drop percentages of line current density from waffle to waffle-hollow (from octagon to octagon-hollow) are also calculated in Table III. From the measured results and calculations, the waffle (or octagon) diode with large device size has larger line current density and larger drop percentage of line current density while modified to waffle-hollow (or octagon-hollow) diode. This implies that the ESD discharging current of waffle (or octagon) diode with large device size would flow more deeply through the N+ central diffusion region because waffle (or octagon) diode with large device size has more contacts at N+ diffusion region to cause a small equivalent resistance at the cathode. With more detailed explanation and illustration, the simulations can give a clear perspective. Fig. 12(a) and (b) are the current vector plots of the diode in small and large sizes, respectively. For convenience, the anode is set along the entire edge of the diode, and the cathode is set along the right half of the top surface of the diode. When the diode is drawn in small size, the fewer contacts at junction area make the current crowded into the nearest corner of the electrode. On the contrary, there are more contacts at the junction area for the diode drawn in large size, as shown in Fig. 12(b). The current crowding behavior experienced in Fig. 12(a) has diminished, and the current can be distributed through the entire electrode more widely. Based on the simulation results and the measured results of line current density in Table III, the ESD discharging current through the diode in large size is expected to flow more deeply through the N+ central diffusion region. Therefore, the diode in large device size has larger reduction of $I_{\rm CP}$ when the diode with non-hollow layout style is modified to hollow layout style.

According to the measured results, the reductions of $I_{\rm CP}$ are 2.4%, 6.2%, and 8.8% for the waffle diodes in sizes A, B, and

TABLE III
LINE CURRENT DENSITY OF DIODE DEVICES

Layout Style	From Waffle to Waffle-hollow						From Octagon to Octagon-hollow					
Size	A	A	B	B	C	C	A	A	B	B	C	C
I_{CP} (A)	0.755	0.737	1.192	1.118	1.675	1.428	0.664	0.656	1.026	0.981	1.434	1.282
N+ Junction Perimeter (μm)	24	24	32	32	40	40	19.92	19.92	26.56	26.56	33.20	33.20
Line Current Density (mA/μm)	31.46	30.71	37.25	34.94	41.88	35.70	33.33	32.93	38.63	36.94	43.19	38.61
Drop Percentage of Line Current Density (%)	2.38		6.20		14.76		1.20		4.37		10.60	

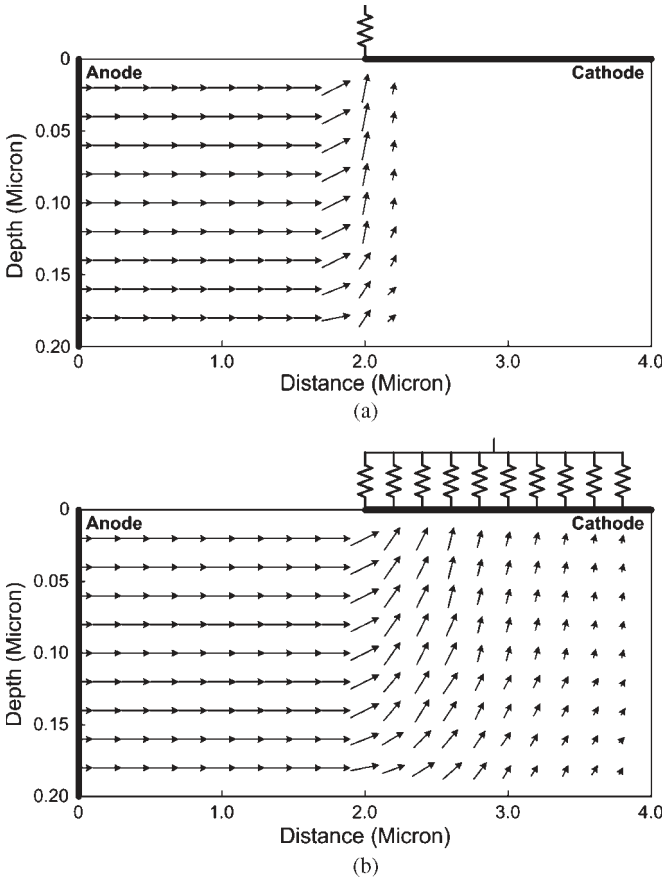

Fig. 12. Simulated vectors of ESD discharging current along the cross section of waffle diode with (a) small and (b) large device sizes.

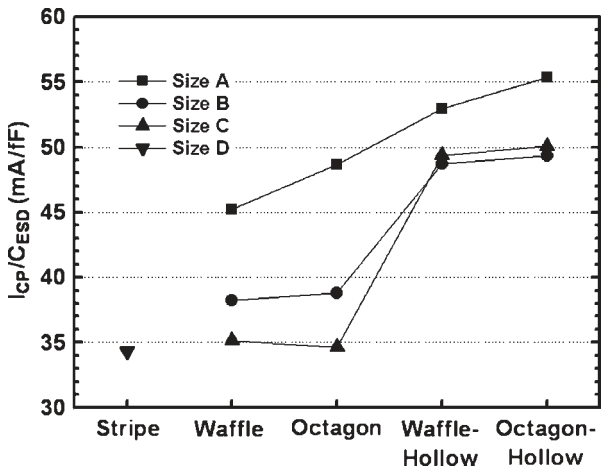

Fig. 13. ($I_{\rm CP}/C_{\rm ESD}$) FOM of ESD protection diodes with different layout styles.

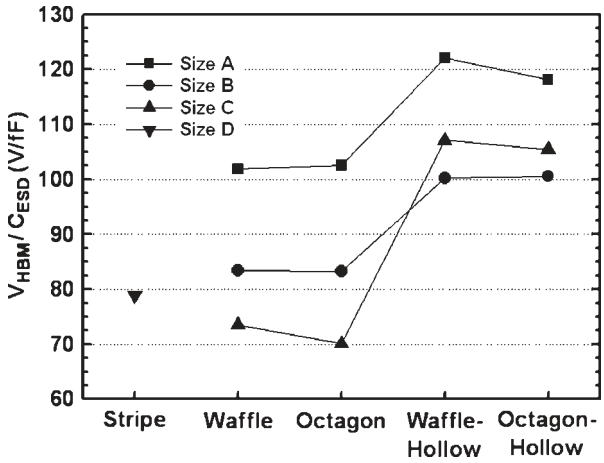

Fig. 14. ($V_{\rm HBM}/C_{\rm ESD}$) FOM of ESD protection diodes with different layout styles.

C, respectively. Also, they are 1.2%, 4.4%, and 10.6% for the octagon diodes in sizes A, B, and C, respectively. Compared with the reductions of parasitic capacitance, the removed N+ central diffusion region is originally flowed by a small part of total ESD discharging current. Consequently, removing the N+ central diffusion region of the diodes can greatly reduce the parasitic capacitance without degrading the ESD protection capability.

C. ESD Robustness

The human-body-model (HBM) ESD robustness of the fabricated diodes is also listed in Table II. The relationship between the HBM ESD level ($V_{\rm HBM}$) and the It_2 based on the measured results in this work is about

$$V_{\rm HBM} \approx (1800 + R_{\rm ON}) \times It_2 \quad (3)$$

where $R_{\rm ON}$ is the turn-on resistance of the diode. The HBM ESD levels of all ESD protection diodes are within the range of 1.4–3.5 kV, except the stripe diode.

D. FOM Comparison and Discussion

The FOMs ($I_{\rm CP}/C_{\rm ESD}$, $V_{\rm HBM}/C_{\rm ESD}$, and $R_{\rm ON} \times C_{\rm ESD}$) of the diode devices are listed in Table II and shown in Figs. 13–15. The most important FOM, $I_{\rm CP}/C_{\rm ESD}$, among the diodes is illustrated in Fig. 13. The trend of $I_{\rm CP}/C_{\rm ESD}$ is apparently increasing from non-hollow to hollow layout style due

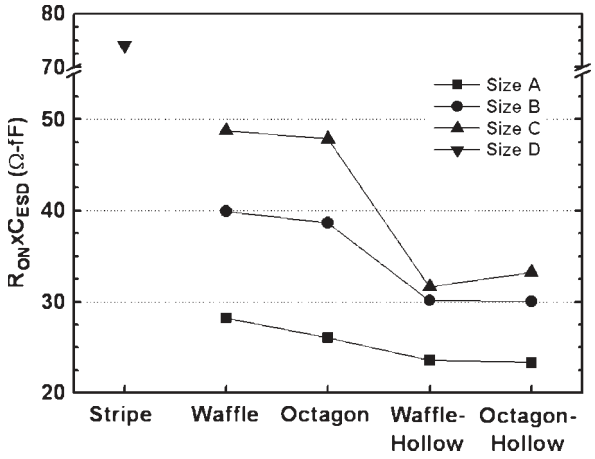

Fig. 15. ($R_{\rm ON} \times C_{\rm ESD}$) FOM of ESD protection diodes with different layout styles.

to the reduction of parasitic capacitance, and the results exactly meet the expectation of layout design. Because the HBM ESD level is directly proportional to It_2, the trend of $V_{\rm HBM}/C_{\rm ESD}$ illustrated in Fig. 14 is quite similar to that in Fig. 13. According to the experimental results of diodes with different layout styles, the diodes with hollow layout styles can apparently achieve higher ESD robustness under the same parasitic capacitance. For instance, the measured results clearly demonstrate that the $I_{\rm CP}/C_{\rm ESD}$ of waffle-hollow (or octagon-hollow) diode in size C is better than that of waffle (or octagon) diode in size B. These two diodes actually have the same total N+ junction area, but the N+ junction perimeter of waffle-hollow (or octagon-hollow) diode in size C is obviously larger. This feature reveals that the diodes with waffle-hollow (or octagon-hollow) layout styles can attain higher $I_{\rm CP}$ than those with waffle (octagon) layout styles under the same total N+ junction area to achieve better $I_{\rm CP}/C_{\rm ESD}$. Besides, the $I_{\rm CP}/C_{\rm ESD}$ can also be slightly improved from waffle (or waffle-hollow) diode to octagon (or octagon-hollow) diode due to the relaxation of current distribution located at the smoother corners.

The $I_{\rm CP}/C_{\rm ESD}$ values of waffle- and octagon-hollow diodes in sizes B and C can achieve almost the same level as that of waffle diode in size A. It represents that the diode with hollow layout style in large size still can sustain $I_{\rm CP}$ as high as that of the diode with waffle layout style in small size under the same parasitic capacitance. As a result, the waffle- and octagon-hollow diodes in large size can perform as well as the waffle diode in small size under careful layout optimization.

From TLP I–V measurement and the results in Fig. 11, $R_{\rm ON}$ can be reduced by increasing the N+ junction perimeter of the ESD diodes, but this action also increases the parasitic capacitance of the ESD diodes simultaneously due to the increased N+ junction area. For ESD protection purposes, the $R_{\rm ON}$ of the ESD diode is expected to be as small as better to effectively clamp the voltage. The $C_{\rm ESD}$ is also highly demanded to be as small as better to avoid the RF circuits' performance degradation. Therefore, the $R_{\rm ON} \times C_{\rm ESD}$ is another useful justification to the diodes, as shown in Fig. 15. The $R_{\rm ON} \times C_{\rm ESD}$ value of the stripe diode is too large, which is hard to be implemented for high-performance RF and high-speed I/O interface applications. For the diodes with hollow layout styles, such values can be reduced to the range from 23 to 34 ($\Omega - {\rm fF}$), which is much smaller than that of the stripe diode. Moreover, the $R_{\rm ON} \times C_{\rm ESD}$ value of the waffle- and octagon-hollow diodes in large size can also be comparable to that of waffle and octagon diodes with small size.

Although the waffle diode in small size theoretically has larger ratio of N+ junction perimeter to N+ junction area, carefully optimizing the size of waffle diode is still required to avoid any capacitance penalty from the junction perimeter [9], [10]. Therefore, it is not necessary to simply shrink the device size of waffle diode to achieve a high value of $I_{\rm CP}/C_{\rm ESD}$ and a low value of $R_{\rm ON} \times C_{\rm ESD}$. In this work, it has been verified that there are two methods, forming octagon and hollow layout styles, to effectively improve the $I_{\rm CP}/C_{\rm ESD}$ and $R_{\rm ON} \times C_{\rm ESD}$ of the diodes.

IV. Conclusion

New proposed diodes with octagon and hollow layout styles have been successfully verified in a 90-nm CMOS process. Layout optimization is the essential element to minimize the parasitic capacitance and to improve ESD robustness of the ESD protection diodes for RF front-end and high-speed I/O applications. As compared to the diodes with stripe and waffle layout styles, the new proposed diodes with hollow layout styles have been demonstrated to significantly improve ESD robustness under the same parasitic capacitance. Therefore, the proposed waffle- and octagon-hollow diodes are more suitable to be implemented to RF front-end and high-speed I/O circuits.

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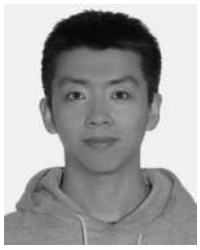

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