Optimization Platform to Find a Switching Pattern of Digital Active Gate Drive for Reducing Both Switching Loss and Surge Voltage

Yu Shan Cheng, *Member, IEEE*, Tomoyuki Mannen, *Member, IEEE*, Keiji Wada, *Senior Member, IEEE*, Koutarou Miyazaki, *Member, IEEE*, Makoto Takamiya, *Senior Member, IEEE*, and Takayasu Sakurai, *Fellow, IEEE*

***Abstract*—A gate driving for power devices is a key technology to further improve switching characteristics. With the help of digital gate driver IC, the switching behavior of power devices can be enhanced even under high-speed switching. In this paper, an evaluation platform for determining the optimal switching pattern of an active gate drive control is proposed for an inverter circuit. A high speed optimization system is built up to search for an advantageous switching pattern that reduces total switching loss of two power devices in an inverter circuit and constrains surge voltage simultaneously. The proposed online optimization demonstrates its feasibility for the full-bridge inverter circuit, which is rated at 500 V with digital active gate drive control. Experimental results show that the proposed optimization system is able to obtain optimal switching pattern from 64^{60} possible combinations of switching patterns within 15 min, which is 6 times faster than the previous study. Optimizations can also conducted under different load current conditions. Eventually, the obtained optimal pattern yields up to 42% reduction in the total switching loss when it constrains surge voltage to minimum compared with the conventional driving pattern.**

***Index Terms*—Active gate drive, automatic optimization, particle swarm optimization (PSO), surge voltage, switching loss.**

I. Introduction

POWER converter circuits are introduced in a wide range of applications including managing energy flow and applying in motor driving. Regardless of power ratings, power devices are one of the dominant components in power converter circuits. By virtue of the progress on semiconductor power device [1], [2], high power density has become feasible because of high-speed switching operation. In fact, switching transient characteristics of power devices has a direct impact on the efficiency and reliability of power converters. The overall performance of a power converter is not only dependent on the properties of power device itself but also on the gate drive control circuit [3]–[5]. Active gate drive techniques were developed to improve the switching behaviors of semiconductor power devices such as MOSFETs [6], Si or SiC IGBTs [7], and GaN FETs [8]–[10]. Unlike the conventional gate drive technique that uses a fixed gate resistor, active gate drive control allows adjustment of the driving current/voltage to shape the switching trajectories. With the active gate drive technique, it is possible to manage the tradeoff between energy loss, device stress, and electromagnetic interference in the switching transient [11], [12].

As the progress on high-speed and low-latency DSP or FPGA, digital control circuits are attractive to realize active gate drive control due to its control flexibility and adaptability [13]–[15]. One programmable gate driver IC proposed in [16] provides transition control in the gate voltage. Another digital active gate drive IC with closed loop gate current control is shown in [17]. A digital active gate drive IC developed in [18] provides an adjustable switching waveform using full digital control. However, the high flexibility in the switching pattern provided by the digital gate drive IC makes the searching for the optimal switching pattern a challenging task. Manual trial-and-error and exhaustive search shows no benefits due to high-dimensional searching space defined by the problem itself. The fact of high computation cost and time consuming is also reported in [19] when automatic optimization based on simulated annealing was applied. A similar issue in determining the gate drive profile was also addressed in [20]–[22]. A systematic approach to demonstrate the effect of digital active gate drive waveforms on an IGBT switching operation was proposed in [20]. As a basis to develop online pattern optimization, substantial experiments were conducted to figure out the number of decision variables that describe the optimal gate waveform. In [21], the searching time for the optimum gate resistor values is reduced because of less experimental tests, which were followed by an analysis of the measured waveforms and losses. In [22], a profiled optimum gate drive waveform is able to adapt to load current variations using driver frequency adaption. Moreover, [23] reported that the resulting optimal pattern is dependent on circuit stray inductance. Different circuit topologies or layouts may result in variations on optimum switching profile. Until now, the design

Manuscript received November 19, 2018; revised March 30, 2019; accepted June 18, 2019. Date of publication July 8, 2019; date of current version August 14, 2019. Paper 2018-IPCC-1150.R1, presented at the 2018 IEEE Energy Conversion Congress and Exposition, Portland, OR, USA, Sep. 23–27, and approved for publication in the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS by the Industrial Power Converter Committee of the IEEE Industry Applications Society. This work was supported by the New Energy and Industrial Technology Development Organization. (Project code: P10022). *(Corresponding author: Yu Shan Cheng.)*

Y. S. Cheng, T. Mannen, and K. Wada are with Tokyo Metropolitan University, Tokyo 192-0364, Japan (e-mail: ys-cheng@tmu.ac.jp; mannen@tmu.ac.jp; kj-wada@tmu.ac.jp).

K. Miyazaki, M. Takamiya, and T. Sakurai are with the University of Tokyo, Tokyo 113-8654, Japan (e-mail: koutaro1.miyazaki@toshiba.co.jp; mtaka@iis.u-tokyo.ac.jp; tsakurai@iis.u-tokyo.ac.jp).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TIA.2019.2927462

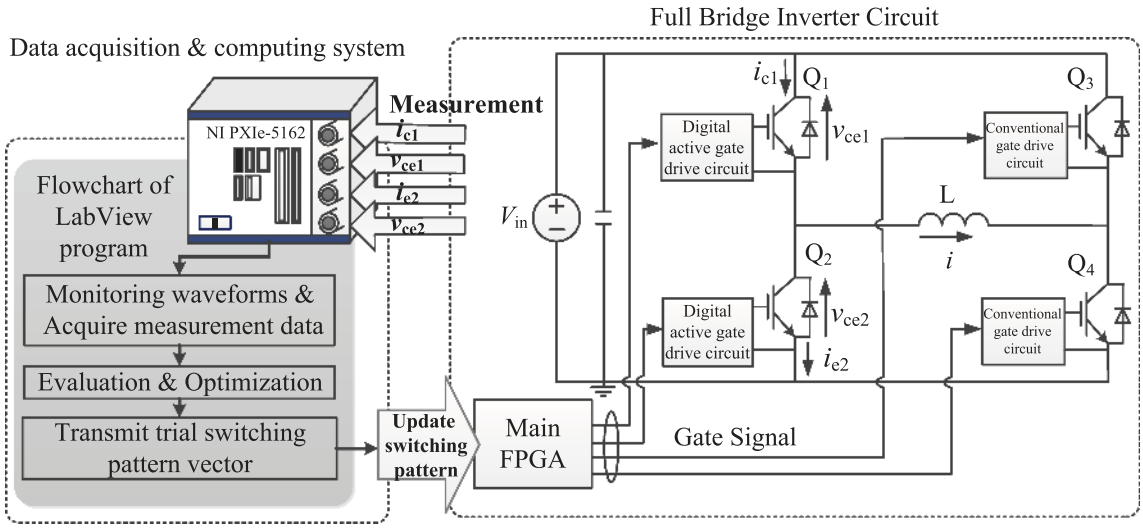


Fig. 1. System diagram for optimizing the switching pattern of the digital active gate drive.

of gate drive waveforms remains a key issue in the application of digital active gate drive circuits. In particular, more variables are involved when it is implemented in a practical inverter system rather than a dedicated testing circuit. To apply this technology and make use of its advantages to maximum, a general and high speed optimization system is required [24].

In this paper, an online optimization platform with high-speed data acquisition and validation of the obtained optimal pattern is proposed for optimizing the switching pattern for a digital active gate drive circuit. This optimization platform is identified to bridge the gap when applying active gate drive IC to an inverter circuit. It is noted that an optimization result from a dedicated testing circuit might fail to perform the identical switching behavior when applying in an inverter. In addition, the time-varying output current of inverter also corresponds to different optimal driving pattern. The proposed online optimization platform is featured by efficient searching algorithm and the integration between circuits and evaluation system. Hence, the proposed optimization platform is regarded as an important preparation work when looking into the relation between active driving pattern and switching behaviors. Experiments were performed with a 500 V, 20 A full-bridge inverter circuit. Specifically, this system can be used to find the optimized gate drive pattern in less than 15 min from entirely 64^{60} possible gate driving patterns. The results show that surge voltage and switching loss were reduced simultaneously.

II. System Configuration

A. Full-Bridge Inverter Circuit

The investigated full-bridge inverter consists of four Si-IGBTs (2MBI150VH-170-50, 1700 V, 150 A) and the inductive load L as illustrated in Fig. 1. The left leg of Q_1 and Q_2 is connected to an active gate driver circuit, respectively, while the right leg IGBT Q_3 and Q_4 are driven with conventional gate drive circuits using a constant gate resistor. The inverter circuit and the driving pattern for active gate drive IC are controlled with an FPGA.

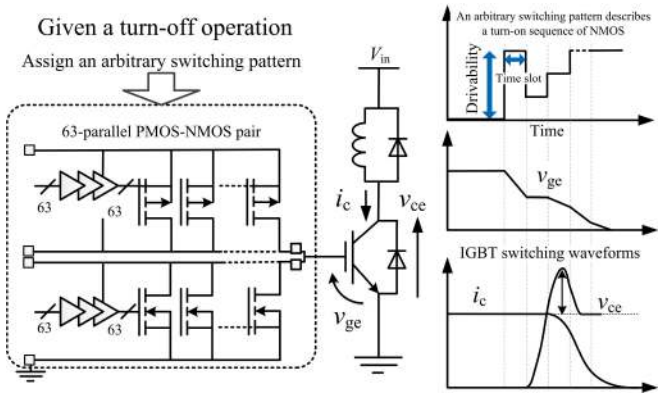


Fig. 2. Illustrative figure to show the adaptability of gate driving waveform using the active gate drive IC.

With a focus on left leg Q_1 and Q_2, the gate signals works complementary to each other and a deadtime is inserted as a turn-ON delay of pulsewidth modulation (PWM) operations. Soft and hard switching are classified depending on the direction of inductor load current and commutation events as shown in [23]. Among them, two hard switching operations are discussed in this paper: first, the turn-ON event of Q_1 when $i > 0$ and second, the turn-ON event of Q_2 when $i < 0$. To evaluate the switching performance, the total switching loss from Q_1 and Q_2, and the surge voltage are considered. As shown in Fig. 1, an iterative evaluation loop includes updating switching pattern, voltage and current measurement, and the evaluation of switching behavior. Each switching pattern and its resulting waveforms are monitored and input to computation system for updating the new switching pattern.

B. Digital Active Gate Driver

Fig. 2 shows a conceptual figure of the effects when applying active gate drive technique and a schematic diagram of the employed gate driver IC. The clock signal in the active gate drive

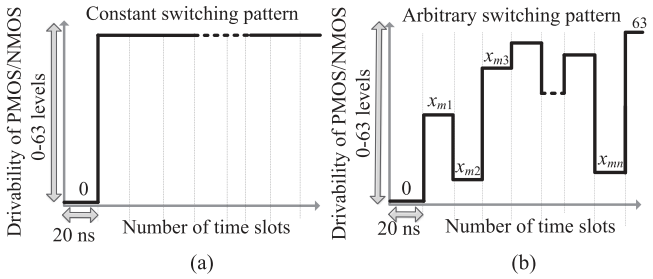


Fig. 3. Conceptual figure of switching patterns for gate drive in (a) the conventional method and (b) an arbitrary method.

IC is set to 50 MHz, and 63 PMOS-NMOS pairs provide the capability of shaping gate waveforms. Since each driver MOS transistor can be tuned from 3 to 80 mA. In this way, the peak driving level 63 can output the maximum rated gate current at 5 A (63 $\times$ 80 mA). Therefore, the digital gate drive IC allows control over the gate current with time intervals as short as 20 ns and up to 64 levels of drivability. To turn on the power device, the number of turn-ON PMOS is determined during the switching transient. The number of turn-ON NMOS is determined to turn OFF the power device. Given an IGBT turn-OFF operation for example, the NMOS turn-ON sequence is regarded as a certain switching pattern, as shown on the top of Fig. 2. This exemplary switching pattern shapes the gate voltage waveform $v_{\rm ge}$ and results in the corresponding transient behavior, i.e., surge voltage and switching loss. It is noted that, Fig. 2 is a conceptual figure to show the adaptability of gate drive waveform using double pulse testing circuit [1]. The actual optimization platform is carried out on full-bridge inverter circuit and connected with active gate drive IC. The switching performance can be managed with an active gate drive circuit, as the switching characteristics in each individual switching period can be adjusted whenever for turn-ON or turn-OFF operation of power devices. In this paper, considering two hard switching events (Q_1 turn-ON operation and Q_2 turn-ON operation), the switching pattern indicates the PMOS turn-ON sequence for an individual active gate drive IC. Fig. 3 illustrates the difference between the conventional driving technique and the active gate drive technique with switching patterns. In contrast to a constant driving voltage in Fig. 3(a), also known as the conventional driving pattern, the active gate drive IC can be configured with an arbitrary pattern, as shown in Fig. 3(b), which generates the corresponding gate driving waveform. Hence, the online optimization system is proposed to determine the most advantageous switching pattern for active gate drive applications.

C. Data Acquisition System

Currently, it is difficult to derive analytic functions describing the switching performance in terms of the driving voltage due to the lack of accurate mathematical models for IGBTs. An online optimization system is proposed to remove numerous uncertainties. To find out an optimal switching pattern, the on-line optimization system aims to automatically update trial switching patterns, instantaneously measure the corresponding transient behavior, and eventually converge the patterns to the most advantageous one. However, the optimal gate switching pattern might vary with operation conditions (e.g., dc voltage and the load current). Moreover, the case temperature of power devices will rise along with operation time and cause variations in its characteristics. Thus, the searching process must be completed as soon as possible under any circumstances. A high-speed and real-time data acquisition system is required for an automatic online optimization system and to ensure that the resulting waveforms are collected instantaneously for evaluation.

As shown in Fig. 1, the required functionalities for data acquisition and computation are provided by a PXIe-8880 PC controller module and PXIe-5162 oscilloscope module from National Instruments (NI). All the voltage ($v_{\rm ce1}$, $v_{\rm ce2}$) and current ($i_{\rm c1}$, $i_{\rm e2}$) waveforms are measured at a sampling rate of 1.25 GS/s and are fed to the optimization system as performance indicators. The National Instruments LabVIEW platform is used for control and monitoring. A flowchart of the LabVIEW program is shown on the left part of Fig. 1. Three main blocks are constructed in the proposed system: a) NI-SCOPE enables oscilloscope configuration, b) NI-VISA (Virtual Instrument Software Architecture interface) provides simple programming for serial data transmission between instruments, and c) event detection is used to initiate PWM signals and then starts to determine the trial pattern. As for evaluation and pattern update, an optimization algorithm is programmed in a MATLAB script and integrated into the LabVIEW program. The system carries out each trial switching pattern every second. Once the trial switching vector is generated for next implementation, this switching pattern command will be delivered via NI-VISA to the main FPGA. Commands or patterns are processed to the transmission port by passing a queue reference between blocks.

III. Optimization

The possible number of switching pattern combinations has significantly increased by using the digital active gate drive IC. One must determine the most advantageous switching patterns for the investigated circuit to fully utilize features provided by the digital active gate drive IC. Based on the turn-ON time from the datasheet, 60 time slots are determined in advance to cover the switching transient period. As a result, there are 64^{60} possible switching patterns provided by active gate driver. Due to such high degrees of freedom for the shape of the switching pattern, exhaustive search is infeasible for finding optimal pattern. Assuming the switching pattern is represented by a vector

$$\mathbf{x}_m = [x_{m1},\, x_{m2},\, x_{m3}, ...x_{mn}] \tag{1}$$

where m is the index of the possible switching vector and n is the number of elements in one switching vector. As there are a large number of variables (x_{m1} to x_{mn}) to be determined, particle swarm optimization (PSO) [25] is utilized to explore the high-dimensional searching space due to its properties of simple implementation and high searching efficiency. Unlike a trajectory-based algorithm, such as simulated annealing or tabu search, a single solution is used to describe the exploring trajectory in the searching space. Therefore, high number of

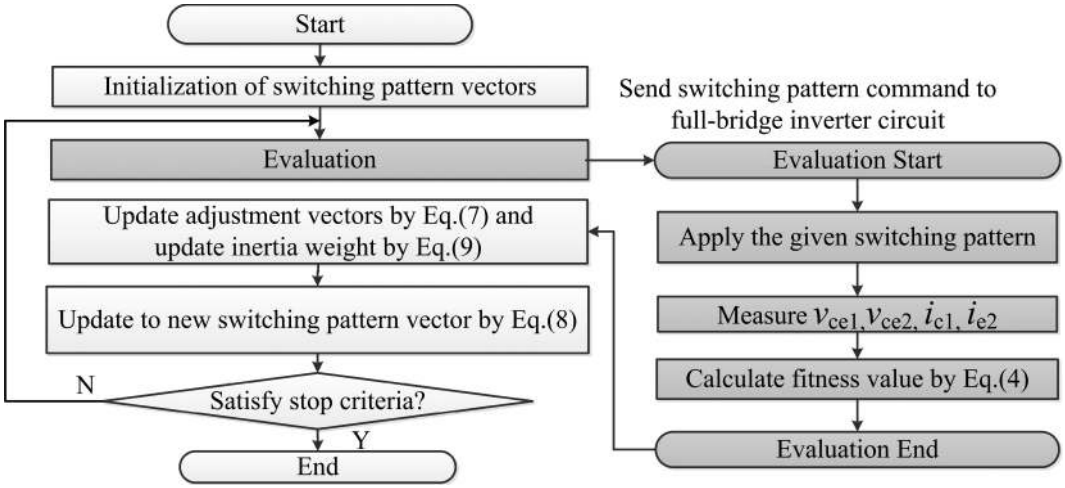


Fig. 4. PSO flowchart and actual measurement for evaluation.

iteration is usually required. A population-based algorithm PSO uses multiple particles/agents, so it is capable of giving a quicker convergence toward the optimum [26]. From the viewpoint of online optimization with an inverter circuit, the high efficiency searching is particularly desired because long time operation might cause temperature rise and change the characteristics of the searching space. In addition, the variants of voltage or current also has impacts on optimal results. The shorter searching time can increase the feasibility of substantial online optimization experiments. In PSO, each particle is regarded as a possible solution in a 60-dimensional space with ranges from 0 to 63 individually. The goal is to reduce switching loss $E_{\rm Loss}$ in (2) while constraining surge voltage $V_{\rm surge}$ in (3). Fig. 2 shows the definitions of these two evaluation indicators graphically

$$E_{\rm Loss} = E_{\rm Q1} + E_{\rm Q2} = \int v_{\rm ce1} i_{\rm c1}\, dt + \int v_{\rm ce2} i_{\rm e2}\, dt \tag{2}$$

$$V_{\rm surge} = \begin{cases} \max(v_{\rm ce2}) - V_{\rm in}, \text{ when } Q1 \text{ turn-on} \\ \max(v_{\rm ce1}) - V_{\rm in}, \text{ when } Q2 \text{ turn-on} \end{cases}. \tag{3}$$

To quantify the performance of the switching behavior, the objective function is formulated as (4). The evaluated indicators $V_{\rm surge}$ and $E_{\rm Loss}$ are normalized using (5) and (6), respectively, to prevent an unbalanced term while searching

$$f_{\rm objective} = V'_{\rm surge} + E'_{\rm Loss} \tag{4}$$

$$V'_{\rm surge} = \frac{V_{\rm surge} - V_{\rm surge,min}}{V_{\rm surge,max} - V_{\rm surge,min}} \tag{5}$$

$$E'_{\rm Loss} = \frac{E_{\rm Loss} - E_{\rm Loss,min}}{E_{\rm Loss,max} - E_{\rm Loss,min}}. \tag{6}$$

The subscript max/min indicates the maximum/minimum of the corresponding quantity. The maximum $V_{\rm surge}$ and minimum $E_{\rm Loss}$ are obtained by applying full constant driving levels $\mathbf{x} = [63,\ 63,\ 63, ...63]$. The minimum $V_{\rm surge}$ and maximum $E_{\rm Loss}$ are obtained by applying low constant driving levels $\mathbf{x} = [3,\ 3,\ 3, ...3]$. The fitness value of each trial switching vector is calculated using (4). To approach toward better fitness value, there is motivation, known as velocity in PSO, attracting particles to move in the searching space. As defined in (7), the velocity vector is determined from the historical experience of each particle denoted as pBest and the best in the group represented as gBest. In order to accelerate convergence, the inertia weight ω is decreased with each iteration using (9). The PSO algorithm was implemented to demonstrate the feasibility of the proposed system at the first place

$$v_{mn}(k+1) = \omega v_{mn}(k) + c_1 r_1 [pBest_{mn} - x_{mn}(k)] + c_2 r_2 [gBest_{mn} - x_{mn}(k)] \tag{7}$$

$$x_{mn}(k+1) = x_{mn}(k) + v_{mn}(k+1) \tag{8}$$

where k is iteration counter, m is the particle counter, n is the element counter of a particle, ω is the inertia weight parameter, c_1 and c_2 are acceleration constants, r_1 and r_2 are uniform random values in [0, 1], $v_{mn}(k)$ is the velocity of particle m at iteration k, and $x_{mn}(k)$ is the current position of particle m at iteration k

$$w = w_{\max} - \frac{w_{\max} - w_{\min}}{\text{iter}_{\max}} \times k \tag{9}$$

where $w_{\max}$ is the maximum inertia weight, $w_{\min}$ is the minimum inertia weight, k is current iteration, and $\text{iter}_{\max}$ is the maximum number of iteration. Fig. 4 presents the optimization flowchart including the update of trial switching patterns and actual measurements for evaluation. Particles would eventually converge to the optimal solution through iterative update and adjustment.

IV. Experimental Results

Fig. 5 shows the proposed optimization system and Fig. 6 shows the interface to set the optimization parameters and monitor the resulting switching waveforms. The new trial pattern and the most advantageous pattern in history during optimization are also given in Fig. 6. The configuration in Table I is used

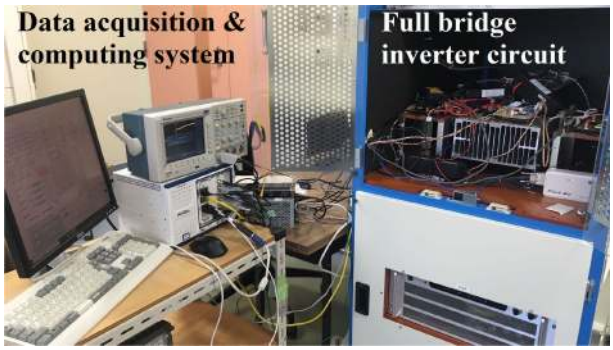


Fig. 5. Picture of the experimental system.

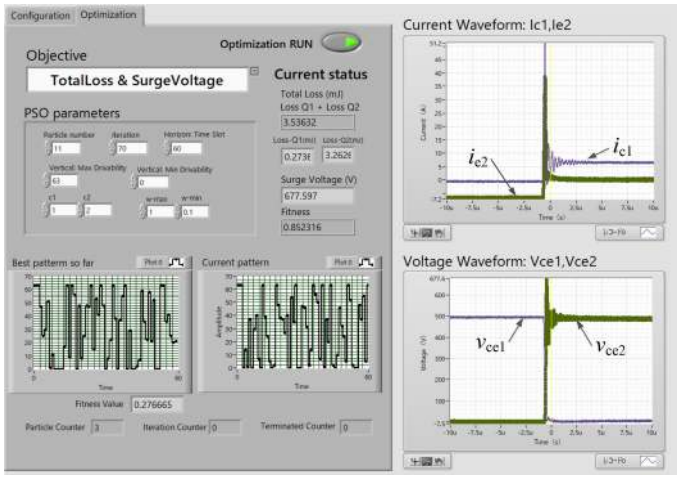


Fig. 6. LabView user interface.

TABLE I
PARAMETERS FOR CIRCUIT EXPERIMENTS

Circuit Parameters		PSO Parameters			
Input voltage V_{in}	500 V	particles	11	$iter_{\max}$	70
Inductor load L	3.2 mH	$x_{\text{mn,max}}$	63	c_1	1
Load current i	8A/-8A	$x_{\text{mn,min}}$	0	c_2	1
Switching frequency	10 kHz	$v_{\text{mn,max}}$	10	$w_{\max}$	1
Deadtime	5 μs	$v_{\text{mn,min}}$	-10	$w_{\min}$	0.1

in the actual experiment. In the searching process, each evaluation loop generates a trial switching pattern every 1 s, then measures the resulting waveforms, and computes the next trial switching pattern. At the end, the total consuming time is less than 15 min to obtain the optimal switching pattern. Compared to the previous research [19], searching time is shorten from 1.5 h to 15 min, which is 6 times faster and becomes beneficial to conduct many times of optimization. Though the investigated circuit and the number decision variables are different, the reduction of searching time helps substantial optimizations under various current conditions and increases efficiency. Three certain switching conditions are demonstrated with conventional and optimal switching patterns: first, turn-ON event of Q_1 when $i = 8$ A, second, turn-ON event of Q_2 when $i = -8$ A, and third, different load current conditions when $i = 2.5$ A and $i = 5$ A. Multiple optimization results are presented to ensure

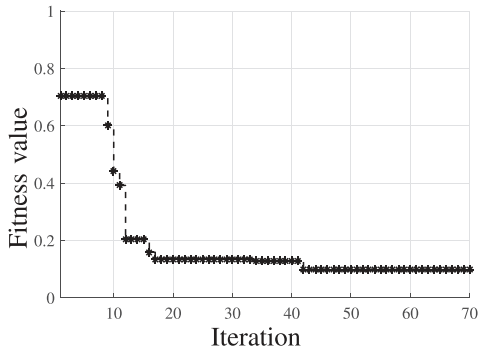


Fig. 7. Convergence history.

TABLE II
COMPARISON OF CONVENTIONAL SWITCHING PATTERN AND OPTIMAL SWITCHING PATTERN FOR Q_1 TURN-ON EVENT WHEN $i = 8$ A

	V_{surge}	E_{Loss}	V'_{surge}	E'_{Loss}	$f_{\text{objective}}$
Constant level 63	300 V (60%)	3.05 mJ	1.00	0.00	1.00
Constant level 3	0 V (0%)	5.70 mJ	0.00	1.00	1.00
Optimal pattern	1 V (0.2%)	3.32 mJ	0.00	0.10	0.10

the searching capability under various PWM operations of an inverter circuit. In other words, for a sinusoidal output current of an inverter, the proposed platform is able to collect all the proper switching patterns corresponding to each load current condition. In addition, all of the optimizations are carried out in the actual inverter circuit rather than a testing circuit. Individual optimization is carried out for each case and the results are presented as below.

A. *Turn-ON Event of Q_1 When $i = 8$ A*

Fig. 7 shows the convergence history and validates the effectiveness of the proposed online optimization system. Hereby, to compare with conventional driving technique, switching waveforms using constant driving level 63 and constant driving level 3 are given in Fig. 8(a) and (b), respectively. Fig. 8(c) shows the switching waveforms when applying the optimal switching pattern. The gate voltage for Q_1 is shaped using the optimized switching pattern. The surge voltage of v_{ce2} is suppressed to 1 V, which is nearly the minimum surge voltage as using low constant driving level 3. Fig. 9 shows the corresponding switching loss of each driving pattern. Most of the switching losses are derived from Q_1 due to hard-switching operation. The duration of switching transient has great impact on the switching loss. Therefore, constant driving level 3 defined the maximum E_{Loss} and minimum V_{surge}, while constant driving level 63 defined the maximum V_{surge} and minimum E_{Loss}. The tradeoff relation between V_{surge} and E_{Loss} is given in Table II. Compared to switching performance of constant driving level 3 where the similar minimum surge voltage has been achieved, the optimal pattern yields up to 42% reduction in the total switching loss.

B. *Turn-ON Event of Q_2 When $i = -8$ A*

Switching pattern optimization was also carried out for the turn-ON event of Q_2 when $i < 0$. The conventional driving pattern

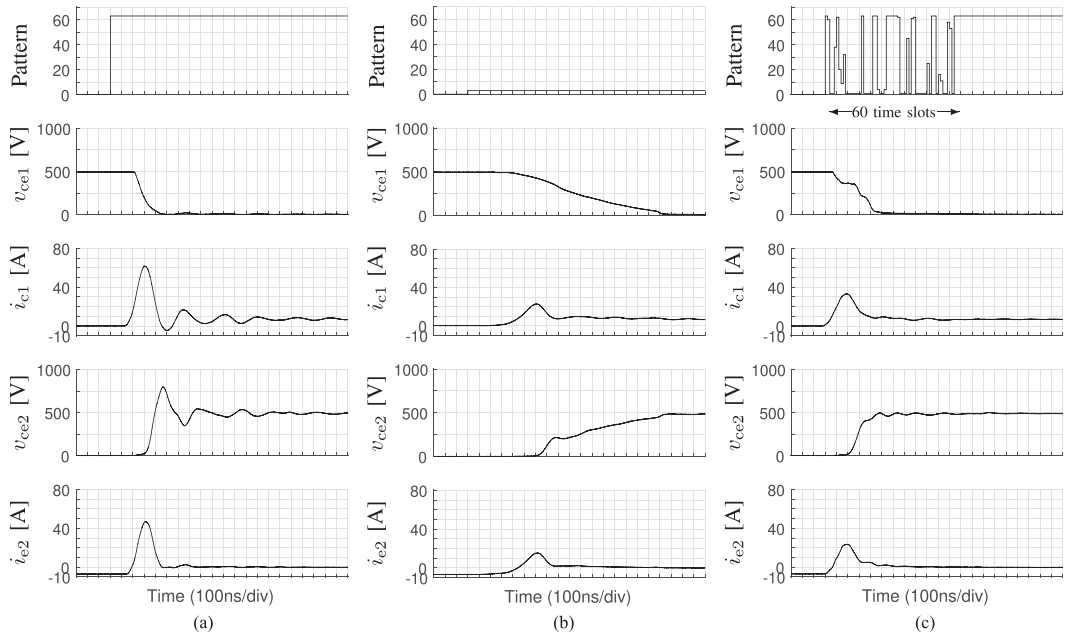


Fig. 8. Implementation of two different driving patterns for Q_1 turn-ON event when $i = 8$ A. (a) Constant driving level 63. (b) Constant driving level 3. (c) Optimal switching pattern.

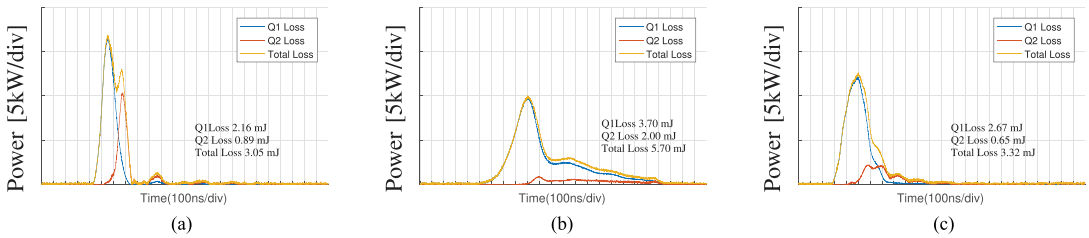


Fig. 9. Switching loss breakdown for Q_1 turn-ON event when $i = 8$ A. (a) Constant driving level 63. (b) Constant driving level 3. (c) Optimal switching pattern.

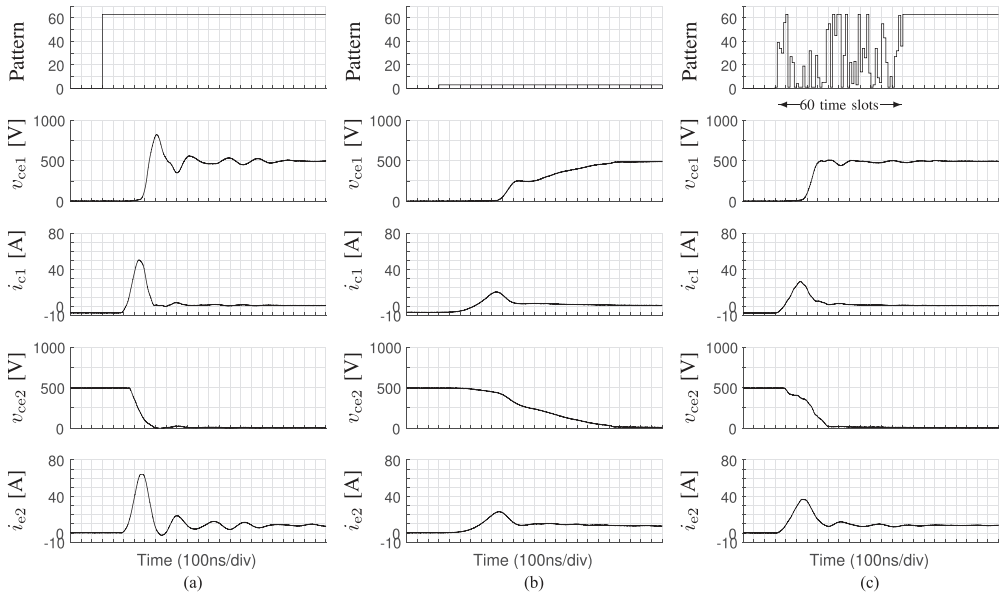


Fig. 10. Implementation of two different driving patterns for Q_2 turn-ON event $i = -8$ A. (a) Constant driving level 63. (b) Constant driving level 3. (c) Optimal switching pattern.

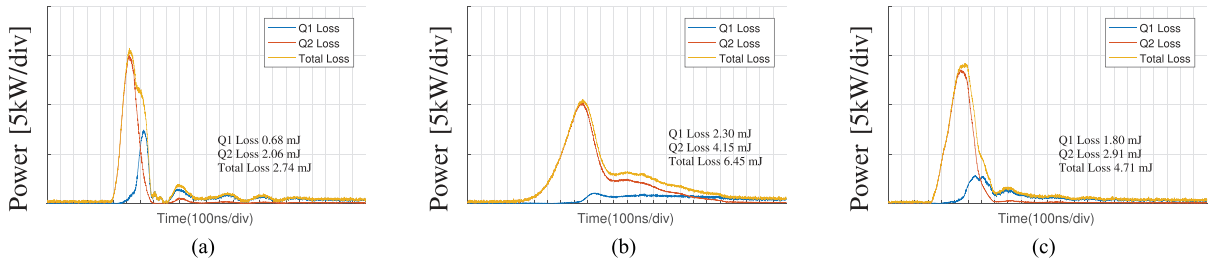


Fig. 11. Switching loss breakdown for Q_2 turn-ON event when $i = -8$ A. (a) Constant driving level 63. (b) Constant driving level 3. (c) Optimal switching pattern.

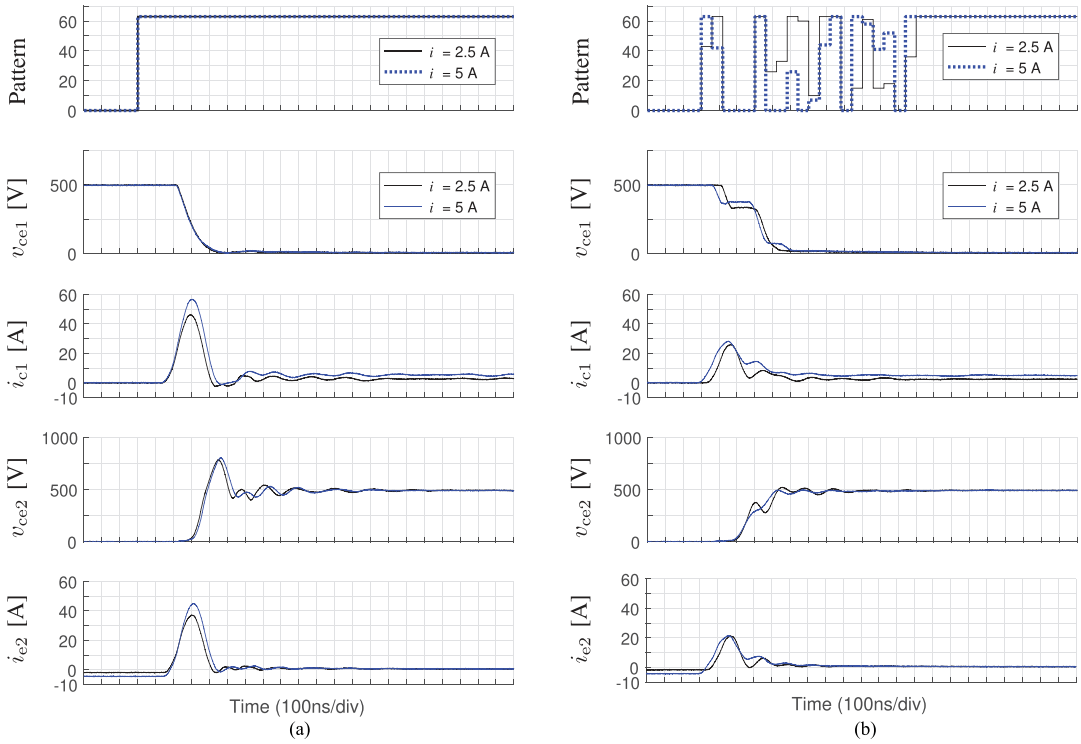


Fig. 12. Demonstration of (a) conventional switching results with full driving level and (b) optimization results under different load currents when $i = 2.5$ A and $i = 5$ A. (a) Conventional switching pattern. (b) Optimal switching pattern.

TABLE III
COMPARISON OF CONVENTIONAL SWITCHING PATTERN AND OPTIMAL SWITCHING PATTERN FOR Q_2 TURN-ON EVENT WHEN $i = -8$ A

	V_{surge}	E_{Loss}	V'_{surge}	E'_{Loss}	$f_{\text{objective}}$
Constant level 63	324 V (64.8%)	2.74 mJ	1.00	0.00	1.00
Constant level 3	0 V (0%)	6.45 mJ	0.00	1.00	1.00
Optimal pattern	9 V (1.8%)	4.71 mJ	0.03	0.53	0.56

was applied as shown in Fig. 10(a) with constant driving level 63 and in Fig. 10(b) with constant driving level 3. Fig. 10(a) shows that there is a 324 V v_{ce1} surge voltage. With the optimized switching pattern shown in Fig. 10(c), Q_2 gate voltage is shaped according to the optimal switching pattern and 9 V of v_{ce1} surge voltage is obtained. Fig. 11 shows the corresponding switching loss of each driving pattern. Most of the switching losses are derived from Q_2 due to hard-switching operation. The tradeoff relation between V_{surge} and E_{Loss} is also given in Table III. The optimal pattern strikes a fine balance where V_{surge} is suppressed to 1.8% and E_{Loss} is also reduced to 4.71 mJ compared to conventional driving.

C. Different Load Current Conditions

To validate the capability of collecting optimal driving patterns under different load current conditions, optimization results are demonstrated in Fig. 12 when load current $i = 2.5$ A and $i = 5$ A. Fig. 12(a) shows the variance of switching transient under different load current conditions. With identical full driving level, waveforms of load current $i = 5$ A presents higher surge voltage in v_{ce2} and higher surge current in i_{c1}. Though the searching space alters with circuit operations, the proposed system can perform optimization regardless of the load current conditions. It can be observed from Fig. 12(b) that surge voltage in v_{ce2}, surge current in i_{c1}, and reverse recovery current of i_{e2} are successfully constrained when applying optimal pattern. In addition, from Fig. 12(b), optimal patterns have some features

in common. At the first 120 ns of pattern profile, there are high driving levels. Then, it is followed by low driving level or even zero level. Generally, the obtained optimal patterns have this characteristic. Hence, it is deduced that the certain shape of profile is critical to suppress the surge voltage.

V. Conclusion

This paper has realized an optimization platform to search the optimal switching pattern for a full-bridge inverter circuit with a digital active gate driver. In the case of using the digital active gate driver, the individual controllability of the driving waveforms results in an extremely large number of possible switching patterns. To extract the maximum benefit from the digital active gate drive control, an optimization system that searches for the proper switching pattern is proposed. The proposed optimization platform is identified to assist product development to fully apply the active gate drive IC in actual inverter circuit.

A 500 V, 20 A full-bride inverter circuit is implemented and served as an investigated circuit for optimal switching pattern. In addition, the proposed optimization system is able to obtain optimal switching pattern from 64^{60} possible combinations of switching patterns within 15 min. Eventually, the obtained optimal pattern yields up to 42% reduction in the total switching loss when it constrains surge voltage to minimum compared with the conventional driving pattern.

References

[1] V. Benda, J. Gowar, and D. A. Grant, *Discrete and Integrated Power Semiconductor Devices: Theory and Applications.* Hoboken, NJ, USA: Wiley, 1999.

[2] R. Barrera-Cardenas, T. Isobe, and M. Molinas, "A meta-parameterized approach for the evaluation of semiconductor technologies," *IEEJ J. Ind. Appl.*, vol. 7, no. 3, pp. 210–217, 2018.

[3] A. J. Charpentier, A. K. Smith, N. Satheesh, and R. Weber, "Gate drive control system for SiC and IGBT power devices," U.S. Patent 9 490 798, Nov. 8, 2016.

[4] K. Yamaguchi, K. Katsura, T. Yamada, and Y. Sato, "Comprehensive study on gate driver for SiC-MOSFETs with gate boost," *IEEJ J. Ind. Appl.*, vol. 7, no. 3, pp. 218–228, 2018.

[5] Y. Lobsiger and J. W. Kolar, "Closed-Loop di/dt and dv/dt IGBT gate driver," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 3402–3417, Jun. 2015.

[6] A. Schindler, B. Koeppl, B. Wicht, and J. Groeger, "10 ns Variable current gate driver with control loop for optimized gate current timing and level control for in-transition slope shaping," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 3570–3575.

[7] X. Yang, Y. Yuan, X. Zhang, and P. R. Palmer, "Shaping high-power IGBT switching transitions by active voltage control for reduced EMI generation," *IEEE Trans. Ind. Appl.*, vol. 51, no. 2, pp. 1669–1677, Mar./Apr. 2015.

[8] B. Sun, R. Burgos, X. Zhang, and D. Boroyevich, "Active dv/dt control of 600V GaN transistors," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1–8.

[9] H. C. P. Dymond *et al.*, "A 6.7-GHz active gate driver for GaN FETs to combat overshoot, ringing, and EMI," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 581–594, Jan. 2018.

[10] J. J. O. Dalton *et al.*, "Shaping switching waveforms in a 650 V GaN FET bridge-leg using 6.7 GHz active gate drivers," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 1983–1989.

[11] H. Obara, K. Wada, K. Miyazaki, M. Takamiya, and T. Sakurai, "Active gate control in half-bridge inverters using programmable gate driver ICs to improve both surge voltage and converter efficiency," *IEEE Trans. Ind. Appl.*, vol. 54, no. 5, pp. 4603–4611, Sep./Oct. 2018.

[12] N. Oswald, B. H. Stark, D. Holliday, C. Hargis, and B. Drury, "Analysis of shaped pulse transitions in power electronic switching waveforms for reduced EMI generation," *IEEE Trans. Ind. Appl.*, vol. 47, no. 5, pp. 2154–2165, Sep./Oct. 2011.

[13] L. Dang, H. Kuhn, and A. Mertens, "Digital adaptive driving strategies for high-voltage IGBTs," *IEEE Trans. Ind. Appl.*, vol. 49, no. 4, pp. 1628–1636, Jul./Aug. 2013.

[14] D. J. Rogers and B. Murmann, "Digital active gate drives using sequential optimization," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2016, pp. 1650–1656.

[15] M. Blank, T. Glck, A. Kugi, and H. Kreuter, "Digital slew rate and s-shape control for smart power switches to reduce EMI generation," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 5170–5180, Sep. 2015.

[16] New Gate Driver Core Optimized for SiC MOSFET Modules. 2018, Accessed: Oct. 31, 2018. [Online] Available at: http://agileswitchnews.blogspot.com/2018/05/new-gate-driver-core-optimized-for-sic.html

[17] W. Frank, A. Arens, and S. Hoerold, "Real-time adjustable gate current control IC solves dv/dt problems in electric drives," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, 2014, pp. 1–7.

[18] K. Miyazaki *et al.*, "General-purpose clocked gate driver IC with programmable 63-level drivability to optimize overshoot and energy loss in switching by a simulated annealing algorithm," *IEEE Trans. Ind. Appl.*, vol. 53, no. 3, pp. 2350–2357, May/Jun. 2017.

[19] K. Miyazaki, M. Takamiya, and T. Sakurai, "Automatic optimization of IGBT gate driving waveform using simulated annealing for programmable gate driver IC," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1–6.

[20] G. Jones and D. Rogers, "Investigation of IGBT switching energy loss and peak overvoltage using digital active gate drives," in *Proc. IEEE Workshop Control Model. Power Electron.*, 2017, pp. 1–8.

[21] H. C. P. Dymond, J. J. O. Dalton, and B. H. Stark, "Rapid co-optimisation of turn-on and turn-off gate resistor values in DC:DC power converters," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 5357–5364.

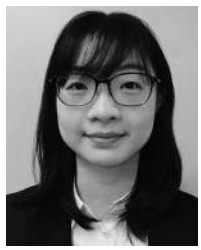
[22] J. J. O. Dalton *et al.*, "Stretching in time of GaN active gate driving profiles to adapt to changing load current," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 3497–3502.

[23] T. Mannen, K. Wada, H. Obara, K. Miyazaki, M. Takamiya, and T. Sakurai, "Active gate control for switching waveform shaping irrespective of the circuit stray inductance in a practical full-bridge IGBT inverter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 3108–3113.

[24] Y. S. Cheng, T. Mannen, K. Wada, K. Miyazaki, M. Takamiya, and T. Sakurai, "Optimization system to find a switching pattern of digital active gate drive for full-bridge inverter circuit," presented at the IEEE Energy Convers. Congr. Expo., 2018, pp. 6441–6447.

[25] J. Kennedy and R. Eberhart, "Particle swarm optimization," in *Proc. IEEE Int. Conf. Neural Netw.*, 1995, vol. 4, pp. 1942–1948.

[26] X.-S. Yang, *Nature-Inspired Optimization Algorithms.* Amsterdam, The Netherlands: Elsevier, 2014.



Yu Shan Cheng received the B.S. and Ph.D. degrees in electrical engineering from the National Taiwan University of Science and Technology, Taipei, Taiwan, in 2012 and 2017, respectively.

From 2015 to 2016, she was with the Technical University of Munich, Munich, Germany, as a Visiting Scholar. From 2017, she works as a Project Researcher with Tokyo Metropolitan University, Tokyo, Japan. Her current research interests include power management of renewable energy systems, metaheuristic optimization, and power converters.

Tomoyuki Mannen (S'13–M'17) received the B.S., M.S., and the Ph.D. degrees from the Tokyo Institute of Technology, Tokyo, Japan, in 2012, 2014, and 2017, respectively, all in electrical engineering.

He joined Tokyo Metropolitan University, Tokyo, Japan, as a Postdoctoral Researcher in 2017, and moved to the Tokyo University of Science in 2018 as an Assistant Professor. Since 2019, he has been an Assistant Professor with the Department of Applied Physics, University of Tsukuba, Tsukuba, Japan. His research interests include grid-connection converters, active power filters, and its control methods.

Dr. Mannen was the recipient of the Institute of Electrical Engineers of Japan Industry Application Society Conference Paper Presentation Award in 2013 and 2017, and the IEEJ Technical Meeting Presentation Award in 2015. He was also the recipient of a Committee Prize Paper Award from the IEEE Industry Applications Society Industrial Power Converter Committee in 2016.

Keiji Wada was born in Hokkaido, Japan. He received the Ph.D. degree in electrical engineering from Okayama University, Okayama, Japan, in 2000.

From 2000 to 2006, he was an Assistant Professor with Tokyo Metropolitan University, and the Tokyo Institute of Technology. Since 2006, he has been an Associate Professor with Tokyo Metropolitan University. His current research interests include medium-voltage inverter, electromagnetic interference filters, and power converter circuit.

Dr. Wada is a senior member of IEEJ.

Koutarou Miyazaki (S'16–M'17) received the B.S., M.S., and Ph.D. degrees in electrical engineering and information systems from The University of Tokyo, Tokyo, Japan, in 2012, 2014, and 2017, respectively.

In 2017, he was a Project Researcher with the Institute of Industrial Science, The University of Tokyo. In 2019, he joined the Corporate Research and Development Center, Toshiba Corporation, Kawasaki, Japan, where he has been involved in the research and development of digital gate driver and short-circuit protection of insulated-gate bipolar transistor.

Makoto Takamiya (S'98–M'00–SM'14) received the B.S., M.S., and Ph.D. degrees in electronic engineering from The University of Tokyo, Tokyo, Japan, in 1995, 1997, and 2000, respectively.

In 2000, he joined NEC Corporation, Japan, where he was engaged in the circuit design of high speed digital LSI's. He joined The University of Tokyo in 2005, where he is currently a Professor with the Institute of Industrial Science. From 2013 to 2014, he was with the University of California, Berkeley, as a Visiting Scholar. His research interests include the integrated power management circuits for wireless powering and energy harvesting for wearable and IoT applications, and the digital gate driver IC for power electronics.

Dr. Takamiya is a member of the technical program committee of the IEEE International Solid-State Circuits Conference (ISSCC) and is a Far East Regional Chair in ISSCC 2020. He is a Distinguished Lecturer of the IEEE Solid-State Circuits Society. He formerly served on the technical program committees of IEEE Symposium on VLSI Circuits from 2009 to 2017 and IEEE Custom Integrated Circuits Conference from 2006 to 2011. He was the recipient of the 2009 and 2010 IEEE Paul Rappaport Awards and the Best Paper Award in 2013 IEEE Wireless Power Transfer Conference.

Takayasu Sakurai (S'77–M'78–SM'01–F'03) received the Ph.D. degree in electrical engineering from The University of Tokyo, Tokyo, Japan, in 1981.

In 1981, he joined Toshiba Corporation, where he designed CMOS DRAM, SRAM, RISC processors, DSPs, and system-on-chip solutions. He focused extensively on interconnect delay and capacitance modeling known as Sakurai model and alpha power-law MOS model. From 1988 to 1990, he was a Visiting Researcher with the University of California, Berkeley, where he conducted research in the field of very large-scale integration (VLSI) CAD. Since 1996, he was a Professor with The University of Tokyo, focusing on low-power high-speed VLSI, memory design, interconnects, ubiquitous electronics, organic ICs, and large-area electronics. He is currently a Professor Emeritus and a Senior Research Fellow with The University of Tokyo. He has authored or coauthored more than 600 technical publications including 100 invited presentations and several books and filed more than 200 patents.

Dr. Sakurai is an IEICE Fellow. He was a recipient of the 2010 IEEE Donald O. Pederson Award in Solid-State Circuits, the 2009 and 2010 IEEE Paul Rappaport Award, the 2010 IEICE Electronics Society Award, the 2009 IEICE Achievement Award, the 2005 IEEE ICICDT Award, the 2004 IEEE Takuo Sugano Award, and the 2005 P&I Patent of the Year Award, and four product awards. He was the Executive Committee Chair of the VLSI Symposia and a Steering Committee Chair of the IEEE A-SSCC. He served as a Conference Chair for the Symposium on VLSI Circuits and ICICDT, a Vice Chair for ASPDAC, a TPC Chair for the A-SSCC and the VLSI Symposium, an Executive Committee Member for ISLPED, and a Program Committee Member for ISSCC, CICC, A-SSCC, DAC, ESSCIRC, ICCAD, ISLPED, and other international conferences. He delivered keynote speech at more than 50 conferences, including ISSCC, ESSCIRC, and ISLPED. He was an Elected AdCom Member of the IEEE Solid-State Circuits Society and an IEEE CAS and SSCS Distinguished Lecturer. He is also a Domain Research Supervisor for nanoelectronics area with the Japan Science and Technology Agency.