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► **To cite this version:**

Maryam Shayesteh, Dan O'Connell, Farzan Gity, Philip Murphy-Armando, Ran Yu, et al.. Optimized Laser Thermal Annealing on Germanium for High Dopant Activation and Low Leakage Current. IEEE Transactions on Electron Devices, Institute of Electrical and Electronics Engineers, 2014, 61 (12), pp.4047 - 4055. 10.1109/ted.2014.2364957 . hal-01921394

**HAL Id: hal-01921394**

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Submitted on 13 Nov 2018

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# Optimized Laser Thermal Annealing on Germanium for High Dopant Activation and Low Leakage Current

Maryam Shayesteh, Dan O' Connell, Farzan Gity, *Student Member, IEEE*, Philip Murphy-Armando, Ran Yu, Karim Huet, Ines Toqué-Tresonne, Fuccio Cristiano, Simona Boninelli, Henrik Hartmann Henrichsen, Peter Folmer Nielsen, Dirch Hjorth Petersen, and Ray Duffy

**Abstract**—In this paper, state-of-the-art laser thermal annealing is used to fabricate Ge diodes. We compared the effect of laser thermal annealing (LTA) and rapid thermal annealing (RTA) on dopant activation and electrical properties of phosphorus and Arsenic-doped n+/p junctions. Using LTA, high carrier concentration above  $10^{20} \text{ cm}^{-3}$  was achieved in n-type doped regions, which enables low access resistance in Ge devices. Furthermore, the LTA process was optimized to achieve a diode  $I_{\text{ON}}/I_{\text{OFF}}$  ratio  $\sim 10^5$  and ideality factor ( $n$ )  $\sim 1.2$ , as it allows excellent junction depth control when combined with optimized implant conditions. On the other hand, RTA revealed very high  $I_{\text{ON}}/I_{\text{OFF}}$  ratio  $\sim 10^7$  and  $n \sim 1$ , at the cost of high dopant diffusion and lower carrier concentrations which would degrade scalability and access resistance.

**Index Terms**—Ge, laser thermal annealing (LTA), leakage current, n+/p junction.

## I. INTRODUCTION

INDEED, many obstacles and challenges need to be addressed before Ge can become a forefront element in advanced CMOS technology. Realization of n-type ultrashallow junctions with highly activated dopants to maintain low

access resistance is a well-known roadblock on this journey. Meanwhile, the relatively small bandgap (0.67 eV) of Ge raises difficulties to minimize the leakage current in pn junctions [1]. Various approaches have been developed to solve these issues among which ultrafast laser thermal annealing (LTA) has drawn a lot of interest [2]–[6]. Providing very limited thermal budgets, LTA has been proven to surpass conventional rapid thermal annealing (RTA) as it boosts activation levels of the dopants well above the equilibrium limit while suppressing dopant diffusion [6]–[9]. Leakage current behavior in p+/n and n+/p Ge junctions has been extensively analyzed [10]–[13]. However, the efficiency of the LTA technique on the control of leakage current in Ge junctions is not fully investigated [14].

The aim of this paper is to systematically compare RTA and LTA with respect to dopant activation and electrical performance of the n+/p junction. Moreover, we aim to explore the tradeoff between dopant activation and leakage current. To fully evaluate these thermal processes, we combine a wide range of material characterization with extensive electrical characterization. In this way, we explore surface roughness and morphology, crystalline integrity, carrier profiling, sheet resistance, and carrier mobility in doped layers, as well as leakage current levels and generation mechanisms.

## II. EXPERIMENTAL DETAILS

Fig. 1 shows a summary of the process flow in this experiment. Ge (100) wafers (p-type, 0.059–0.088  $\Omega \text{ cm}$ ) received standard cleaning prior to either P or As implant with the dose of  $10^{15} \text{ cm}^{-2}$  and the energy of 15 and 28 keV, respectively. The P implantation amorphized the Ge substrate to a depth of 30–35 nm which is 35–40 nm for As. It is a feature of Ge substrates that the amorphous/crystalline (a/c) interface is not smooth after ion implantation. Following implantation, LTA (single pulse,  $\lambda = 308 \text{ nm}$ ) was applied on one set of samples at  $E_{\text{TH}} = 0.55 \text{ J/cm}^2$ ,  $E_{\text{TH}} + 0.25$ ,  $E_{\text{TH}} + 0.5$ , and  $E_{\text{TH}} + 0.65 \text{ J/cm}^2$  energy densities to cure the crystal damage and electrically activate the dopants. We define the threshold energy  $E_{\text{TH}}$  as the onset where the Ge surface begins to melt. It is known that changing the energy density changes the melt depth at the Ge surface. Each LTA shot covered an area of  $1 \text{ cm} \times 1 \text{ cm}$  over 158–164 ns of exposure time. One P- and one As-implanted samples were subjected to RTA at 500 °C in  $N_2$  for 3 min as a control

Manuscript received June 30, 2014; revised October 3, 2014; accepted October 21, 2014. Date of publication November 4, 2014; date of current version December 9, 2014. This work was supported in part by the Science Foundation Ireland under Grant 09/SIRG/11623 and Grant 09/SIRG/11621, and in part by the Higher Education Authority Programme for Research in Third-Level Institutions. The review of this paper was arranged by Editor H. Shang.

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Digital Object Identifier 10.1109/TED.2014.2364957

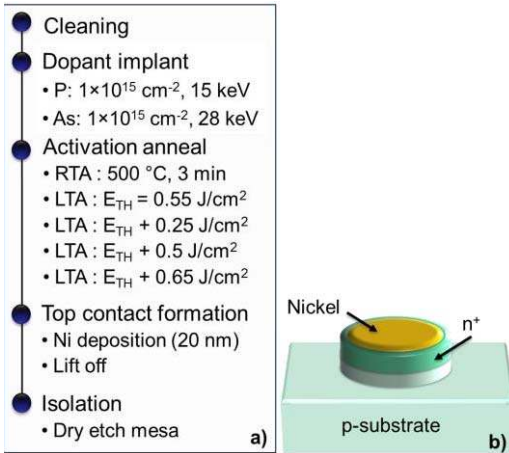


Fig. 1. (a) Summary of the experimental process flow in this paper. (b) Fabricated and characterized diode test structure.

case. Diodes were subsequently fabricated from P-implanted samples. The top contact was formed by evaporation of 20 nm nickel and then patterned by a liftoff process. The diodes were isolated from each other by dry etching of a mesa with 600–700 nm height [Fig. 1(b)]. No germanidation annealing was performed. Ioannou-Sougliridis *et al.* [15] reported enhanced leakage current caused by diffusion of Pt atoms into the depletion region during germanide formation. Fig. 1(b) shows a schematic of the fabricated and characterized circular diodes ranging from 100 to 500  $\mu\text{m}$  diameter.

The first stage of material characterization involved examination of the surface topography. Atomic force microscopy (AFM) was performed in noncontact tapping mode at room temperature on  $5 \mu\text{m} \times 5 \mu\text{m}$  area for surface examination and surface roughness measurements (RMS) before and after the annealing process. Scanning electron microscopy (SEM) was performed on an FEI 650 FEG SEM to inspect the surfaces and test structures. Then, cross-sectional transmission electron microscopy (TEM) was carried out to monitor the crystal integrity by using a 200 keV JEOL 2010-HC TEM for the defect analysis, performed under weak beam dark field (WBDF) conditions, and a 200 keV JEOL 2010F for high-resolution imaging. For carrier profiling, secondary ion mass spectrometry (SIMS) was done on a CAMECA IMS 4FE6 system, available at the UMS-CNRS Castaing characterisation centre of Toulouse, to obtain the chemical concentration of the dopants, and electrochemical capacitance voltage (ECV) profiling was performed to determine active carrier concentration of the samples. The last stage of material characterization concerned Hall sheet carrier concentration ( $N_{HS}$ ), mobility ( $\mu_H$ ), and sheet resistance ( $R_S$ ) measurements which was done using a microHALL-M300 tool at CAPRES A/S. Several measurements were acquired on each sample for statistical average values.

### III. RESULTS AND DISCUSSION

#### A. Material Characterization

The samples were initially examined with AFM to inspect the effect of LTA on the surface morphology. After implantation, the RMS was approximately 0.3 nm.

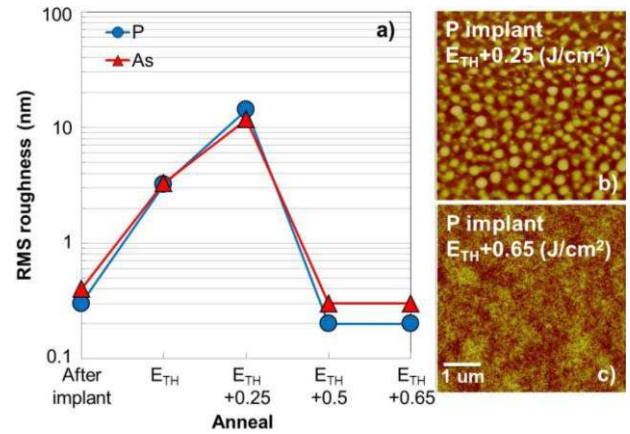


Fig. 2. (a) Surface roughness versus laser energy for P and As samples. Example AFM images of P-implanted samples treated by LTA at (b)  $E_{TH} + 0.25 \text{ J/cm}^2$  and (c)  $E_{TH} + 0.65 \text{ J/cm}^2$ .

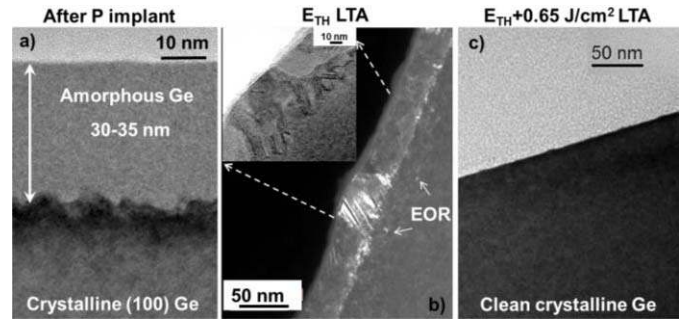


Fig. 3. Representative TEM images of (a) amorphous and crystalline interface in Ge with 30–35 nm amorphous depth after P implant, (b) defective crystalline Ge after  $E_{TH}$  LTA, and (c) crystalline Ge with no visible defects after  $E_{TH} + 0.65 \text{ J/cm}^2$  LTA.

As is reflected in the extracted RMS values shown in Fig. 2(a), the application of LTA in the partial melt regime ( $E_{TH}$  and  $E_{TH} + 0.25 \text{ J/cm}^2$ ) deteriorated the roughness of the surface. It is known that these energy densities can melt in part the amorphous Ge [7]. At  $E_{TH} + 0.5$  and  $E_{TH} + 0.65 \text{ J/cm}^2$  the substrate was melted beyond the amorphous region which resulted in a smooth surface after the LTA process. Fig. 2(b) and (c) shows representative AFM images from P-implanted samples after  $E_{TH} + 0.25 \text{ J/cm}^2$  and  $E_{TH} + 0.65 \text{ J/cm}^2$ , respectively.

From these data, it appears that the higher LTA energy densities are more favorable to reduce the roughness of the surface.

Representative cross-sectional TEM images of the samples are shown in Fig. 3. Fig. 3(a) shows the sample after P implantation with the a/c interface 35 nm below the surface. Fig. 3(b) shows the P-implanted sample after  $E_{TH}$  LTA. As seen in the WBDF image, the previous amorphous layer is crystallized but stacking faults are also formed (as shown in the high-resolution image in the inset) because of poor templated recrystallization. Moreover, the presence of end-of-range (EOR) defects at 40 nm below the surface, behind the previous a/c interface, indicates that the melting arrived just in correspondence of the a/c interface. The

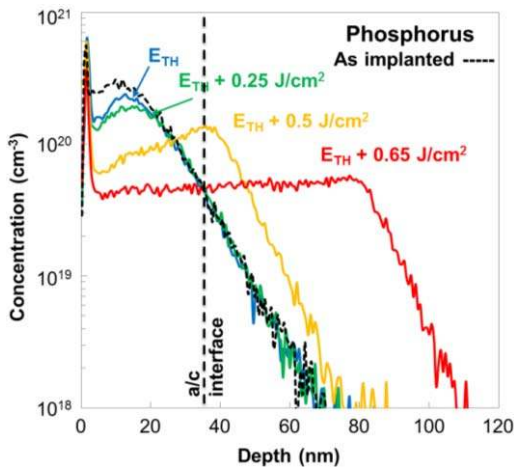


Fig. 4. SIMS profile of P-implanted samples subjected to LTA at energies ranging from  $E_{TH}$  to  $E_{TH} + 0.65 \text{ J/cm}^2$ .

same phenomenon was observed by Tsouroutas *et al.* [6]. Fig. 3(c) shows the P-implanted sample subjected to  $E_{TH} + 0.65 \text{ J/cm}^2$  LTA which resulted in apparently defect-free crystalline Ge. At this energy, Ge is melted beyond the a/c interface.

Once again it appears that the higher thermal budget of the high energy density LTA process is desirable, as fewer crystal defects are evident in the TEM images.

Fig. 4 shows SIMS depth profiles of the P-implanted samples subjected to LTA. The a/c interface is shown by a dashed line. The peak on the surface is probably due to a SIMS artifact. From dose integration of the SIMS profiles, it was determined that 23%–38% of P out-diffused during the  $E_{TH}$  to  $E_{TH} + 0.65 \text{ J/cm}^2$  LTA. Maximum dopant concentration of  $2.4 \times 10^{20} \text{ cm}^{-3}$  was obtained after LTA at  $E_{TH}$ . No evidence of redistribution of dopants for the lowest thermal budget cases ( $E_{TH}$  and  $E_{TH} + 0.25 \text{ J/cm}^2$ ).

As expected, higher laser energies resulted in a deeper junction and more diffusion of dopants into the substrate. Enhanced redistribution of the dopants in molten Ge created a boxlike profile after  $E_{TH} + 0.65 \text{ J/cm}^2$  LTA. In this case, the maximum dopant concentration is reduced down to  $5.3 \times 10^{19} \text{ cm}^{-3}$  owing to diffusion.

Dopant loss could be reduced significantly with a careful optimization of the implant conditions, with a much shallower amorphized depth that requires a shallower melting depth and shorter melting time, which subsequently reduces the out diffusion of dopants. Using a capping layer would also help to reduce the dopant loss, hence maximizing the active carrier concentration. An extensive study by Impellizzeri *et al.* [16] on the effect of LTA on activation of B in Ge proved that incorporation of oxygen coming from the native oxide on the Ge surface can impede electrical activation of dopants, which could also be a concern for leakage if oxygen reaches the depletion region of the junction. Comparison of the equilibrium diffusion coefficient for oxygen in Ge [17] with that of for P and As extracted by Chui *et al.* [18] shows that P and As diffuse faster than oxygen in Ge during the annealing process. For the nonequilibrium

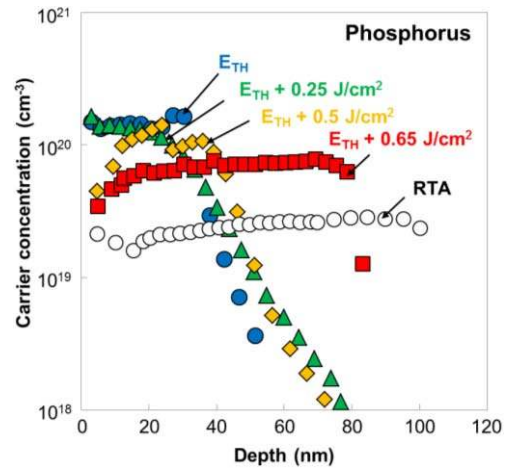


Fig. 5. Active carrier concentration from P-implanted samples obtained by ECV. LTA resulted in higher carrier concentration compared with RTA.

LTA process, we would not expect the oxygen to diffuse faster than the P and As, effectively catching up with the dopants and reaching the depletion region in significant concentration levels.

Fig. 5 shows active dopant concentration versus depth obtained from ECV measurements for P-implanted samples. Comparison of ECV and SIMS profiles for each of the laser energies shows a good agreement between the two techniques. Therefore it appears, within the error bars of the two characterization techniques, all the retained dose of P is activated, with a maximum active concentration of  $1.65 \times 10^{20} \text{ cm}^{-3}$ , close to the result reported by Mazzocchi *et al.* [7] ( $1.2 \times 10^{20} \text{ cm}^{-3}$ ) for P by using similar laser energy densities. Using LTA on Sb-implanted Ge, Thareja *et al.* [8] also achieved carrier concentrations above  $10^{20} \text{ cm}^{-3}$ .

The observed peak at  $\sim 35 \text{ nm}$  in the  $E_{TH}$  LTA is located in the most defective zone of this sample, as found by TEM analysis [Fig. 3(b)] and indicates that the carrier concentration at this depth exceeds the dopant concentration (see SIMS profile, Fig. 4). Similar to what has already been found during B activation in Si after excimer laser annealing [19], it is therefore suggested that the presence of this ECV peak is due to the existing defects rather than to the active dopants. Indeed, the charges measured by ECV are associated with the energy levels distributed in a wide energy range of the bandgap, including those associated with extended defects [20], [21]. Finally, from the ECV profile of the RTA control sample it can be confirmed that RTA resulted in a lower level of active concentration of  $2.7 \times 10^{19} \text{ cm}^{-3}$  and a deeper junction compared to the LTA samples.

Fig. 6 shows SIMS depth profiles of the As-implanted samples subjected to LTA. Here the a/c interface lays 35–40 nm below the surface indicated by the dashed line. Almost no redistribution of dopants is observed at  $E_{TH}$  LTA. Dose integration of the SIMS profile at this energy shows no dopant loss during the LTA process. However, subsequent LTA energies resulted in 10%–20% dose loss. Using  $E_{TH} + 0.65 \text{ J/cm}^2$  LTA a boxlike profile is formed with the melt depth lying about 80 nm below the surface. Here the

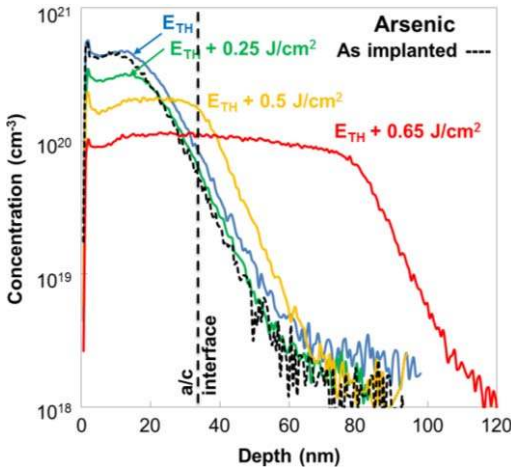


Fig. 6. SIMS profile of As-implanted samples subjected to LTA at energies ranging from  $E_{TH}$  to  $E_{TH} + 0.65 \text{ J/cm}^2$ .

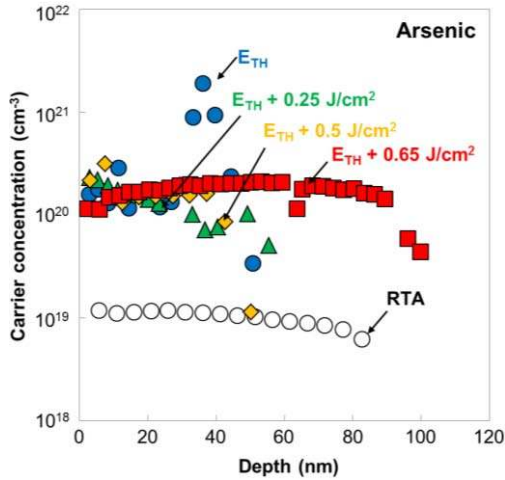


Fig. 7. Active carrier concentration from As-implanted samples obtained by ECV. LTA resulted in higher carrier concentration compared with RTA. The peak in the carrier concentration of the  $E_{TH}$  profile is due to the accumulation of defects in the junction not dopants alone.

plateau concentration is  $>10^{20} \text{ cm}^{-3}$ . Similar to the P samples no observable defects were formed after the amorphized Ge region (including EOR defects) was fully melted and regrown.

Active carrier concentration of the As-doped samples was also measured using the ECV profiling technique as shown in Fig. 7. High active concentrations  $>10^{20} \text{ cm}^{-3}$  were achieved after  $E_{TH}$  LTA on As-implanted samples with a peak concentration of  $10^{21} \text{ cm}^{-3}$  at  $\sim 35 \text{ nm}$ . Several  $E_{TH}$  samples were remeasured to confirm these results. Integrated dose of the  $E_{TH}$  profile is  $>10^{15} \text{ cm}^{-2}$  indicating that the charge is coming not from the dopant but from defects at the original a/c interface similar to what previously discussed for the P-implanted samples (Fig. 5).

As shown for P in Fig. 3, similar trends were obtained for As resulting from the LTA process. Like the P case, higher laser energies resulted in deeper doping profiles and lower levels of dopant concentration owing to diffusion. Again within the error bars of the ECV and SIMS characterization techniques,

TABLE I  
MICRO-HALL EFFECT MEASUREMENTS

Dopant	Anneal ( $\text{J/cm}^2$ )	$\mu_H$ ( $\text{cm}^2/\text{Vs}$ )	$N_{HS}$ ( $\text{cm}^{-2}$ )	$R_s$ ( $\Omega$ )
P	$E_{TH}+0.5$	118	$5.78 \times 10^{14}$	91.8
P	$E_{TH}+0.65$	161	$5.60 \times 10^{14}$	69.4
As	$E_{TH}+0.5$	94	$9.01 \times 10^{14}$	73.9
As	$E_{TH}+0.65$	112	$8.63 \times 10^{14}$	64.5

it appears that all the retained dose of As is activated. As a comparison, Hellings *et al.* [3] reported 13%–26% activation for As-implanted Ge by using millisecond laser annealing. ECV characterization on the control RTA sample shows carrier concentration  $\sim 10^{19} \text{ cm}^{-3}$ . Using excimer laser annealing, Milazzo *et al.* [5] obtained active carrier concentration of As dopant above  $10^{20} \text{ cm}^{-3}$ .

Table I shows the mobility and micro-Hall effect measurements on P- and As-implanted samples after  $E_{TH} + 0.5$  and  $E_{TH} + 0.65 \text{ J/cm}^2$  LTA. Higher laser energy in both sets of samples resulted in improved carrier mobility ( $\mu_H$ ) and also lower sheet resistance ( $R_s$ ). This is consistent with the observations from material studies where the higher laser energy repaired the crystal lattice after the implantation process (Fig. 3). Extracted sheet carrier densities with Hall measurements ( $N_{HS}$ ) is in good agreement with the active integrated concentrations obtained using ECV profiling technique. Active carrier concentration normally increases with increased thermal budget but from these measurements it remains constant. The observed discrepancy in the extracted values may be associated with the out-diffusion of the dopants during the thermal treatment as well as an almost perfect activation of dopants in both cases.

In conclusion, from the material analysis, it is apparent that the best choice of LTA condition depends on a number of factors. At low energy density, we observe a diffusionless high activation of dopants, at a cost of residual defects in the crystal. At high energy density, crystalline integrity is drastically better while maintaining very impressive levels of carrier concentration. However, care must be taken to optimize the process to avoid excessive dopant diffusion.

### B. Electrical Characterization

Fig. 8 shows  $I-V$  characteristics obtained from  $500 \mu\text{m}$  circular diodes processed by LTA and RTA. Because of the similarity in the material characterization trends for P and As implants, we focus on P in the electrical analysis in the remainder of this paper.

The  $E_{TH}$  LTA sample shows poor  $I-V$  characteristics with very high leakage current and ideality factor  $n$  larger than 2. This can be associated with the formation of a defective substrate during the recrystallization process. Annihilation of defects at higher laser energies (Fig. 3) resulted in improved  $I-V$  characteristics.  $I_{ON}/I_{OFF}$  ratio  $>10^4$  was obtained between  $-1$  and  $1 \text{ V}$  for  $E_{TH} + 0.65 \text{ J/cm}^2$ , with  $n = 1.4$ . Note that smaller dimension diodes produced a higher  $I_{ON}/I_{OFF}$  ratio above  $10^5$  with  $n = 1.2$  (Fig. 14).

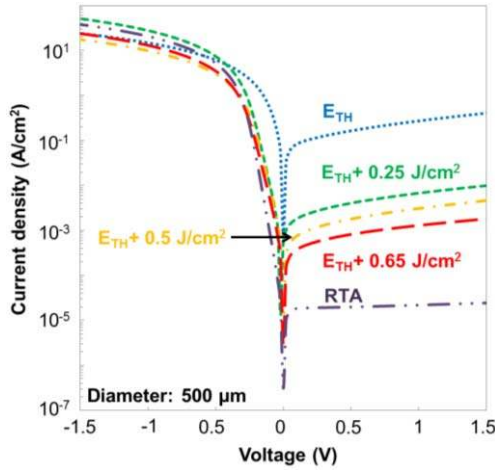


Fig. 8. Diode  $I$ - $V$  characteristics from P-implanted samples treated by RTA and LTA ( $E_{TH}$  -  $E_{TH} + 0.65 \text{ J/cm}^2$ ).

Significantly, RTA diodes showed ideal behavior with  $n = 1.03$  and  $I_{ON}/I_{OFF}$  ratio  $> 10^6$ . From the  $I$ - $V$  characteristics, it can be concluded that there are deep level defects in the n+/p junctions formed by LTA which form generation centers contributing to the leakage current [22]. In the RTA case, on the contrary, long thermal budget cured the defects in the depletion layer and resulted in very low leakage current. Moreover, diffusion of dopants due to the long RTA (compared with LTA) shifted the junction depth beyond the original defective region within the n+ part of the junction so that the remaining defects (if any) would not be located in the depletion region and have an impact on the leakage current. As stated earlier,  $I$ - $V$  measurements were carried out on a large set of diode structures from which perimeter leakage current density ( $J_P$ ) was extracted using

$$I = P \cdot J_P + A \cdot J_A \quad (1)$$

which becomes

$$\frac{I}{A} = \frac{P}{A} \cdot J_P + J_A \quad (2)$$

where  $P$  and  $A$  are, respectively, perimeter and area of the diode, and  $J_P$  and  $J_A$  are, respectively, perimeter and area leakages. To confirm perimeter leakage is not significant, Fig. 9 shows leakage current density at 1 V versus different perimeter/area ratios for the LTA and RTA diodes. For clarity, data are presented in semi-log scale. A straight line can be well fitted to the data in linear scale with the slope of the line corresponding to the perimeter leakage current, according to (2). It can be confirmed that both RTA and LTA diodes exhibit very low perimeter leakage which is at least two orders of magnitude smaller than the area leakage current. The graph also gives good overview of the current density for all types of samples showing improvement in leakage current from  $E_{TH}$  to  $E_{TH} + 0.65 \text{ J/cm}^2$  to the RTA diode.

There are different mechanisms responsible in leakage current which are temperature and electric field dependent, and can be classified as Shockley-Read-Hall (SRH) generation/recombination, trap-assisted tunneling (TAT),

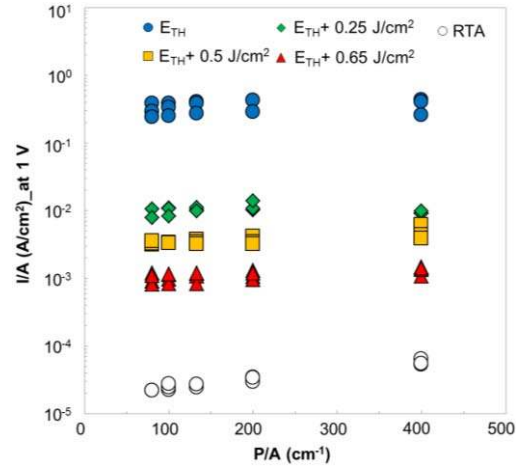


Fig. 9. Representative perimeter leakage current density at reverse voltage of 1 V for different perimeter area ratios for LTA and RTA diodes.

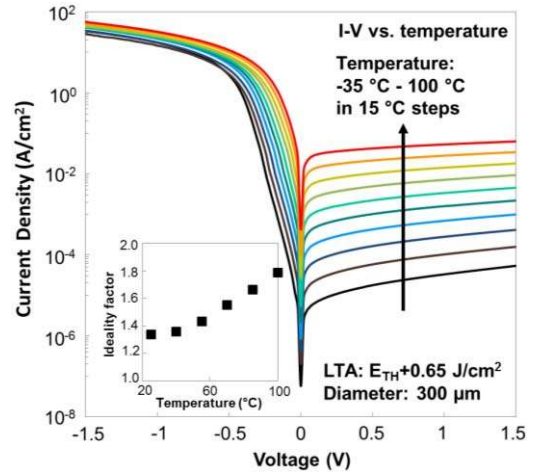


Fig. 10.  $I$ - $V$  characteristic of  $E_{TH} + 0.65 \text{ J/cm}^2$  LTA diode for temperature increments from  $-35 \text{ }^\circ\text{C}$  to  $100 \text{ }^\circ\text{C}$  in  $15 \text{ }^\circ\text{C}$  steps.

band-to-band tunneling (BBT) and diffusion current [22]. To determine the dominant mechanism,  $I$ - $V$  measurements were carried out at temperatures ranging from  $-35 \text{ }^\circ\text{C}$  to  $100 \text{ }^\circ\text{C}$  in  $15 \text{ }^\circ\text{C}$  steps. An activation energy ( $E_A$ ) was then derived from Arrhenius plots. Generally, SRH dominated leakage current is more pronounced in the presence of deep-level defects in the junction with  $E_A$  approximately half of the bandgap. TAT occurs when defects operate as trap levels in the depletion region, causing electrons to be captured and tunnel due to the electric field.  $E_A$  around half of the bandgap is also expected for TAT. If a high electric field exists in the junction, then the most probable mechanism to happen is BBT, as electrons are actuated from valence band in the p-side to the conduction band in the n-side through the depletion region.  $E_A$  is approximately 0 eV in this case. For diffusion current, which is proportional to the square of intrinsic carrier concentration, ( $n_i^2$ ),  $E_A$  is close to the bandgap [23].

In Fig. 10,  $I$ - $V$  characteristics from  $300 \text{ } \mu\text{m}$   $E_{TH} + 0.65 \text{ J/cm}^2$  LTA diode structures at different temperatures

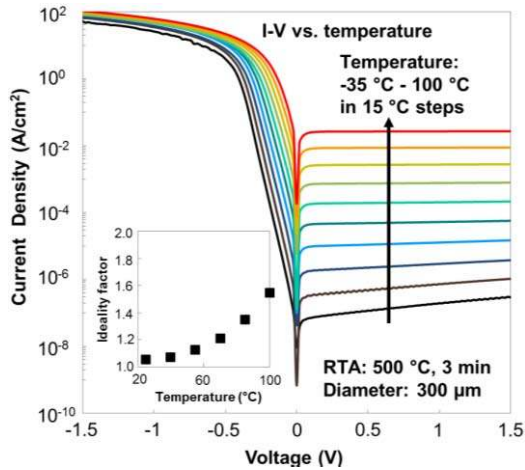


Fig. 11.  $I$ - $V$  characteristic from RTA sample for temperature increments from  $-35$  °C to  $100$  °C in  $15$  °C steps.

are shown. The effect of temperature on diode behavior was reflected in the ideality factor extracted at each temperature. The inset of Fig. 10 shows variation of  $n$  versus temperature with  $n$  increasing by temperature. In these measurements, leakage current increased about three orders of magnitude at  $1$  V, suggesting that diode behavior is strongly affected by temperature variations. Meanwhile, at low temperatures [from  $-35$  °C to room temperature (RT)] leakage current is more dependent on the electric field.

Activation energy for this sample at  $1$  V was found to be  $0.47$  eV, which is bigger than half of the Ge bandgap. According to theory, SRH-dominated leakage current is proportional to depletion width which itself is proportional to  $V^{0.5}$  [22]. Measurements on the LTA diode revealed that the leakage current is proportional to  $V^x$  with  $x > 0.5$  for temperatures from  $-35$  °C to  $55$  °C and  $x < 0.5$  for temperatures from  $55$  °C to  $100$  °C. These results along with extracted  $E_A$  values, which will be shown later, point out that the leakage mechanisms are dominated by TAT and SRH, respectively.

Fig. 11 shows representative  $I$ - $V$  characteristics obtained from a  $300$   $\mu\text{m}$  RTA diode. Again, temperature measurements were carried out from  $-35$  °C to  $100$  °C with  $15$  °C increments. Similar to the LTA diode, ideality factor was increased by temperature as shown in the inset of Fig. 11. Leakage current was enhanced about five orders of magnitude at  $1$  V owing to the temperature change. For this particular sample, the current can be categorized in two different regimes in terms of the leakage current behavior. From  $-35$  °C up to  $10$  °C, the leakage current showed electric field dependence whereas it showed weak dependence on the electric field from  $25$  °C to  $100$  °C. This difference was also reproduced in the activation energy extraction. Note that we performed this analysis on all the diode structures and samples, and this figure shows a representative data sample set.

Fig. 12 shows reverse current density versus  $1/kT$  from a  $300$   $\mu\text{m}$   $E_{\text{TH}} + 0.65$   $\text{J}/\text{cm}^2$  LTA diode for RT to  $100$  °C. Extracted activation energies from the Arrhenius plots for  $0.5$ – $2$  V are  $\sim 0.5$ – $0.4$  eV, respectively. The inset shows similar graph for  $1$  V for the RTA sample where the diode behavior splits in to two regimes. Different activation

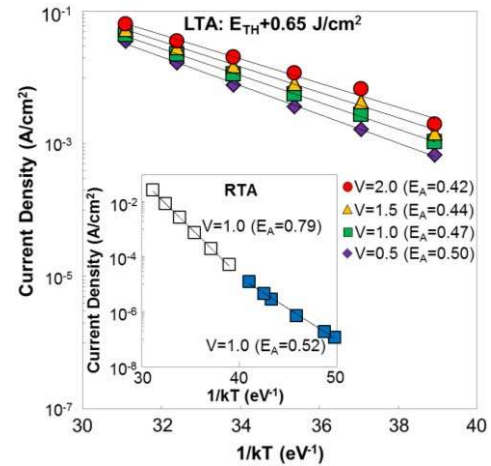


Fig. 12. Reverse current density versus  $1/kT$  from  $E_{\text{TH}} + 0.65$   $\text{J}/\text{cm}^2$  LTA sample for RT and above. Activation energy is extracted from the slope of the fitted lines. Inset: current density versus  $1/kT$  for the RTA sample for which different behavior is observed below and above RT.

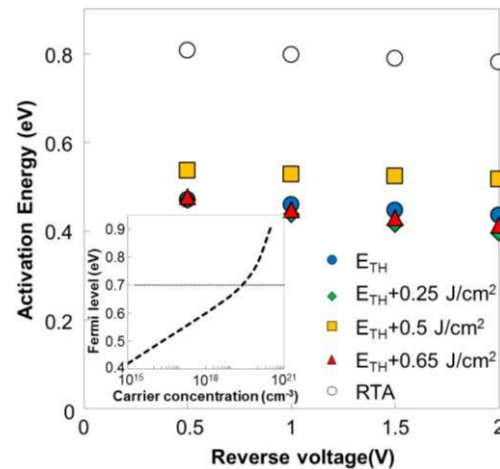


Fig. 13. Activation energy versus reverse bias extracted from RTA and LTA diodes. Inset: calculated Fermi level versus carrier concentration in the n-type region, using a 30-band k.p model.

energies at high and low temperatures were also observed by Eneman *et al.* [24].

Below RT, the  $E_A$  was  $0.52$  eV suggesting TAT as the main contributor to the leakage current. Interestingly, for the temperatures above RT the extracted  $E_A$  was  $0.79$  eV. Considering voltage independency of the  $I$ - $V$  characteristics, it could be interpreted that diffusion is dominating the leakage mechanism in this regime with few generation centers in the depletion layer.

Activation energy versus voltage for RTA and LTA samples at RT and above is shown in Fig. 13. For all LTA samples, activation energy is between  $0.4$  and  $0.6$  eV. Note that  $E_A = 0.79$  eV (RTA case) is very close to direct bandgap ( $0.8$  eV) of Ge. This appears to be a surprising result as the indirect bandgap of Ge is  $0.67$  eV. The reason for  $E_A > 0.67$  eV is not well understood and is currently under investigation. It should be noted that multiple samples and multiple diode structures produced this result. Furthermore, we tested our samples on two entirely different probe stations producing the same results. Moreover, we repeated the entire experiment and RTA processed diodes still produced  $E_A > 0.67$  eV.

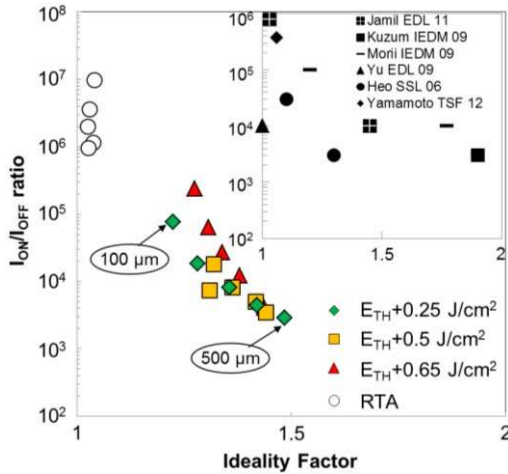


Fig. 14.  $I_{ON}/I_{OFF}$  ratio versus ideality factor for LTA and RTA samples. Inset:  $I_{ON}/I_{OFF}$  ratio for other works published.

The activation energies for the RTA samples are over 90 meV in excess of what is expected for a perfectly crystalline sample doped at  $2.7 \times 10^{19} \text{ cm}^{-3}$ . The inset in Fig. 13 shows the Fermi level versus carrier concentration for Ge, calculated using a 30-band  $\mathbf{k}\cdot\mathbf{p}$  model [25]. At the reported doping concentration, the Fermi level and hence the activation energy should lie around 0.7 eV. Possible reasons for higher activation energies are: 1) a higher carrier concentration of  $\sim 10^{20} \text{ cm}^{-3}$ , introduced in the process of making the diodes and 2) a hybridization of the conduction band with the impurity level at high doping concentration, which may shift the bottom of the conduction band higher in energy. Both these effects would result in an  $E_A$  strongly sensitive to doping concentration. However, we saw in our ECV data shown in Fig. 5 for RTA processed P implants that the active concentration was approximately  $2.7 \times 10^{19} \text{ cm}^{-3}$  which seems to be inconsistent with the aforementioned first explanation. We are currently investigating this trend in the experimental data further through advanced theory and modeling.

Fig. 14 shows the  $I_{ON}/I_{OFF}$  ratio versus  $n$  extracted from 100–500  $\mu\text{m}$  LTA and RTA diodes. Colored symbols show the results from LTA diodes, and open symbols show the RTA case. The best  $I_{ON}/I_{OFF}$  ratio from LTA samples was obtained from the 100  $\mu\text{m}$   $E_{TH} + 0.65 \text{ J/cm}^2$  LTA diode with  $n = 1.3$  and  $I_{ON}/I_{OFF}$  ratio =  $2.4 \times 10^5$ , which matches the best reported to date for Ge diodes with LTA [8]. RTA diodes exhibit  $n$  less than 1.05, with corresponding  $I_{ON}/I_{OFF}$  ratio  $\sim 10^7$ , which to the best of our knowledge is the highest obtained for Ge diodes to date.  $n \sim 1$  indicates that there are few defects in the junction, and the total leakage current is mainly dominated by diffusion current.

To benchmark our results, the inset shows similar works on Ge that have been reported so far [11]–[14], [26], [27]. Jamil *et al.* [11] used spin-on-dopant technique and reported  $n \sim 1.03$  and  $I_{ON}/I_{OFF}$  ratio  $\sim 10^5$ – $10^6$  compared with conventional ion implantation with  $n = 1.45$  and  $I_{ON}/I_{OFF}$  ratio  $\sim 10^3$ – $10^4$ . Kuzum *et al.* [12] achieved  $n \sim 1.9$  and  $I_{ON}/I_{OFF}$  ratio  $\sim 10^3$  from nMOS devices with  $\text{GeO}_x\text{N}_y$  dielectrics. Morii *et al.* [13] reported  $n \sim 1.2$  and  $I_{ON}/I_{OFF}$  ratio  $\sim 10^5$  from junctions created by gas phase doping

and  $n \sim 1.77$  and  $I_{ON}/I_{OFF}$  ratio  $\sim 10^4$  from P-implanted n+/p junctions. Yu *et al.* [26] compared *in situ* doping with ion implantation and reported  $n \sim 1$  and  $I_{ON}/I_{OFF}$  ratio  $\sim 10^3$  for *in situ* doping and ion implantation, respectively. Yamamoto *et al.* [27] fabricated n+/p diodes with  $n \sim 1.06$  and  $I_{ON}/I_{OFF}$  ratio  $\sim 3.7 \times 10^5$ . Koike *et al.* [28] reported  $I_{ON}/I_{OFF}$  ratio  $\sim 10^6$  by two-step P implantation followed by RTA. Heo *et al.* [14] applied plasma doping followed by excimer laser annealing on Ge and obtained  $n \sim 1.1$ – $1.3$  and  $I_{ON}/I_{OFF}$  ratio  $\sim 10^3$ – $10^4$ . Their ideality factor is better than the value reported in this paper but the obtained  $I_{ON}/I_{OFF}$  ratio seems to be lower compared with our data. In our paper, we used ion implant whereas plasma doping was used by Heo *et al.* [14]. This may lead to differences in damage and defect distributions close to the junction, leading to different diode performance. Plasma implant is known to reduce EOR defects and keep the implanted region very shallow ( $\sim 10 \text{ nm}$  in [14]). In that case, the melting time is probably shorter, thus the dopants out-diffusion is limited. In addition, high concentration of P on the surface could act as a capping layer limiting the oxygen incorporation from the native oxide which may result in less defects.

There is certainly a tradeoff between high levels of carrier concentration and the electrical performance of the n+/p junctions. LTA provides high carrier concentration, which is good for access resistance with tradeoff in  $I_{ON}/I_{OFF}$ . The opposite is true for RTA technique. From our data, it is evident that optimum LTA condition can be found to achieve high carrier concentration with acceptable  $I_{ON}/I_{OFF}$  ratios.

#### IV. CONCLUSION

In this paper, material and electrical characteristics of n+/p junctions in Ge formed by RTA and LTA process techniques were compared. High carrier concentration ( $> 10^{20} \text{ cm}^{-3}$ ) was accomplished using LTA for activating the dopants and also removal of the crystal damage induced by ion implantation. Retained dose drops with increasing thermal budget; however, ECV and Hall effect data indicate almost 100% activation of the dose that was retained. Furthermore, high quality n+/p junction diodes were demonstrated with  $I_{ON}/I_{OFF}$  ratio  $\sim 10^7$  and  $I_{ON}/I_{OFF}$  ratio  $\sim 10^5$  for RTA and LTA samples, respectively. To fulfill requirements for highly activated dopants and high  $I_{ON}/I_{OFF}$  ratios, more optimization needs to be done to fine tune the LTA process. Also, more analysis is required to pinpoint the nature of the mechanism involved in extraction of activation energy greater than 0.67 eV in RTA Ge diodes.

#### ACKNOWLEDGMENT

The authors would like to thank M. T. Hungria from the Centre de Microcaractérisation Raimond Castaing, Toulouse, for performing the SIMS measurements. F. Cristiano and S. Boninelli would also like to thank A. La Magna from CNR-IMM Catania for inspiring discussions.

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