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McGrath, Teixeira, C., & Holmes, G. (2017). Optimized phase disposition (PD) modulation of a modular multilevel converter. IEEE Transactions on Industry Applications, 53(5), 4624–4633.
https://doi.org/10.1109/TIA.2017.2697953
Document Version: Accepted Manuscript

Published Version: https://doi.org/10.1109/TIA.2017.2697953

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Citation:

McGrath, B, Teixeira, C and Holmes, G 2017, 'Optimized phase disposition (PD) modulation of a modular multilevel converter', IEEE Transactions on Industry Applications, vol. 53, no. 5, pp. 4624-4633.

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Optimised Phase Disposition (PD) Modulation of a Modular Multilevel Converter

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***Abstract* — This paper presents a theoretical harmonic analysis of phase disposition (PD) and phase shifted carrier (PSC) pulse width modulation (PWM) strategies for MMC converters. It is shown that when these strategies are implemented on a per MMC arm basis, their spectral performances converge because of cancellation of odd carrier sideband groups between each phase leg's arms. An improved PD modulation strategy is then presented that uses a single PD modulator for the entire phase leg, followed by a state machine decoder that evenly distributes switching pulses to all sub-modules across the phase leg upper and lower arms to balance the distribution of sub-module commutation events. The resulting strategy achieves optimum phase leg PD spectral performance, and also achieves natural voltage balancing of the MMC sub-modules. All theoretical findings are supported by simulation and experimental results obtained using a five level MMC prototype.**

***Index Terms* – Modular multilevel converter, MMC, double Fourier, pulse width modulation, spectral analysis.**

I. INTRODUCTION

The modular multilevel converter (MMC) is now well established as the topology of choice for high power energy conversion applications that operate at medium/high voltage levels [1]-[17]. MMCs offer several advantages, including scalability to high operating voltages using the series connection of *2N* commutation sub-modules (*N* per arm), ability to operate from a single overall DC link without requiring source bulk storage capacitors, and a capability to synthesise switched waveforms with low levels of harmonic distortion [2]-[4]. However MMC modulation has proved to be quite complex, essentially for two reasons. Firstly, since the MMC topology can synthesise its output voltage using multiple redundant switched states, these states need to be appropriately selected to maintain balance of the individual sub-module DC link voltages [4][5] and to evenly distribute device switching losses between all sub-modules over each fundamental cycle [4]. Secondly, the nature of the MMC topology causes circulating currents to flow between the upper and lower MMC arms for each phase leg, and these currents should be minimised as much as possible to reduce device conduction and commutation losses [4][5]. Much of the recent research into the MMC control has been to explore how best to manage these requirements.

While a large number of pulse width modulation (PWM) alternatives have been proposed for MMC's over the last decade [4], they are generally variations of the established Phase Shifted Carrier (PSCPWM)[18] and level-shifted phase disposition (PD)[19][20] strategies, derived from previously reported usage with other multilevel converters. PSCPWM modulates the N individual sub-modules of each MMC arm independently, by comparing a fundamental reference waveform against an individual (triangular) carrier waveform that fully occupies the linear modulation range. The sub-module carriers within each arm are phase shifted relative to each other by $2\pi/N$, to achieve harmonic cancellation up to the N^{th} carrier sideband group. Further harmonic reduction is possible by "interleaving", whereby the lower arm carrier groups are phase shifted relative to the upper arm group by either $0°$ for odd N, or π/N for even N, resulting in $2N+1$ output voltage levels and cancellation up to the $2N^{th}$ sideband carrier group [6][7]. This approach equally distributes switching events across all sub-modules automatically, is readily modified to achieve active sub-module voltage balancing via localised duty cycle augmentation or sort and select algorithms [4], and has also been recently identified as providing a natural sub-module voltage balancing response [8].

PD modulation on the other hand compares a fundamental reference against N smaller magnitude carriers arranged continuously across the linear modulation range. PD PWM is well known from other multilevel inverter applications to reduce harmonic output distortion compared to PSCPWM because it puts significant energy into the first carrier harmonic, which is co-phasal between the phase legs of a three phase system and therefore does not contribute to the converter line-to-line output voltage harmonic distortion [20]. As with PSCPWM, PD PWM is generally implemented separately for each MMC arm [4], and can synthesise $N+1$ switched output voltage levels when synchronized arm pulse patterns are used, or $2N+1$ switched output voltage levels with reduced distortion levels when the arm pulse patterns are interleaved [10][16][17]. Note that interleaving can be achieved either explicitly by imposing a carrier phase shift [10], or via a virtual state mapping technique [16][17]. However, the results reported

in [10] only achieve marginal harmonic gains for PD versus PSCPWM implemented using this approach, which is inconsistent with the previously reported substantial harmonic gains of PD for other multilevel inverters [20].

This paper presents a detailed investigation of the phase leg output harmonics for a MMC switched by PD and PSCPWM under interleaved conditions [21]. It shows how implementing PD on a per arm basis negates the primary benefit of this modulation strategy, since it cancels the first carrier sideband group harmonics (which contains the PD "signature" common mode carrier harmonic) between the two arms and leaves only the second carrier sideband harmonics (which are identical to PSCPWM) in the switched output waveform. The paper then shows how PD PWM can be optimally implemented on a MMC by scheduling the switching events of both arms as an integrated process, to achieve both $2N+1$ switched voltage levels and a substantial phase leg first carrier co-phasal harmonic component between the three phase outputs. As with all PD implementations for multilevel inverters with redundant switched states, the converter transitions created by the modulation process are then decoded into specific sub-module switching events using post modulation processing, to balance sub-module switching transitions. Simulation and experimental results obtained using a prototype five level MMC are presented to validate the theoretical principles developed in this paper.

II. MMC CIRCUIT ANALYSIS.

Fig. 1 shows the topology of a three phase MMC, where each phase leg consists of an upper and lower arm, each formed by the series connection of N identical sub-modules, that are linked to the phase leg output through a pair of inductors. Each sub-module has a complementary switch pair and a floating capacitor, which under balanced conditions is charged to V_{DC}/N. For generality, the arm inductors can be considered as coupled (i.e. a common core) with winding leakage and mutual inductances L_k and L_b respectively, and a series resistance R_b per winding. Time

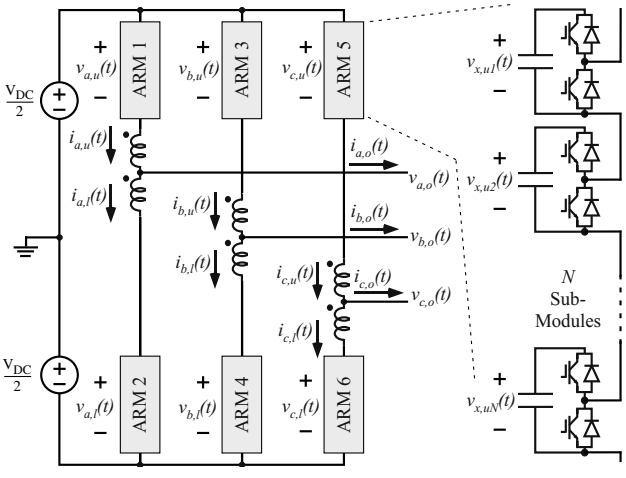


Fig. 1. Circuit topology of a three phase MMC.

derivative circuit relationships between the arm currents for each phase leg can be derived using Kirchoff's voltage law (KVL) around the upper and lower arm loops as:

$$\frac{V_{DC}}{2} - v_{x,u}(t) - v_{x,o}(t) = R_b i_{x,u}(t) + [L_k + L_b]\frac{di_{x,u}(t)}{dt} + L_b\frac{di_{x,l}(t)}{dt} \quad (1)$$

$$\frac{V_{DC}}{2} - v_{x,l}(t) + v_{x,o}(t) = R_b i_{x,l}(t) + [L_k + L_b]\frac{di_{x,l}(t)}{dt} + L_b\frac{di_{x,u}(t)}{dt} \quad (2)$$

where $x \in \{a,b,c\}$. For each phase leg, differential and common mode arm voltages and phase currents can now be defined according to:

$$v_{x,dm}(t) = [v_{x,u}(t) - v_{x,l}(t)]/2 \quad (3)$$

$$v_{x,cm}(t) = [v_{x,u}(t) + v_{x,l}(t)]/2 \quad (4)$$

$$i_{x,dm}(t) = [i_{x,u}(t) - i_{x,l}(t)]/2 = i_{x,o}(t)/2 \quad (5)$$

$$i_{x,cm}(t) = [i_{x,u}(t) + i_{x,l}(t)]/2 = i_{x,circ}(t) \quad (6)$$

Note that (5) and (6) identify how the MMC phase leg output currents, $i_{x,o}(t)$, and circulating currents, $i_{x,circ}(t)$, are purely differential and common mode only, respectively. Time derivative equations for $i_{x,dm}(t)$ and $i_{x,cm}(t)$ can now be created by first subtracting and then adding (1) and (2), and then substituting the appropriate common and differential mode expressions from (3) to (6), to produce:

$$-v_{x,dm}(t) - v_{x,o}(t) = R_b i_{x,dm}(t) + L_k\frac{di_{x,dm}(t)}{dt} \quad (7)$$

$$\frac{V_{DC}}{2} - v_{x,cm}(t) = R_b i_{x,cm}(t) + [L_k + 2L_b]\frac{di_{x,cm}(t)}{dt} \quad (8)$$

For the usual condition that R_b and L_k are negligible, (7) and (8) can be reduced to:

$$v_{x,o}(t) \approx -v_{x,dm}(t) \quad (9)$$

$$v_{x,cm}(t) \approx \frac{V_{DC}}{2} - 2L_b\frac{di_{x,cm}(t)}{dt} \quad (10)$$

Eqn. (9) shows that the phase leg output voltages are determined by the differential mode arm voltages only, while (10) shows that the common mode (circulating) currents are determined only by the common mode arm voltages. Hence the best way to assess a MMC PWM strategy in terms of output harmonic performance (and circulating currents if desired) is clearly to identify the harmonics generated by the strategy for each phase leg as differential or common mode voltage components.

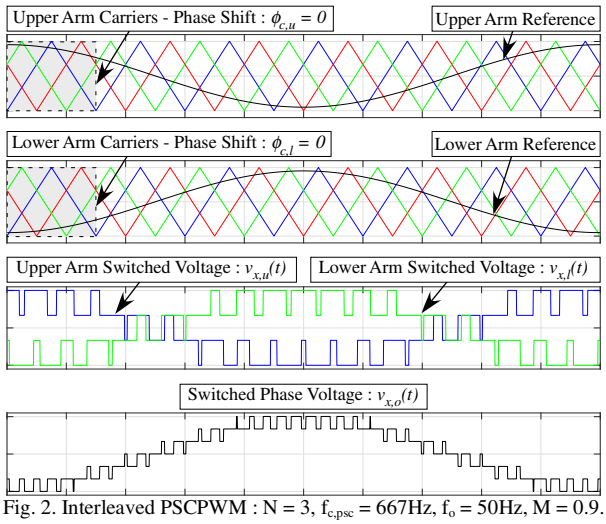


Fig. 2. Interleaved PSCPWM : N = 3, $f_{c,psc}$ = 667Hz, f_o = 50Hz, M = 0.9.

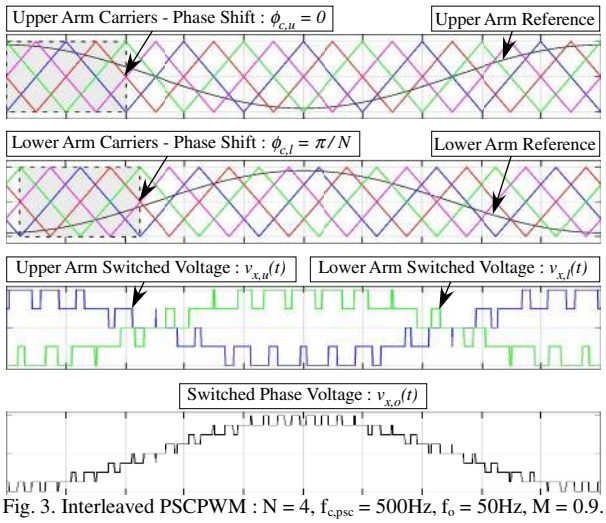


Fig. 3. Interleaved PSCPWM : N = 4, $f_{c,psc}$ = 500Hz, f_o = 50Hz, M = 0.9.

III. Harmonic Analysis of PSCPWM and PD PWM

Double Fourier series analysis will now be used to identify the differential mode MMC harmonics, and hence the phase voltage, produced by PSCPWM and PD PWM.

A. PSCPWM.

Figs. 2 and 3 show the reference and carrier waveforms associated with the PSCPWM strategy for two exemplar MMC converters with an odd $(N=3)$ and even $(N=4)$ number of cells per arm. Note how the low frequency fundamental PWM reference waveforms for the upper and lower arms are phase shifted by π to achieve the required differential mode fundamental output in accordance with (9). Each carrier has its frequency $f_{c,psc}$, set to the desired sub-module switching frequency, and the carrier groups within each MMC arm are phase shifted by $2\pi/N$. This produces a switched MMC arm voltage with an apparent switching frequency $Nf_{c,psc}$, as is clearly evident in Figs. 2 and 3 with $Nf_{c,psc} = 2\text{kHz}$. Interleaved operation, with the associated $2N+1$ switched phase leg voltage levels (i.e. 7 levels in Fig. 2, and 9 levels in Fig. 3) results when the upper and lower MMC arm carrier groups are phase shifted with respect to one another using [6][7]:

$$\phi_{c,u} = 0, \qquad \phi_{c,l} = 0, \qquad N \textbf{ odd} \tag{11}$$

$$\phi_{c,u} = 0, \qquad \phi_{c,l} = \pi/N, \qquad N \textbf{ even} \tag{12}$$

The harmonic solution for PSCPWM is readily found by summing the Double Fourier series for (naturally sampled) PWM for each arm's sub-modules, using the same approach as for a cascaded H-bridge inverter [18]. This approach yields (13), shown at the bottom of the page, for $x \in \{a,b,c\}$ and $y \in \{u,l\}$, and where $J_n(\gamma)$ denotes a Bessel function of the first kind with order n and parameter γ, M is the modulation depth, ω_o and $\omega_{c,psc}$ are the reference and carrier angular frequencies, and $\theta_{x,y}$ are the phase leg fundamental reference angles defined as:

$$\theta_{x,u} \in \{0, -2\pi/3, 2\pi/3\} \quad \text{and} \quad \theta_{x,l} = \theta_{x,u} + \pi \tag{14}$$

The differential mode voltage harmonics are found by substituting (13) into (3) with the required carrier phase shift conditions from (11) and (12). For PSCPWM these harmonics have the same form irrespective of whether N is odd or even, and are given by (15), shown at the bottom of the page. This result identifies that the first sideband group in the MMC phase voltage is centered around the frequency $2Nf_{c,psc}$, indicating an apparent switching frequency doubling in the formation of the phase voltage. This is to be expected given the asynchronous switching pulses in the upper and lower arm voltages, as shown in Figs. 2 and 3.

B. PD PWM.

Figs. 4 and 5 show the reference and carrier waveforms for the PD PWM strategy for the two MMC converters with $N=3$ and $N=4$, with modulation conditions set so as to achieve the same number of overall commutation events in the output voltage when compared to the PSCPWM strategy shown in Figs. 2 and 3. This requires that the PD carrier frequency is set to $Nf_{c,psc}$. Interleaved PD PWM, again with the associated $2N+1$ switched phase leg voltage levels, requires that the upper and lower arm voltage pulses are asynchronous [10], which means carrier phase shifts of:

$$v_{x,y}(t) = \frac{V_{DC}}{2} + \frac{MV_{DC}}{2}\cos\left(\omega_o t + \theta_{x,y}\right) + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{2V_{DC}}{mN\pi}\sin\left(\left(Nm+n\right)\frac{\pi}{2}\right)J_n\left(Nm\frac{\pi}{2}M\right)\cos\left(mN\left[\omega_{c,psc}t+\phi_{c,y}\right]+n\left[\omega_o t+\theta_{x,y}\right]\right) \tag{13}$$

$$v_{x,dm}(t) = \frac{MV_{DC}}{2}\cos\left(\omega_o t + \theta_{x,y}\right) + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{V_{DC}}{mN\pi}\cos\left(\left[mN+n+1\right]\pi\right)J_{2n-1}\left(mN\pi M\right)\cos\left(2mN\omega_{c,psc}t+\left(2n-1\right)\left[\omega_o t+\theta_{x,y}\right]\right) \tag{15}$$

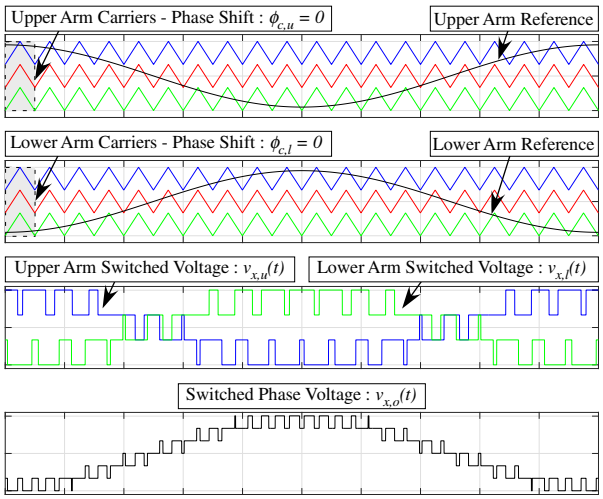


Fig. 4. Interleaved PD PWM : N = 3, $f_{c,pd}$ = 2kHz, f_o = 50Hz, M = 0.9.

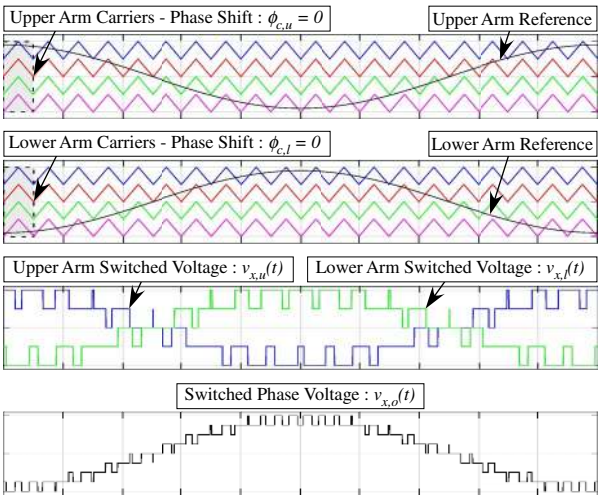


Fig. 5. Interleaved PD PWM : N = 4, $f_{c,pd}$ = 2kHz, f_o = 50Hz, M = 0.9.

$$\phi_{c,u} = 0, \qquad \phi_{c,l} = 0 \tag{16}$$

The PD harmonic solution is more complex compared to PSCPWM, since each arm's sub-module sine-triangle comparison process is discontinuous. However considering balanced MMC sub-module voltages (i.e. $v_{x,yj} = V_{DC}/N$, for $x \in \{a,b,c\}$, $y \in \{u,l\}$, and $j \in \{1,\ldots,N\}$), the approach presented in [20] can be applied, which yields:

$$\begin{aligned} v_{x,y}(t) &= \frac{V_{DC}}{2} + \frac{MV_{DC}}{2}\cos\left(\omega_o t + \theta_{x,y}\right) \\ &+ \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} \frac{C_{m_{even}n_{odd}}}{m}\cos\begin{pmatrix} 2m\left[\omega_{c,pd}t + \phi_{c,y}\right] \\ +\left(2n-1\right)\left[\omega_o t + \theta_{x,y}\right] \end{pmatrix} \\ &+ \sum_{m=0}^{\infty}\sum_{n=-\infty}^{\infty} \frac{C_{m_{odd}n_{even}}}{2m+1}\cos\begin{pmatrix} \left(2m+1\right)\left[\omega_{c,pd}t + \phi_{c,y}\right] \\ +2n\left[\omega_o t + \theta_{x,y}\right] \end{pmatrix} \end{aligned} \tag{17}$$

where $\omega_{c,pd} = N\omega_{c,psc}$ is the PD carrier angular frequency. Note that the double summation term for the odd harmonic group $m_{odd}n_{even}$ in (17) creates the characteristic PD carrier harmonic when $m = 0$ and $n = 0$.

For PD PWM the $C_{m_{even}n_{odd}}$ coefficients have the same essential form, irrespective of whether N is odd or even, with only a minor sign change. Hence for **even** N:

$$C_{m_{even}n_{odd}} = \frac{V_{DC}}{N\pi} J_{2n-1}\left(Nm\pi M\right)\cos\left(\left(n-1\right)\pi\right) \tag{18}$$

and for **odd** N:

$$C_{m_{even}n_{odd}} = \frac{V_{DC}}{N\pi} J_{2n-1}\left(Nm\pi M\right)\cos\left(\left(m+n-1\right)\pi\right) \tag{19}$$

In contrast the $C_{m_{odd}n_{even}}$ coefficients are much more complex as shown in (20) and (21) below [20], where:

$$\alpha_h = \cos^{-1}\left(2h/NM\right) \tag{22}$$

$$\beta_h = \cos^{-1}\left(\left(2h-1\right)/NM\right) \tag{23}$$

$$C_{m_{odd}n_{even}} = \frac{4V_{DC}}{N\pi^2}\sum_{k=0}^{\infty}\cos\left(k\pi\right)J_{2k+1}\left(\xi_m\right)\left[\begin{aligned} &\frac{1}{2n-2k-1}\left\{\sin\left(\left(2n-2k-1\right)\frac{\pi}{2}\right) + \sum_{h=1}^{N/2-1} 2\sin\left(\left(2n-2k-1\right)\alpha_h\right)\cos\left(h\pi\right)\right\} \\ &+\frac{1}{2n+2k+1}\left\{\sin\left(\left(2n+2k+1\right)\frac{\pi}{2}\right) + \sum_{h=1}^{N/2-1} 2\sin\left(\left(2n+2k+1\right)\alpha_h\right)\cos\left(h\pi\right)\right\} \end{aligned}\right], \; N \textbf{ even} \tag{20}$$

$$\begin{aligned} C_{m_{odd}n_{even}} &= \frac{4V_{DC}}{N\pi^2}\cos\left(m\pi\right)\times \\ &\left[\begin{aligned} &\sum_{k=1,k\neq|n|}^{\infty}\left\{\cos\left(k\pi\right)J_{2k}\left(\xi_m\right)\sum_{h=1}^{(N-1)/2}\cos\left(h\pi\right)\left(\frac{\sin\left(2\left(n-k\right)\beta_h\right)}{n-k} + \frac{\sin\left(2\left(n+k\right)\beta_h\right)}{n+k}\right)\right\} \\ &+\cos\left(n\pi\right)J_{2n}\left(\xi_m\right)\left[\frac{\pi}{2} + \sum_{h=1}^{(N-1)/2}\cos\left(h\pi\right)\left(2\beta_h + \left.\frac{\sin\left(4n\beta_h\right)}{2n}\right|_{n\neq 0}\right)\right] + \frac{J_0\left(\xi_m\right)}{n}\left.\sum_{h=1}^{(N-1)/2}\sin\left(2n\beta_h\right)\cos\left(h\pi\right)\right|_{n\neq 0} \end{aligned}\right], \; N \textbf{ odd} \end{aligned} \tag{21}$$

$$v_{x,dm}(t)=\frac{MV_{DC}}{2}\cos\left(\omega_o t+\theta_{x,y}\right)+\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{V_{DC}}{N\pi m}J_{2n-1}(Nm\pi M)\cos((n-1)\pi)\cos\left(2m\omega_{c,pd}t+(2n-1)\left[\omega_o t+\theta_{x,y}\right]\right),\quad N\ \textbf{even} \tag{25}$$

$$v_{x,dm}(t)=\frac{MV_{DC}}{2}\cos\left(\omega_o t+\theta_{x,y}\right)+\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{V_{DC}}{N\pi m}J_{2n-1}(Nm\pi M)\cos((m+n-1)\pi)\cos\left(2m\omega_{c,pd}t+(2n-1)\left[\omega_o t+\theta_{x,y}\right]\right),\ N\ \textbf{odd} \tag{26}$$

$$\xi_m=(2m+1)NM\ \pi/2 \tag{24}$$

As with PSCPWM, the differential mode harmonics are found by substituting (17) and (20) into (3) with the carrier phase shift conditions in (16), which after some manipulation yields (25) and (26). A comparison of (25) and (26) with (13) and (15) shows that the differential mode harmonics of interleaved PSCPWM and PD PWM have identical magnitude functions, and hence the output spectral performance of both strategies must be the same.

This analysis is confirmed in Figs. 6,7,9 and 10, which compare the arm, phase and line-to-line voltage spectra of the interleaved PD and PSCPWM strategies for the $N=3$ and $N=4$ MMCs, for the PWM conditions shown in Figs. 2 to 5. Note that all spectra presented in this paper use a logarithmic scale showing three decades (i.e. 10^0 to 10^{-3}) for the magnitude axis. Comparison of Fig. 6 to 7 and Fig. 9 to 10, shows the key difference between the PSCPWM and PD strategies, which is that for PD the odd carrier sideband groups within the arm voltages are dominated by a large carrier harmonic while the associated sidebands are suppressed. This is the well reported mechanism by which PD achieves superior performance to other multilevel PWM strategies [19][20]. However since the odd sideband groups are common mode in an MMC, the phase voltage only consists of the even sideband groups which are clearly identical to the PSCPWM sidebands. Hence the line to line voltages of MMCs controlled by PD and PSCPWM in this way are identical.

IV. Improved MMC PD Implementation with a Post-Modulation Phase Leg State Machine Decoder.

Section III has identified that PD PWM of a MMC cannot be effectively implemented on a per arm basis. Hence an improved way of implementing PD PWM with *N* sub-modules per arm is required that still achieves *2N+1* output switching levels, but also creates a significant (i.e 20% magnitude) output carrier harmonic component. This can be done by modulating each arm pair as an integrated $2N+1$ level phase leg, using a standard PD modulator structure with the substitutions $N\rightarrow 2N$ to account for the increased number of voltage levels, and $\omega_{c,pd}\rightarrow 2\omega_{c,pd}$ to achieve the same total number of commutation events. The consequence of this is that the phase voltage spectrum will be governed by the even N PD harmonic solution, according to (27) below, and with the Fourier coefficients defined in (18) and (20).

Figs. 8 and 11 demonstrate the harmonic gains that can be achieved with this strategy, and show the MMC phase and line to line voltage spectra for equivalent PWM conditions as shown in Figs. 6,7,9 and 10 for the $N=3$ and $N=4$ MMCs. In both cases a large carrier harmonic can be clearly observed in the phase voltage at 4kHz, with a substantially more spread sideband group clustered around this frequency. However, when the carrier harmonic cancels in the formation of the line to line voltage, the remaining sidebands are lower in magnitude compared to the previously reported interleaved PSCPWM and PD strategies. The consequential harmonic benefit is illustrated in Fig. 12, which compares the normalised weighted THD (NWTHD) for each strategy, with NWTHD defined as:

$$NWTHD=\sqrt{\sum_{n=2}^{\infty}\left(V_n/n\right)^2}\ M/V_1 \tag{28}$$

Note that Fig. 12 shows only the even N case for conciseness, but similar results are readily obtained for odd N. Without interleaving, PD is clearly superior to PSCPWM. As discussed in section III, both single arm modulation strategies converge with interleaving. However modulating the MMC as a unified $2N+1$ phase leg enables the harmonic properties of PD PWM to be further exploited, with a significant additional reduction in overall distortion. Note that this gain is realised despite the production of additional low magnitude (~0.1%) sidebands at lower frequencies (~1kHz).

Since PD PWM only defines the target output voltage level, a decoding strategy is then required to select discrete sub-module switched states. Established MMC PWM decoders typically employ a sort and select type algorithm [4][9][11]-[14]. However the approach presented in this paper exploits the recently reported natural balancing mechanism of an MMC [8], and uses a finite state machine decoder, similar to that reported for flying capacitor [22] and coupled inductor semi-bridge converters [23]. For the MMC context it is first necessary to define all possible phase leg switched states to identify state redundancies, and then to determine the instantaneous differential and common mode voltages that result. This is illustrated for a $N=2$ MMC system in Table I.

$$v_{x,o}(t)=\frac{MV_{DC}}{2}\cos\left(\omega_o t+\theta_{x,u}\right)+\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{C_{m_{even}n_{odd}}}{m}\cos\begin{pmatrix}4m\omega_{c,pd}t+\\(2n-1)\left[\omega_o t+\theta_{x,u}\right]\end{pmatrix}+\sum_{m=0}^{\infty}\sum_{n=-\infty}^{\infty}\frac{C_{m_{odd}n_{even}}}{2m+1}\cos\begin{pmatrix}2(2m+1)\omega_{c,pd}t+\\2n\left[\omega_o t+\theta_{x,u}\right]\end{pmatrix} \tag{27}$$

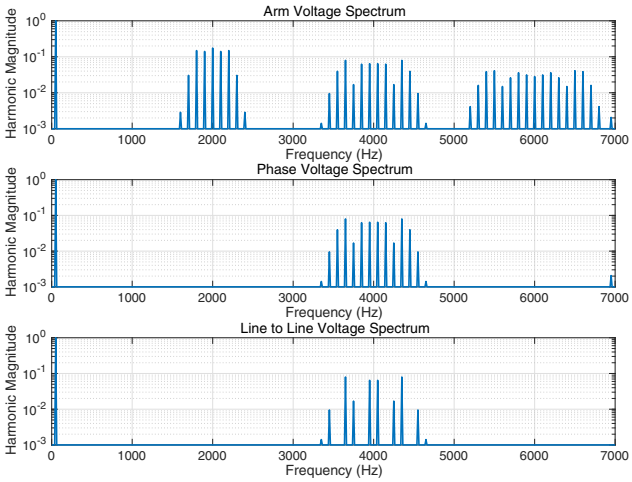


Fig. 6. Interleaved PSCPWM : N = 3, f_c = 667Hz, f_o = 50Hz, M = 0.9.

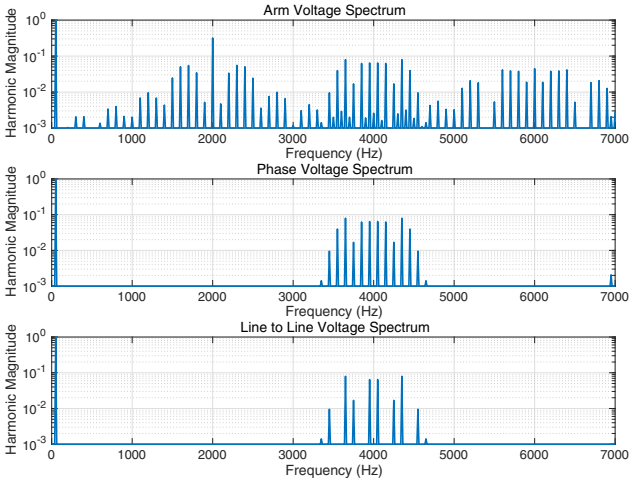


Fig. 7. Interleaved PD PWM : N = 3, f_c = 2kHz, f_o = 50Hz, M = 0.9.

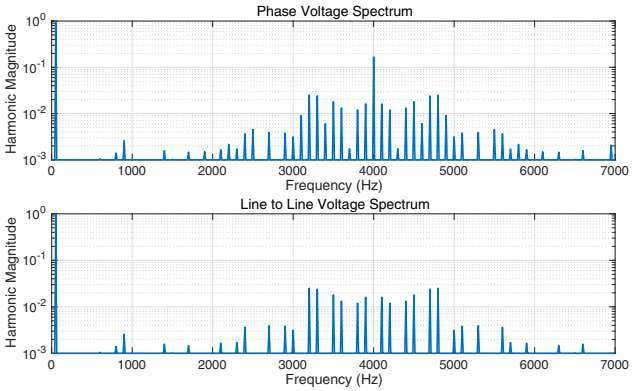


Fig. 8. Phase Leg Based PD: N = 3, f_c = 4kHz, f_o = 50Hz, M = 0.9.

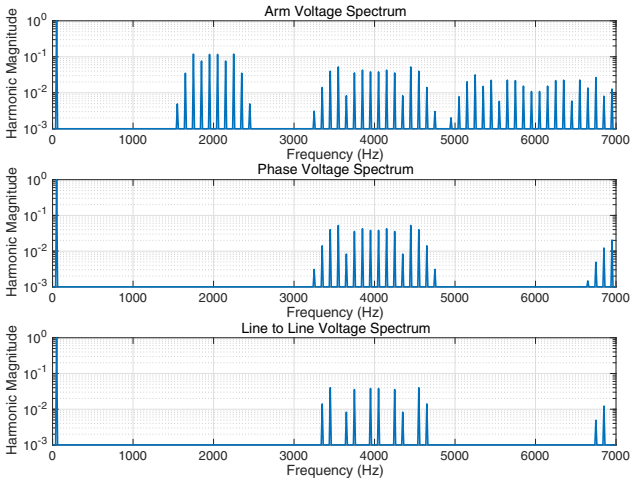


Fig. 9. Interleaved PSCPWM : N = 4, f_c = 500Hz, f_o = 50Hz, M = 0.9.

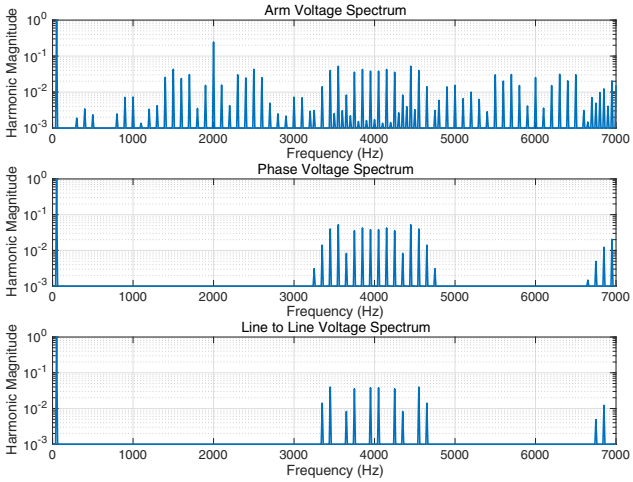


Fig. 10. Interleaved PD PWM : N = 4, f_c = 2kHz, f_o = 50Hz, M = 0.9.

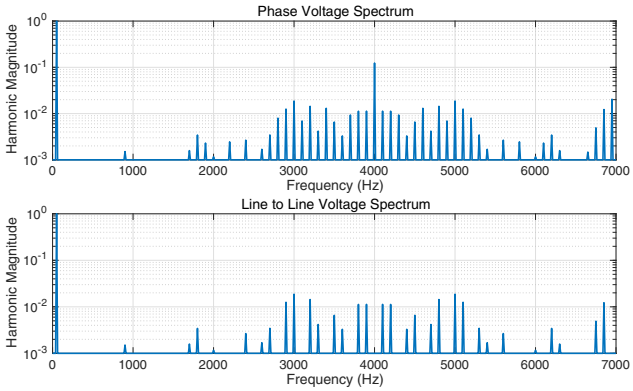


Fig. 11. Phase Leg Based PD : N = 4, f_c = 4kHz, f_o = 50Hz, M = 0.9.

From this data a finite state machine can be constructed, consisting of $2N$ rows corresponding to each PWM disposition band, each with $4N$ logical states to account for the total number of phase leg sub-modules (i.e. $2N$) and the two switching events produced within each carrier interval. Sub-module switched states are then allocated to

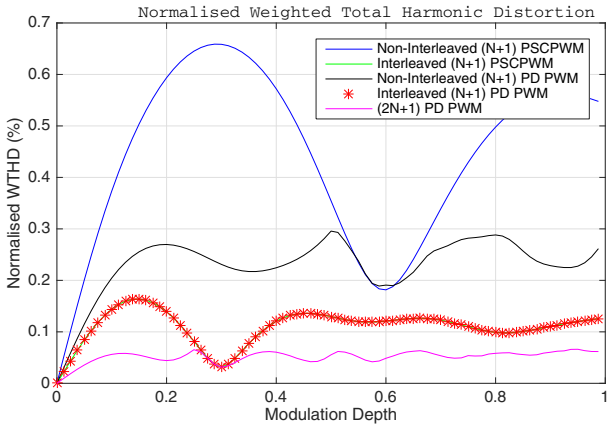


Fig. 12. MMC NWTHD curves : N = 4, (N+1) PSCPWM (f_c = 500Hz), (N+1) PD (f_c = 2kHz), (2N+1) PD f_c = 4kHz, f_o = 50Hz.

their relevant row for a given disposition band, in a sequence that balances the usage of upper and lower arm sub-module devices while simultaneously achieving cycle-by-cycle reversal of the common mode voltage to constrain the circulating current. This state machine is shown in Fig. 13, where the $2N$ rows can be identified with the states S_0 to S_7, S_8 to S_{15}, S_{16} to S_{23} and S_{24} to S_{31}, with the associated phase leg switched state identified as C_0 to C_F from Table I.

State transitions are identified using the target level selection (i.e. L_0 to L_4) defined by the PD modulator. While transitions within the rows are straight forward, care must be taken with transitions that require a row change (i.e. disposition band transitions) since a PD modulator can cause a shortening or lengthening of the switched pulse interval by one half-carrier period at these points. This effect would cause a bias change to the common mode

TABLE I: SWITCHED STATES v_{dm} AND v_{cm} FOR N=2.

C	c_3	c_2	c_1	c_0	v_{upper}	v_{lower}	v_{dm}	v_{cm}
C_C	1	1	0	0	0	V_{DC}	$V_{DC}/2$	$V_{DC}/2$
C_8	1	0	0	0	0	$V_{DC}/2$	$V_{DC}/4$	$V_{DC}/4$
C_4	0	1	0	0	0	$V_{DC}/2$	$V_{DC}/4$	$V_{DC}/4$
C_E	1	1	1	0	$V_{DC}/2$	V_{DC}	$V_{DC}/4$	$3V_{DC}/4$
C_D	1	1	0	1	$V_{DC}/2$	V_{DC}	$V_{DC}/4$	$3V_{DC}/4$
C_0	0	0	0	0	0	0	0	0
C_A	1	0	1	0	$V_{DC}/2$	$V_{DC}/2$	0	$V_{DC}/2$
C_6	0	1	1	0	$V_{DC}/2$	$V_{DC}/2$	0	$V_{DC}/2$
C_9	1	0	0	1	$V_{DC}/2$	$V_{DC}/2$	0	$V_{DC}/2$
C_5	0	1	0	1	$V_{DC}/2$	$V_{DC}/2$	0	$V_{DC}/2$
C_F	1	1	1	1	V_{DC}	V_{DC}	0	V_{DC}
C_2	0	0	1	0	$V_{DC}/2$	0	$-V_{DC}/4$	$V_{DC}/4$
C_1	0	0	0	1	$V_{DC}/2$	0	$-V_{DC}/4$	$V_{DC}/4$
C_B	1	0	1	1	V_{DC}	$V_{DC}/2$	$-V_{DC}/4$	$3V_{DC}/4$
C_7	0	1	1	1	V_{DC}	$V_{DC}/2$	$-V_{DC}/4$	$3V_{DC}/4$
C_3	0	0	1	1	V_{DC}	0	$-V_{DC}/2$	$V_{DC}/2$

voltage, producing additional circulating current ripple. The solution to this follows the principles established for coupled inductor semi-bridge converters [23], in which additional transition states are included, with a half-carrier timing correction depending on whether the transition is rising or falling. In Fig. 13 this is shown as the additional 24 states between rows 1 and 2, and 3 and 4. More details concerning these row transitions can be found in [23].

The process of developing a state machine for an MMC with a large number of sub-modules follows the same basic principles established above and also documented in [22] and [23]. However considerable labor is required to develop a state machine as N increases, since the state machine size is proportional to N^2. Hence it may be desirable to implement PD PWM on a per-phase basis using a sort and select type algorithm [4][9][11]-[14] or virtual mapping technique [16][17]. However any such framework would need to consider sub-modules across the entire phase leg, and not just within each MMC arm.

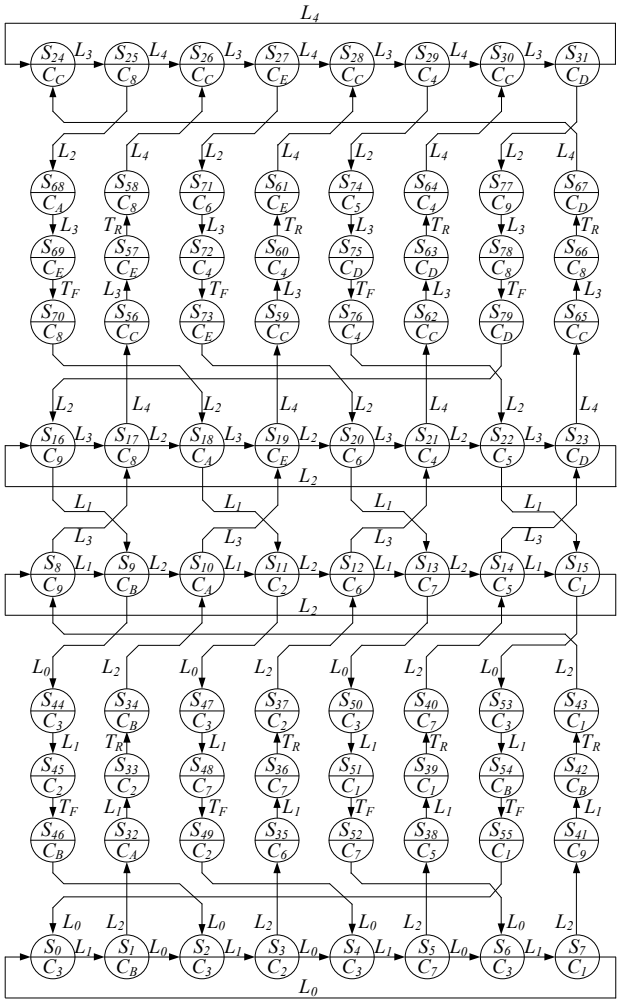


Fig. 13: State machine decoder for coordinated phase-leg based PDPWM of a five level single phase leg modular multilevel converter.

TABLE II: SYSTEM PARAMETERS

Description	Label	Value
Number of modules per arm	N	2
dc-link voltage	V_{dc}	400 V
Fundamental frequency	f_o	50 Hz
Individual module switching frequency	f_m	500 Hz
Effective switching frequency	f_c	2 kHz
Modulation depth	M	0.9
Individual module bus capacitors	C_{dc}	2,700 µF
Coupled-inductor		
Self-inductance	L	2.0 mH
Leakage-inductance	L_k	0.1 mH
Mutual-inductance	L_b	1.9 mH
Individual winding-resistance	R_w	50 mΩ
Load resistance		19.2 Ω

V. SIMULATION AND EXPERIMENTAL RESULTS

The theoretical concepts presented in this paper have been validated using PSIM models, and a prototype MMC with parameters detailed in Table II. The MMC was modulated using a Texas Instruments TMS320F2812 processor, with the state machine decoder implemented on an Altera MAX-II EPM570T100C5 CPLD.

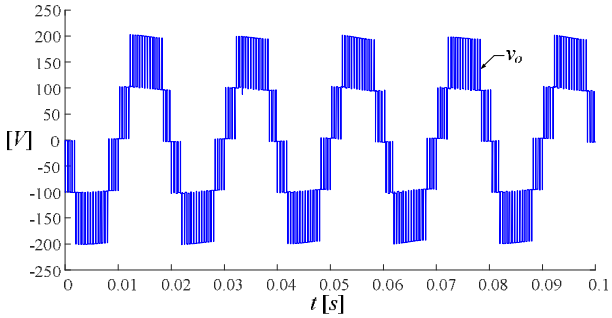
Fig. 14 shows the simulated phase "a" MMC waveforms for a load transient considering a reduction in load inductance from 110mH to 45mH at 0.033s, corresponding to a change in lagging power factor from 0.5 to 0.8. These results show the production of five distinct voltage levels in the phase voltage output (a), as expected for the integrated PD PWM implementation. Furthermore, Fig. 14 confirms that the state machine of Fig. 13 can control the MMC sub-module voltages (d), with balanced capacitor voltage despite the load transient and change in the load, circulating (c) and upper and lower arm (b) currents.

Fig. 15 shows experimental waveforms for one phase leg of the MMC for a load inductance of 4mH, corresponding to a lagging load power factor of 0.99. Again the distinct five voltage levels are evident (a) as expected for the integrated PD PWM process. The balanced upper and lower arm currents (b) combined with the balanced sub-module capacitor voltages (c) validates that the state machine can exploit the MMC natural balance property in a similar way as has been reported for flying capacitor inverters [22].

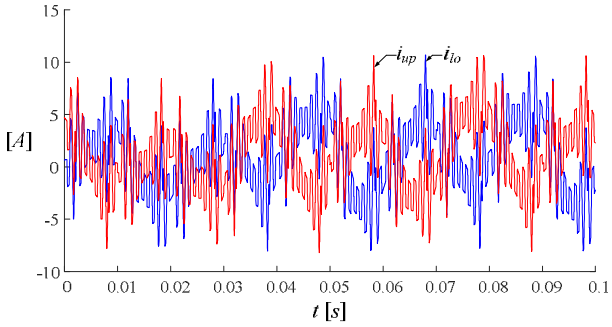
Fig. 16 compares the simulated and experimental MMC phase voltage spectrum, which clearly shows the large dominant carrier harmonic expected for PD PWM, which will cancel in the line to line output voltage and hence reduce the overall inverter distortion. These results confirm that PWM of the overall MMC phase leg with a $2N+1$ PD strategy and an associated state machine can fully utilise all available MMC voltage levels, while still exploiting the superior harmonic properties of the PD PWM strategy.

VI. CONCLUSION

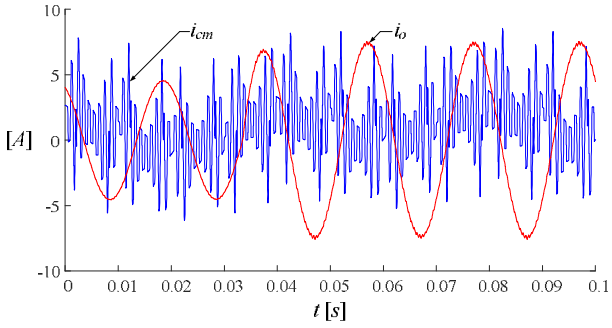
This paper has presented an analytical study of the harmonic performance of interleaved PD and PSCPWM for



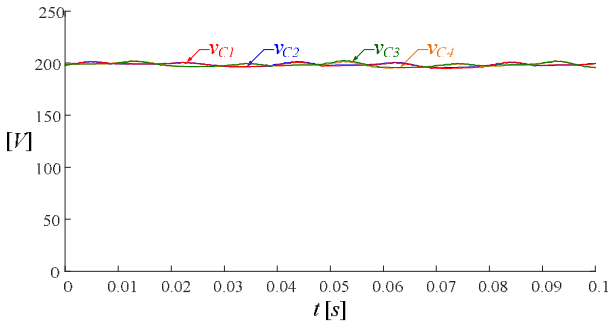
(a) Switched phase voltage.



(b) MMC upper and lower arm currents.

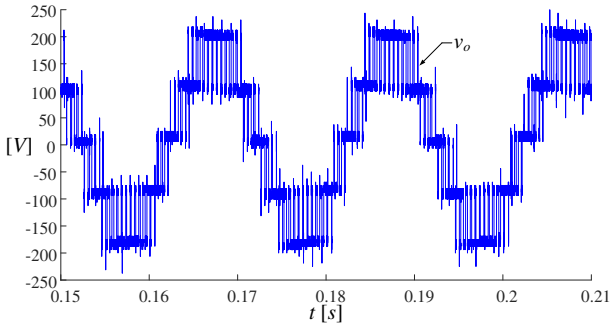


(c) MMC output and circulating currents.

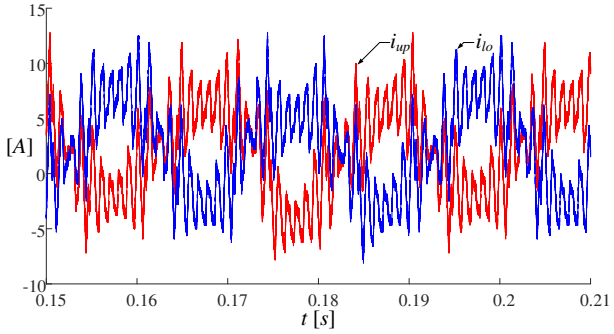


(d) Sub-module capacitor voltages.

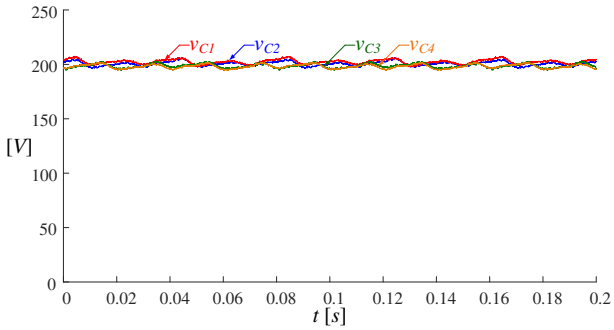
Fig. 14. Simulated phase "a" MMC waveforms – Load transient considering a 0.5 to 0.8 lagging power factor transition at 0.033s.



(a) Switched phase voltage.



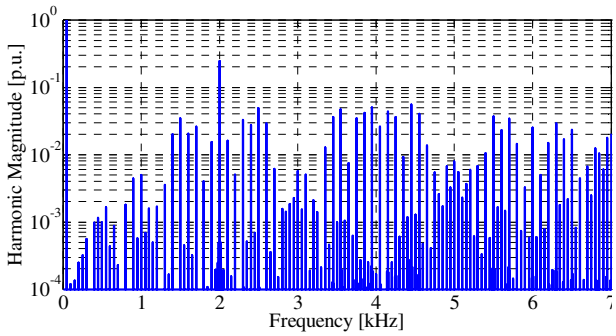
(b) MMC upper and lower arm currents.



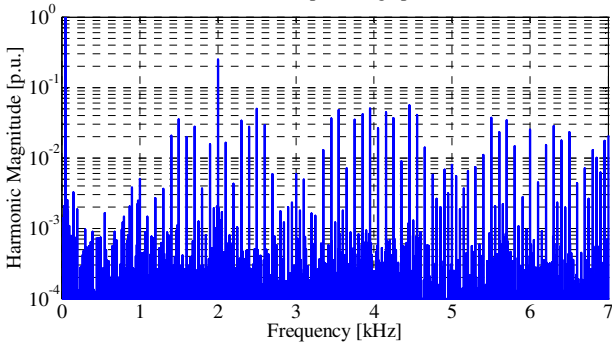
(c) Sub-module capacitor voltages.

Fig. 15. Experimental phase "a" steady state MMC waveforms for a lagging load power factor of 0.99.

MMC converters. The analysis has shown that both strategies produce the same differential mode harmonics across the upper and lower MMC arms, and hence must have the same output spectral performance. It is then shown that to realise the harmonic benefits of the PD strategy while synthesising $2N+1$ voltage levels it is necessary to modulate the entire phase leg structure with an over-arching PD strategy, which must then be decoded to select phase leg states that manage the common mode voltage and hence the circulating current. Finally a state machine methodology is presented that evenly distributes switching pulses across the upper and lower arm cells. The resulting strategy achieves optimum phase leg PD spectral performance, and naturally balances the MMC sub-module voltages.



(a) Simulated MMC phase leg spectrum.



(b) Experimental MMC phase leg spectrum.

Fig. 16. Spectral Comparison: f_c = 2kHz, f_o = 50Hz, M = 0.9.

ACKNOWLEDGEMENT

The authors acknowledge the financial support from the Australian Research Council under project DP140102437.

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